

General Description

The WSP2088 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the small power switching and load switch applications.

The WSP2088 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent C_{dv}/dt effect decline
- Green Device Available

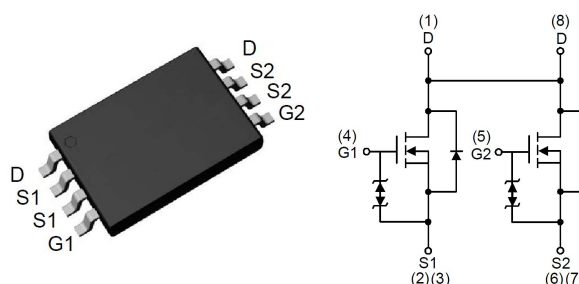
Product Summary

BV_{DSS}	$R_{DS(on)}$	I_D
20V	11.5m Ω	7.5A

Applications

- High Frequency Point-of-Load Synchronous
Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- ESD:2KV

TSSOP-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D@T_c=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	7.5	A
$I_D@T_c=70^{\circ}C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	6	A
I_{DM}	Pulsed Drain Current ²	30	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation ³	1.25	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	100	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	70	$^{\circ}C/W$

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.022	---	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=7.5A$	---	11.5	14.5	$m\Omega$
		$V_{GS}=2.5V, I_D=5A$	---	14.5	20	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.5	0.7	1.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-2.33	---	$mV/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=16V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=16V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=5A$	---	36	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	4	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=10V, V_{GS}=4.5V, I_D=7.5A$	---	13.5	18	nC
Q_{gs}	Gate-Source Charge		---	1.5	---	
Q_{gd}	Gate-Drain Charge		---	5.8	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V, V_{GS}=4.5V, R_G=3.3\Omega, I_D=5A$	---	10.8	20	ns
T_r	Rise Time		---	14.5	26	
$T_{d(off)}$	Turn-Off Delay Time		---	51	55	
T_f	Fall Time		---	45	81	
C_{iss}	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1MHz$	---	900	---	pF
C_{oss}	Output Capacitance		---	175	---	
C_{rss}	Reverse Transfer Capacitance		---	160	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	1.5	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	30	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$	---	0.7	1.3	V
t_{rr}	Reverse Recovery Time	$I_F=7.5A, dI/dt=100A/\mu s, T_J=25^{\circ}\text{C}$	---	13.5	---	nS
Q_{rr}	Reverse Recovery Charge		---	4	---	nC

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, $t \leq 10\text{sec}$.

2.The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3.The power dissipation is limited by 150°C junction temperature

4.The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

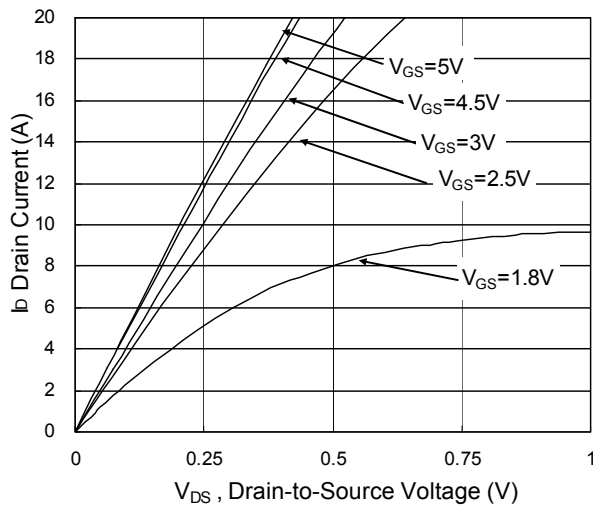


Fig.1 Typical Output Characteristics

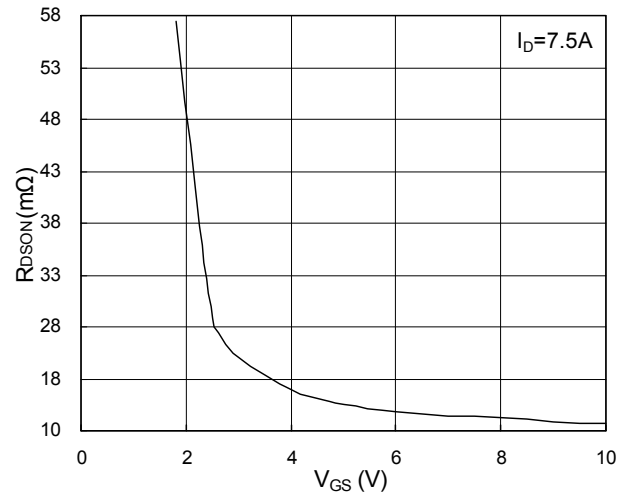


Fig.2 On-Resistance vs. Gate-Source

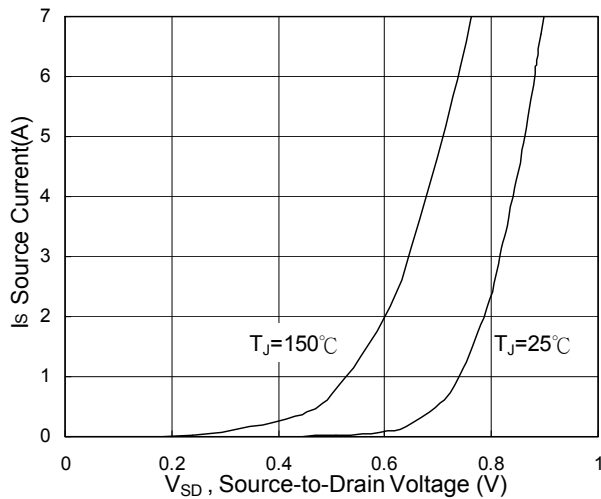


Fig.3 Forward Characteristics Of Reverse

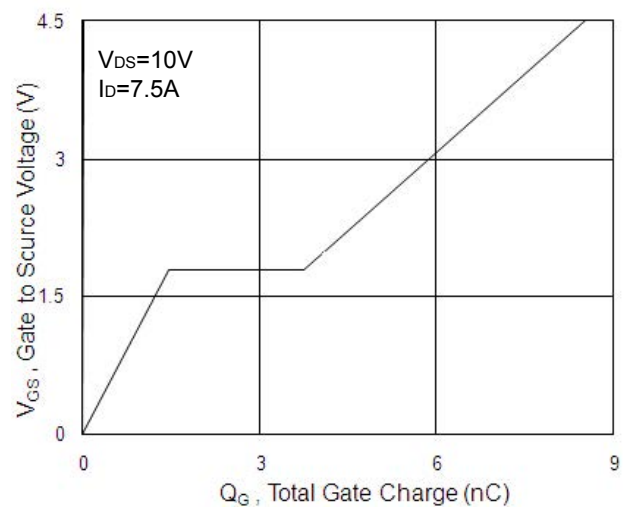


Fig.4 Gate-Charge Characteristics

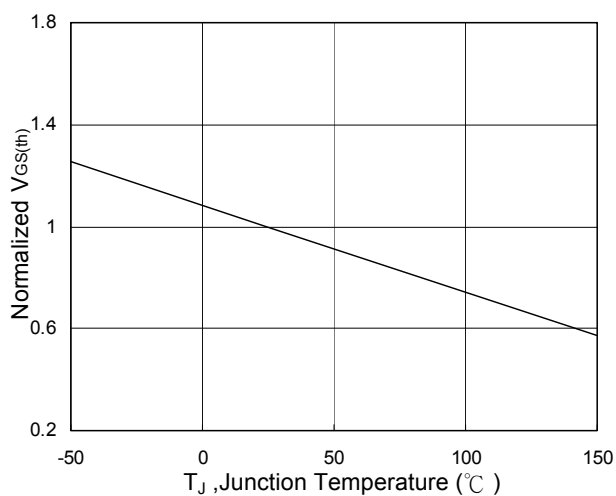


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

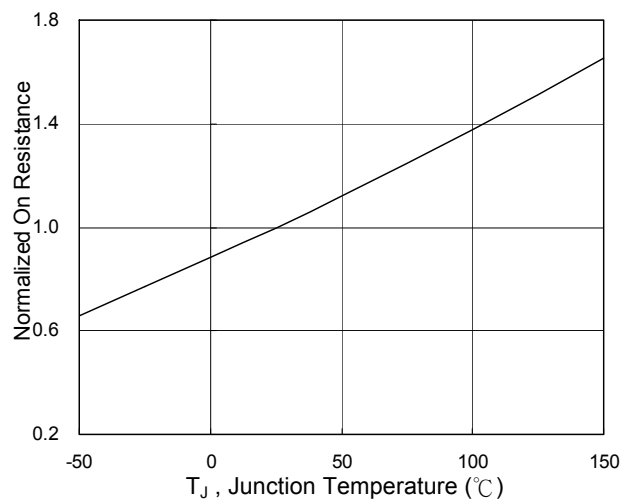


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

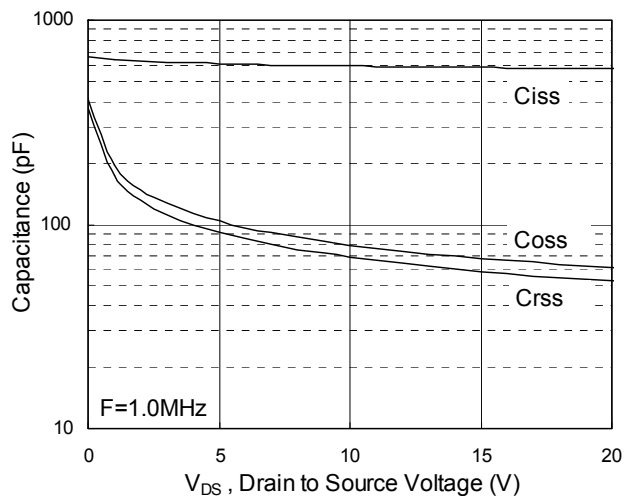


Fig.7 Capacitance

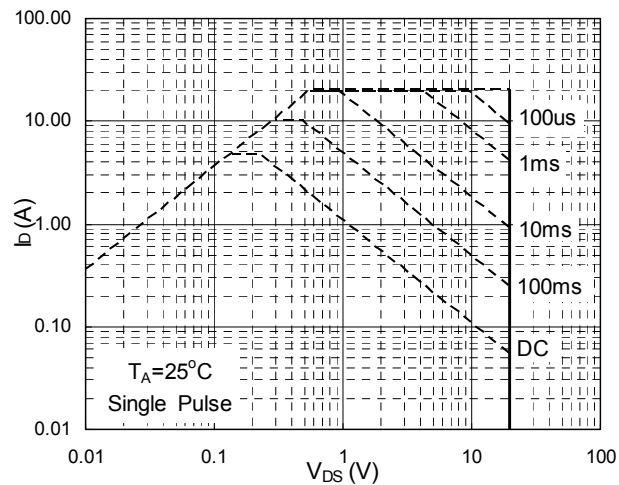


Fig.8 Safe Operating Area

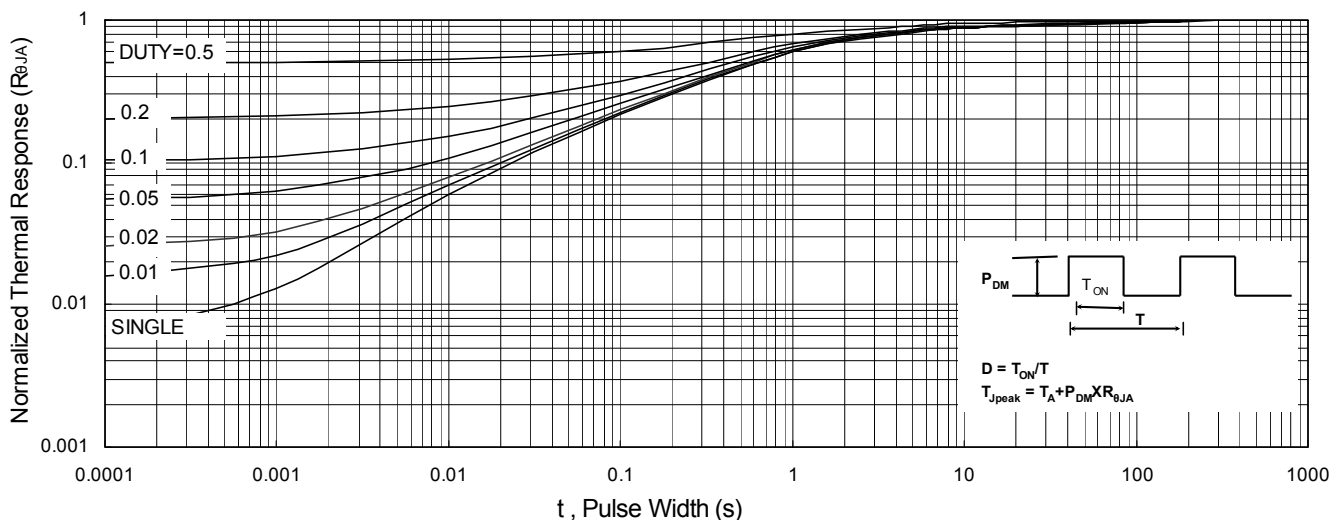


Fig.9 Normalized Maximum Transient Thermal Impedance

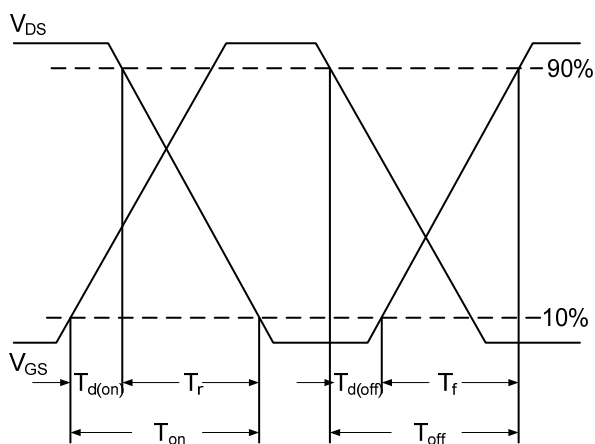


Fig.10 Switching Time Waveform

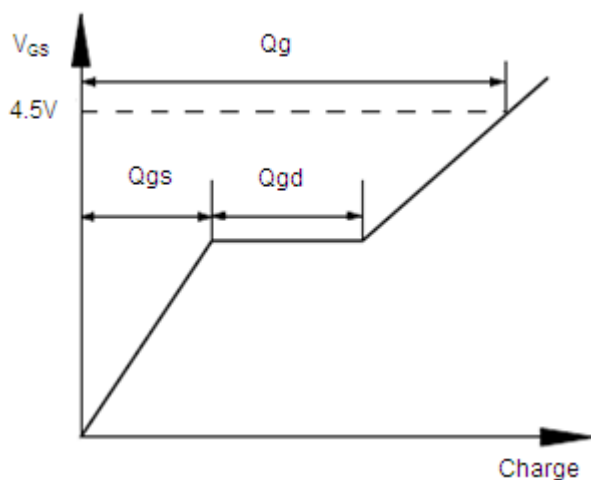


Fig.11 Gate Charge Waveform

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