RClamp3324P
Low Capacitance RailClamp®
4-Line Surge and ESD Protection

PROTECTION PRODUCTS

Description

RailClamp® 3324P provides ESD protection for high-speed data interfaces. It features a high maximum ESD withstand voltage of ±17kV contact and ±20kV air discharge per IEC 61000-4-2. RClamp3324P is designed to minimize both the ESD peak clamping and the TLP clamping. Package inductance is reduced at each pin resulting in lower peak ESD clamping voltage. The dynamic resistance is among the industry's lowest at 0.15 Ohms (typical). Maximum capacitance on each line to ground is 0.65pF allowing the RClamp3324P to be used in applications operating in excess of 5GHz without signal attenuation. Each device will protect up to four lines (two high-speed pairs).

RClamp3324P is in a 10-pin SGP2510P8 package measuring 2.5 x 1.0mm with a nominal height of 0.60mm. The leads have a nominal pin-to-pin pitch of 0.50mm. Flow- through package design simplifies PCB layout and maintains signal integrity on high-speed lines.

The combination of low peak ESD clamping, low dynamic resistance, and innovative package design enables this device to provide the highest level of ESD protection for applications such as USB 3.0, eSATA, and DisplayPort.

Features

- Transient Protection to
  - IEC 61000-4-2 (ESD) 20kV (Air), 17kV (Contact)
  - IEC 61000-4-4 (EFT) 4kV (5/50ns)
  - IEC 61000-4-5 (Lightning) 4.5A (8/20µs)
- Package design optimized for high speed layout
- Protects four high-speed data lines
- Working Voltage: 3.3V
- Low Capacitance: 0.65 pF maximum (I/O to GND)
- Dynamic Resistance: 0.15 Ohms (Typ)
- Solid-State Silicon-Avalanche Technology

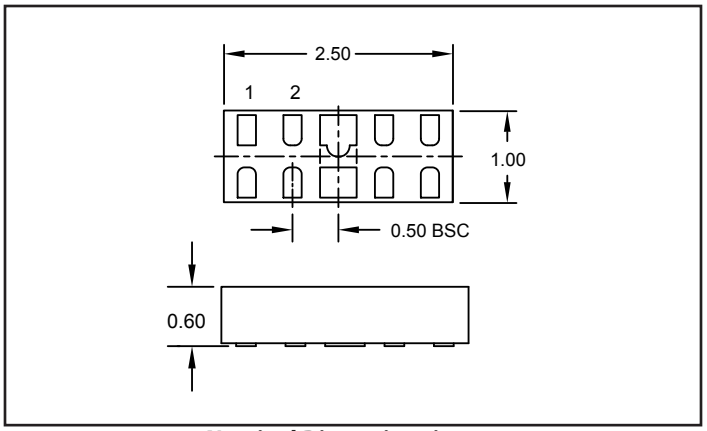
Mechanical Characteristics

- SGP2510P8 Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 2.5 x 1.0 x 0.60 mm
- Lead Finish: NiPdAu
- Molding Compound Flammability Rating: UL 94V-0
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

Applications

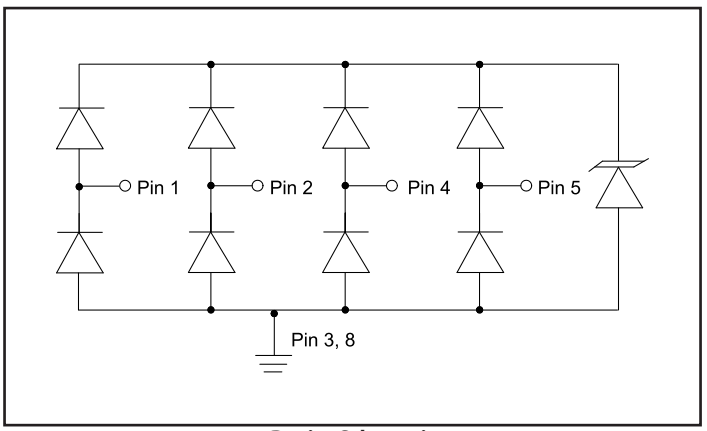
- USB 3.0
- Industrial Equipment
- Digital Visual Interface
- LVDS Interfaces
- eSATA

Nominal Dimension



Nominal Dimensions in mm

Functional Schematic



Device Schematic

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20µs)	I_{PP}	4.5	A
ESD per IEC 61000-4-2 (Contact)(1) ESD per IEC 61000-4-2 (Air)(1)	V_{ESD}	±17 ±20	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 125°C Any I/O pin to GND				3.3	V
Trigger Voltage	V_{TRIG}	tp = 0.2/100ns (TLP) Any I/O pin to GND			8		V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V	T = 25°C		0.01	0.05	µA
			T = 125°C			0.150	µA
Clamping Voltage(2)	V_C	I_{PP} = 1A, tp = 8/20µs, Any I/O pin to GND			2.5	3.5	V
Clamping Voltage(2)	V_C	I_{PP} = 4.5A, tp = 8/20µs, Any I/O pin to GND			3.5	4.5	V
ESD Clamping Voltage(3)	V_C	I_{PP} = 4A, tp = 0.2/100ns (TLP) Any I/O pin to GND			3.5		V
ESD Clamping Voltage(3)	V_C	I_{PP} = 16A, tp = 0.2/100ns (TLP) Any I/O pin to GND			5.3		V
Dynamic Resistance(3), (4)	R_{DYN}	tp = 0.2/100ns (TLP) Any I/O pin to GND			0.15		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz Any I/O pin to GND			0.60	0.65	pF
		V_R = 0V, f = 1MHz Between I/O Pins			0.30	0.40	pF

Notes:

(1): ESD Gun return path to Ground Reference Plane (GRP)

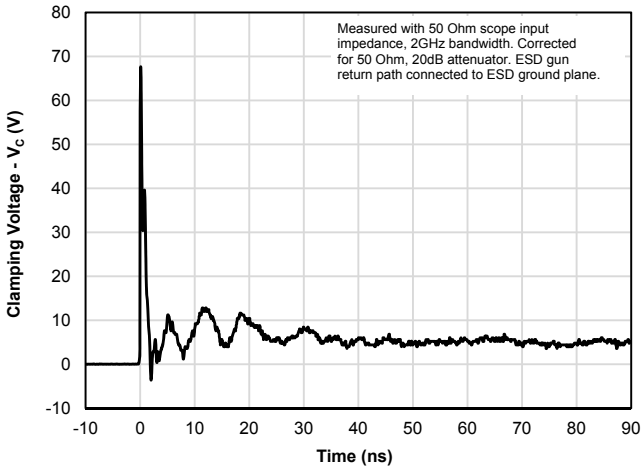
(2): Measured using an 8/20us constant current source.

(3): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.

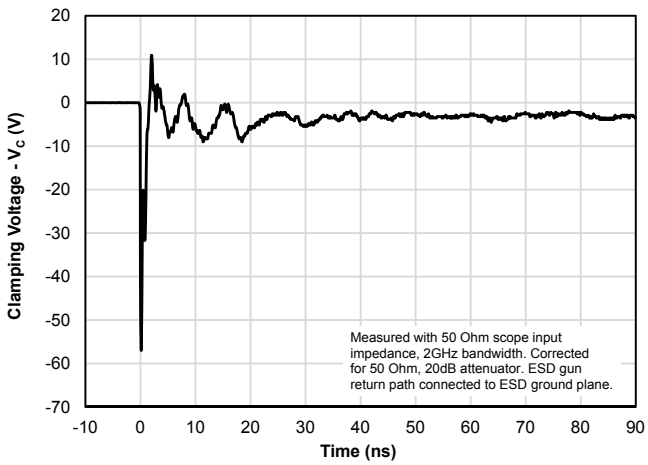
(4): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

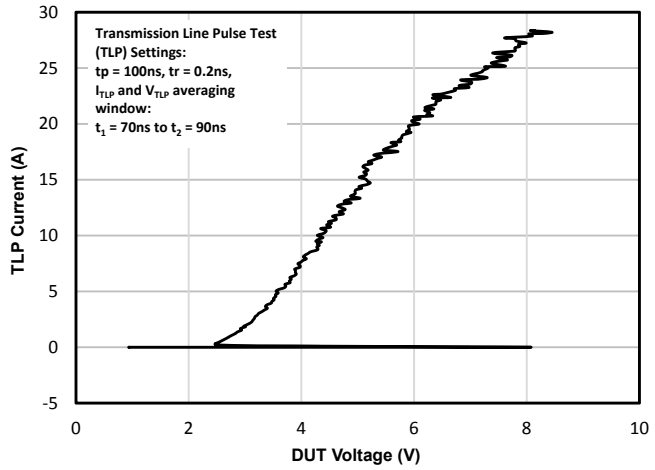
ESD Clamping (+8kV Contact per IEC 61000-4-2)



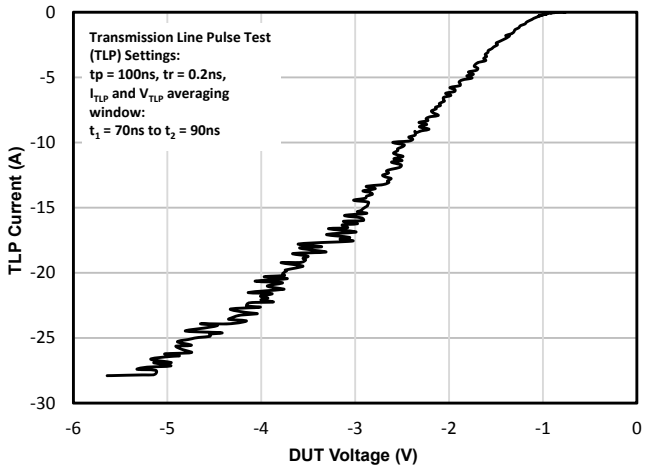
ESD Clamping (-8kV Contact per IEC 61000-4-2)



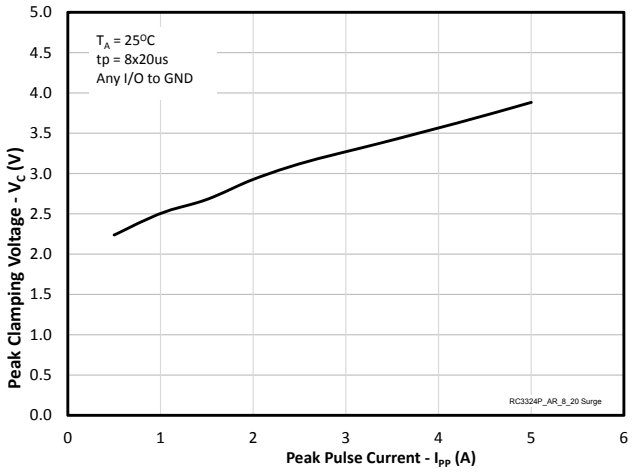
TLP Curve (Positive Pulse)



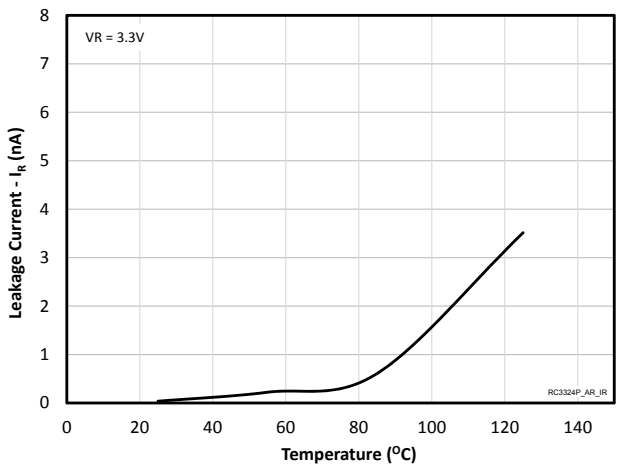
TLP Curve (Negative Pulse)



Clamping Voltage vs. Peak Pulse Current (tp=8/20us)

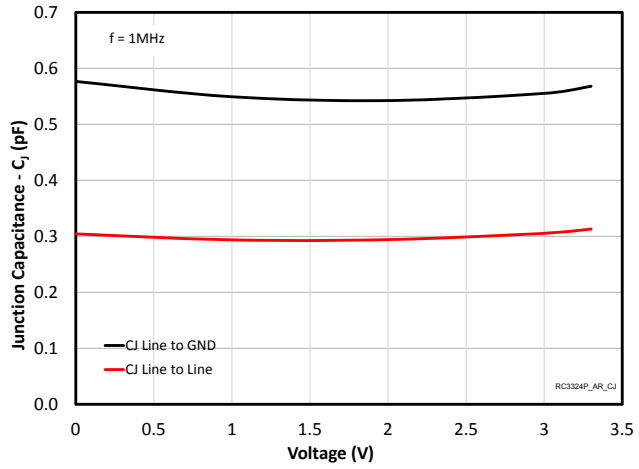


Reverse Leakage Current (I_R) vs. Temperature

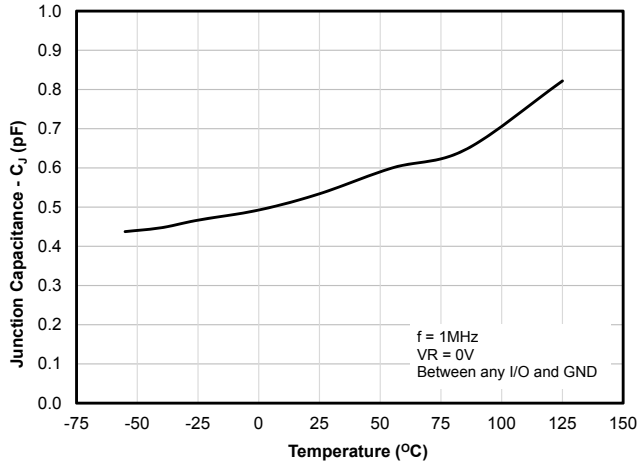


Typical Characteristics (Continued)

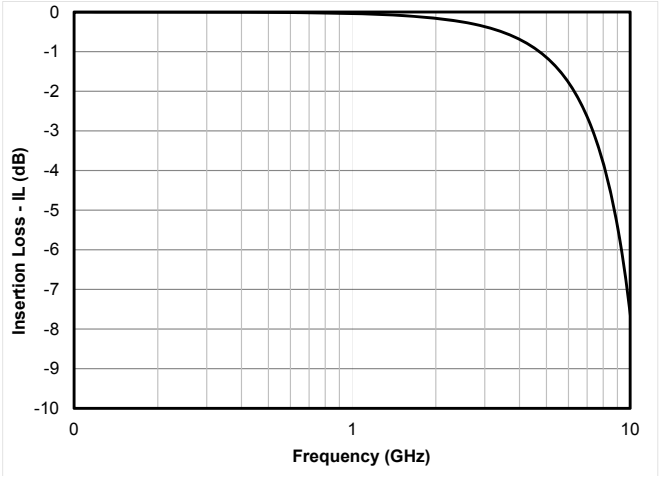
Capacitance vs. Reverse Voltage



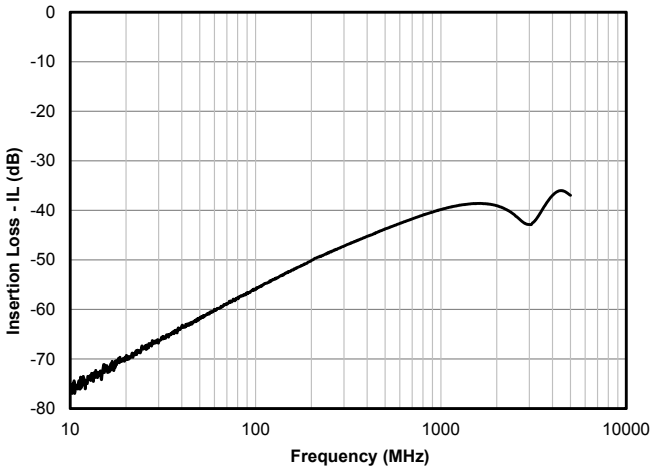
Capacitance vs. Temperature



Insertion Loss - S21



Analog Crosstalk



Application Information

USB Interface Protection

For USB 3.0 applications, RClamp3324P is recommended for protecting the 5Gb/s SuperSpeed line pairs. Figure 1 below shows an example of protecting a USB 3.0 Type-A interfaces (host side shown). Lines are routed through each device entering at pins 1, 2, 4, and 5 and exiting at pins 10, 9, 7, and 6 respectively (Figure 2). Each trace should run under the device and connect the pins together. Ground connection is made at the center tabs (pins 3, and 8). Traces should be kept the same length to avoid impedance mismatch. The differential impedance of each pair can be controlled for USB 3.0 (85 Ohms +/-15%) while maintaining a minimum trace-to-trace and trace-to-pad spacing. Individual PCB design constraints may necessitate different spacing or trace width. Both ground pads should be connected for optimal performance. Ground connection is made using filled via-in-pad.

RClamp0512TQ is be used to protect D+ and D- lines. These lines are routed through RClamp0512TQ at pin1 and pin 2. Pin 3 is connected to the ground plane. RClamp0512TQ is qualified to AEC-Q100. Additional information may be found on the device data sheet.

Single line devices such as uClamp0571P are recommended for surge and ESD protection of the VBus line. This device features high surge and ESD capability and may be used on 5V power rails. In power delivery (PD) applications, higher working voltage TVS device may be needed. Options exist for ESD and surge protection up to 24V.

Device Placement

Placement of the protection component is a critical element for effective ESD suppression. TVS diodes should be placed as close to the connector as possible. This helps reduce transient coupling to nearby traces. Ground connections should be made directly to the ground plane using micro-vias. This reduces parasitic inductance in the ground path and minimizes the clamping voltage seen by the protected device.

Figure 1 - USB 3.0 Type-A Protection Example

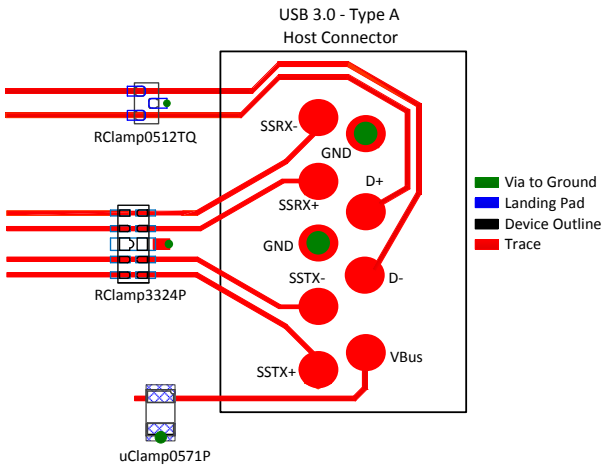
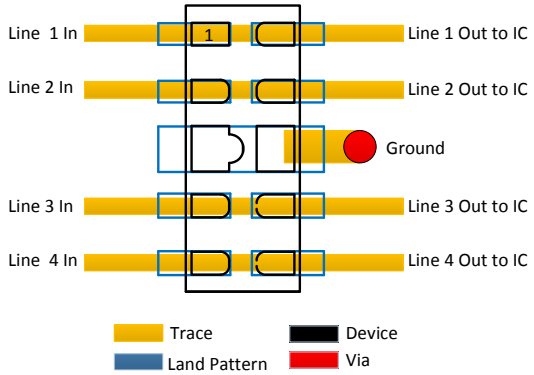
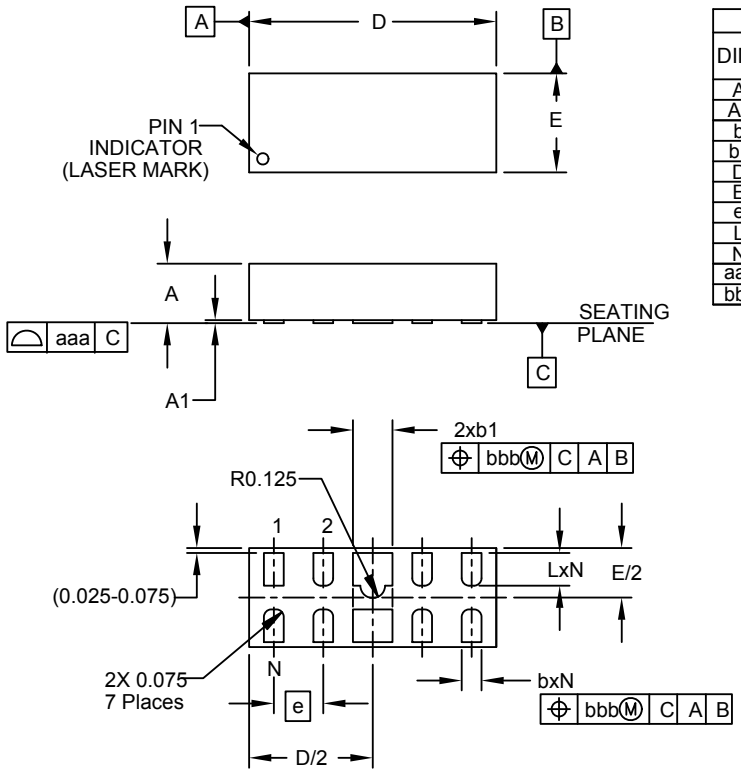


Figure 2 - Trace Routing



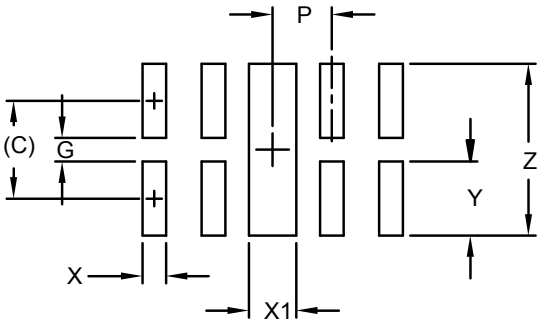
Outline Drawing - SGP2510P8



DIM	DIMENSIONS MILLIMETERS MIN	NOM	MAX
A	0.57	0.60	0.63
A1	0.00	0.03	0.05
b	0.15	0.20	0.25
b1	0.35	0.40	0.45
D	2.45	2.50	2.575
E	0.95	1.00	1.075
e	0.50 BSC		
L	0.28	0.33	0.38
N	8		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

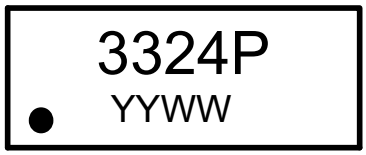
Land Pattern - SGP2510P8



DIM	DIMENSIONS MILLIMETERS
C	(0.825)
G	0.20
P	0.50
X	0.20
X1	0.40
Y	0.625
Z	1.45

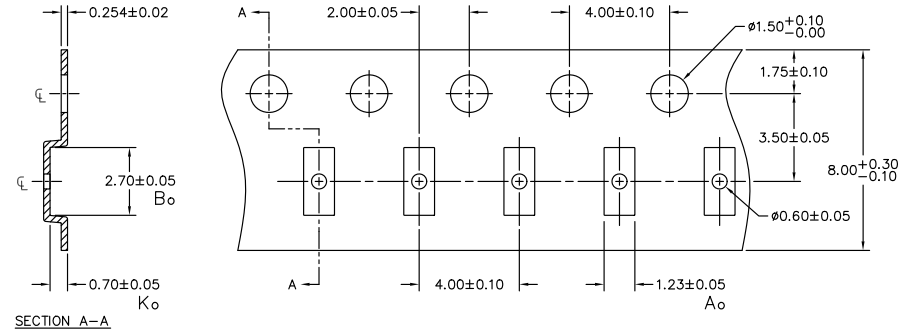
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



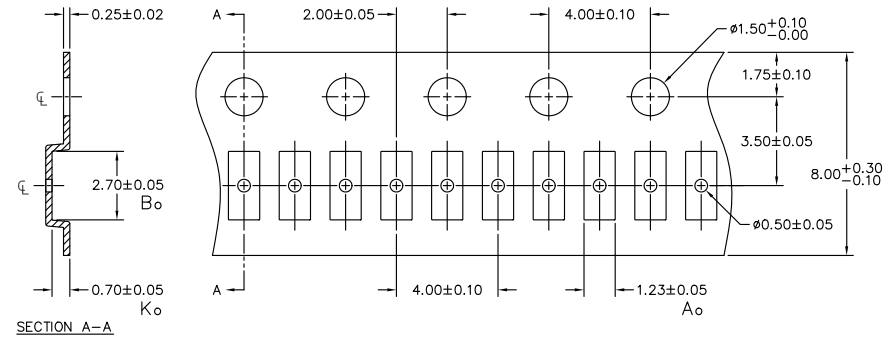
Notes: Dot indicates pin 1 location

Tape and Reel Specification



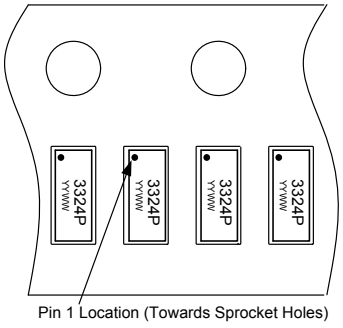
NOTES: 1.) ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

Carrier Tape, 4mm Pitch Option



NOTES: 1.) ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

Carrier Tape, 2mm Pitch Option



Device Orientation in Tape

Ordering Information

Part Number	Qty per Reel	Pocket Pitch	Reel Size
RClamp3324P.TCT	3,000	4mm	7″
RClamp3324P.TNT	10,000	2mm	7″
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