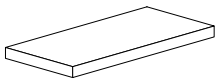
88-common x 132-segment BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6677 is a bit map LCD driver to display graphics or characters. It contains 15,840 bits display data RAM, microprocessor interface circuits, instruction decoder, 132-segment and 88-common drivers.
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel interface.
The NJU6677 displays 88 x 132 dots graphics or 8-character 5-line by 16 x 16 dots character.
It oscillates by built-in OSC circuit without any external components.
Furthermore, the NJU6677 features Partial Display Function which creates up to 2 blocks of active display area and optimizes duty cycle ratio. This function sets optimum boosted voltage by the combination with both of programmable 5-time voltage booster circuit and 201-step electrical variable resistor. As result, it reduces the operating current.
The operating voltage from 2.4V to 3.6V and low operating current are useful for small size battery operating items.

■ PACKAGE OUTLINE



NJU6677CL

■ FEATURES

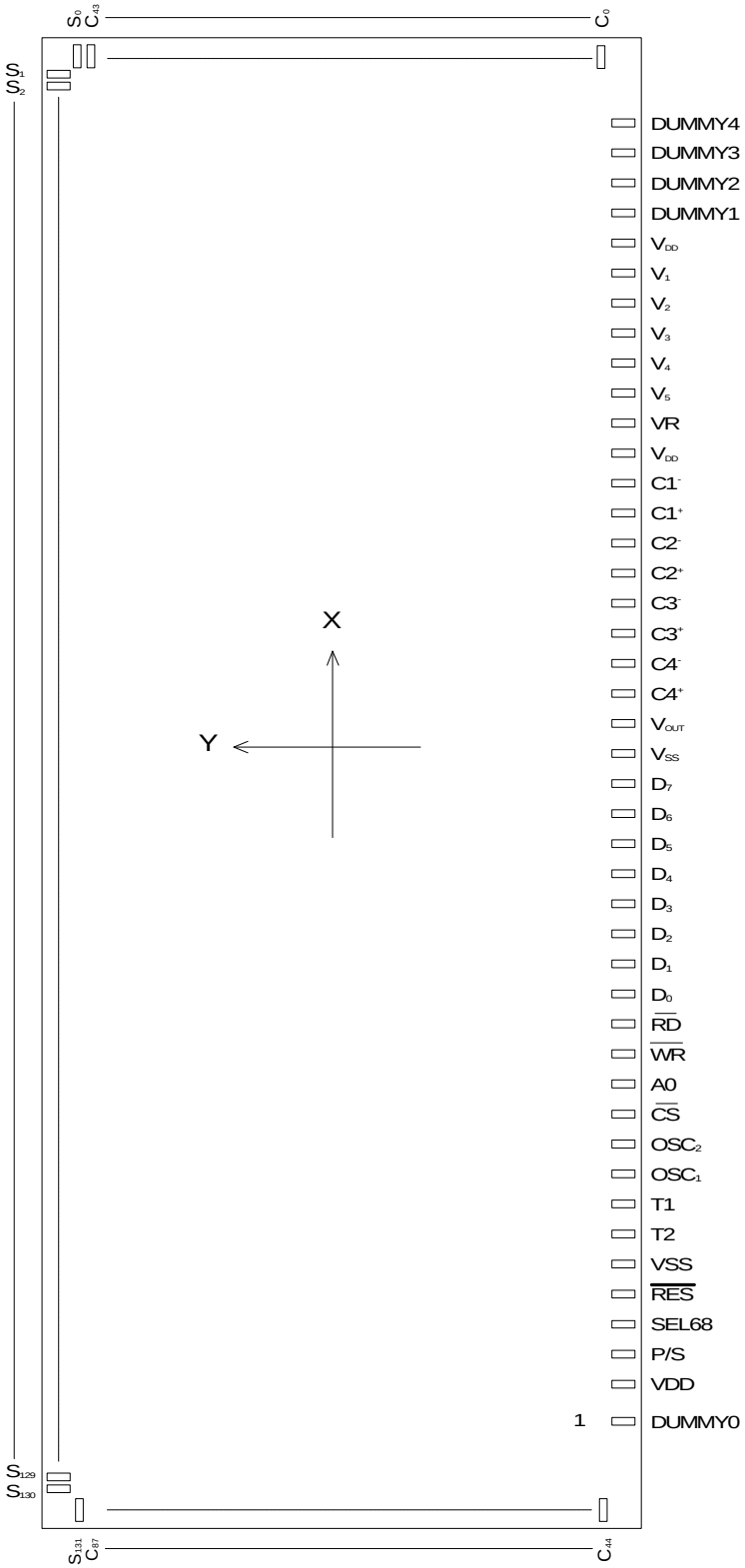
- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 15,840 bits
- 220 LCD Drivers - 88-common and 132-segment
- Direct Microprocessor Interface for both of 68 and 80 type MPU
- Serial Interface
- Partial Display Function
  (2 blocks of active display area and automatic duty cycle ratio selection)
- Easy Vertical Scroll by the variable start line address and over size display data RAM
- Programmable Bias selection ; 1/4,1/5,1/6,1/7,1/8,1/9,1/10 bias
- Common Driver Order Assignment by mask option

Version	C_0 to C_{87}(Pin name)
NJU6677A	Com_0 to Com_{87}
NJU6677B	Com_{87} to Com_0

- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Display Start Line Set, Partial Display, Bias Select, Column Address Set, Status Read, All On/Off, Voltage Booster Circuits Multiple Select(Maximum 5-time), n-Line Inverse, Read Modify Write, Power Saving, ADC Select, etc.
- Power Supply Circuits for LCD; Programmable Voltage Booster Circuits(5-time Maximum), Regulator, Voltage Follower x 4
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.4V to 3.6V
- LCD Driving Voltage --- 6.0V to 18V
- Package Outline --- COF / TCP / Bumped Chip
- C-MOS Technology

JUL.10.2000
Ver.2.1

■ PAD LOCATION



Chip Center	: X=0um,Y=0um
Chip Size	: X=8.31mm,Y=2.93mm
Chip Thickness	: 675um ± 30um
Bump Size	: 45um x 83um
Pad pitch	: 60um(Min)
Bump Height	: 15um TYP.
Bump Material	: Au

■ TERMINAL DESCRIPTION

Chip Size 8.31x2.93mm (Chip Center X=0um,Y=0um)

PAD No.	Terminal	X= um	Y= um
1	DUMMY0	-3884.0	-1305.0
2	V_{DD}	-3179.2	-1305.0
3	P/S	-3014.1	-1305.0
4	SEL68	-2793.7	-1305.0
5	$\overline{RES}$	-2557.3	-1305.0
6	V_{SS}	-2400.1	-1305.0
7	T_2	-2242.9	-1305.0
8	T_1	-2007.3	-1305.0
9	OSC_1	-1786.9	-1305.0
10	OSC_2	-1550.5	-1305.0
11	$\overline{CS}$	-1330.1	-1305.0
12	A0	-1093.7	-1305.0
13	$\overline{WR}$	-873.3	-1305.0
14	$\overline{RD}$	-636.9	-1305.0
15	D_0	-400.2	-1305.0
16	D_1	-179.8	-1305.0
17	D_2	40.6	-1305.0
18	D_3	261.0	-1305.0
19	D_4	481.4	-1305.0
20	D_5	701.8	-1305.0
21	$D_{6(SCL)}$	922.2	-1305.0
22	$D_{7(SI)}$	1142.6	-1305.0
23	V_{SS}	1300.1	-1305.0
24	V_{OUT}	1370.1	-1305.0
25	$C4^+$	1466.0	-1305.0
26	$C4^-$	1614.8	-1305.0
27	$C3^+$	1674.8	-1305.0
28	$C3^-$	1823.6	-1305.0
29	$C2^+$	1883.6	-1305.0
30	$C2^-$	2032.4	-1305.0
31	$C1^+$	2092.4	-1305.0
32	$C1^-$	2241.2	-1305.0
33	V_{DD}	2311.2	-1305.0
34	VR	2491.2	-1305.0
35	V_5	2561.2	-1305.0
36	V_4	2631.2	-1305.0
37	V_3	2701.2	-1305.0
38	V_2	2771.2	-1305.0
39	V_1	2841.2	-1305.0
40	V_{DD}	2911.2	-1305.0
41	DUMMY1	3119.2	-1305.0
42	DUMMY2	3179.2	-1305.0
43	DUMMY3	3239.2	-1305.0
44	DUMMY4	3884.0	-1305.0
45	C_0	3995.0	-1318.1
46	C_1	3995.0	-1258.1
47	C_2	3995.0	-1198.1
48	C_3	3995.0	-1138.1
49	C_4	3995.0	-1078.1
50	C_5	3995.0	-1018.1

PAD No.	Terminal	X= um	Y= um
51	C_6	3995.0	-958.1
52	C_7	3995.0	-898.1
53	C_8	3995.0	-838.1
54	C_9	3995.0	-778.1
55	C_{10}	3995.0	-718.1
56	C_{11}	3995.0	-658.1
57	C_{12}	3995.0	-598.1
58	C_{13}	3995.0	-538.1
59	C_{14}	3995.0	-478.1
60	C_{15}	3995.0	-418.1
61	C_{16}	3995.0	-358.1
62	C_{17}	3995.0	-298.1
63	C_{18}	3995.0	-238.1
64	C_{19}	3995.0	-178.1
65	C_{20}	3995.0	-118.1
66	C_{21}	3995.0	-58.1
67	C_{22}	3995.0	1.9
68	C_{23}	3995.0	61.9
69	C_{24}	3995.0	121.9
70	C_{25}	3995.0	181.9
71	C_{26}	3995.0	241.9
72	C_{27}	3995.0	301.9
73	C_{28}	3995.0	361.9
74	C_{29}	3995.0	421.9
75	C_{30}	3995.0	481.9
76	C_{31}	3995.0	541.9
77	C_{32}	3995.0	601.9
78	C_{33}	3995.0	661.9
79	C_{34}	3995.0	721.9
80	C_{35}	3995.0	781.9
81	C_{36}	3995.0	841.9
82	C_{37}	3995.0	901.9
83	C_{38}	3995.0	961.9
84	C_{39}	3995.0	1021.9
85	C_{40}	3995.0	1081.9
86	C_{41}	3995.0	1141.9
87	C_{42}	3995.0	1201.9
88	C_{43}	3995.0	1261.9
89	S_0	3995.0	1321.9
90	S_1	3870.0	1305.0
91	S_2	3810.0	1305.0
92	S_3	3750.0	1305.0
93	S_4	3690.0	1305.0
94	S_5	3630.0	1305.0
95	S_6	3570.0	1305.0
96	S_7	3510.0	1305.0
97	S_8	3450.0	1305.0
98	S_9	3390.0	1305.0
99	S_{10}	3330.0	1305.0
100	S_{11}	3270.0	1305.0

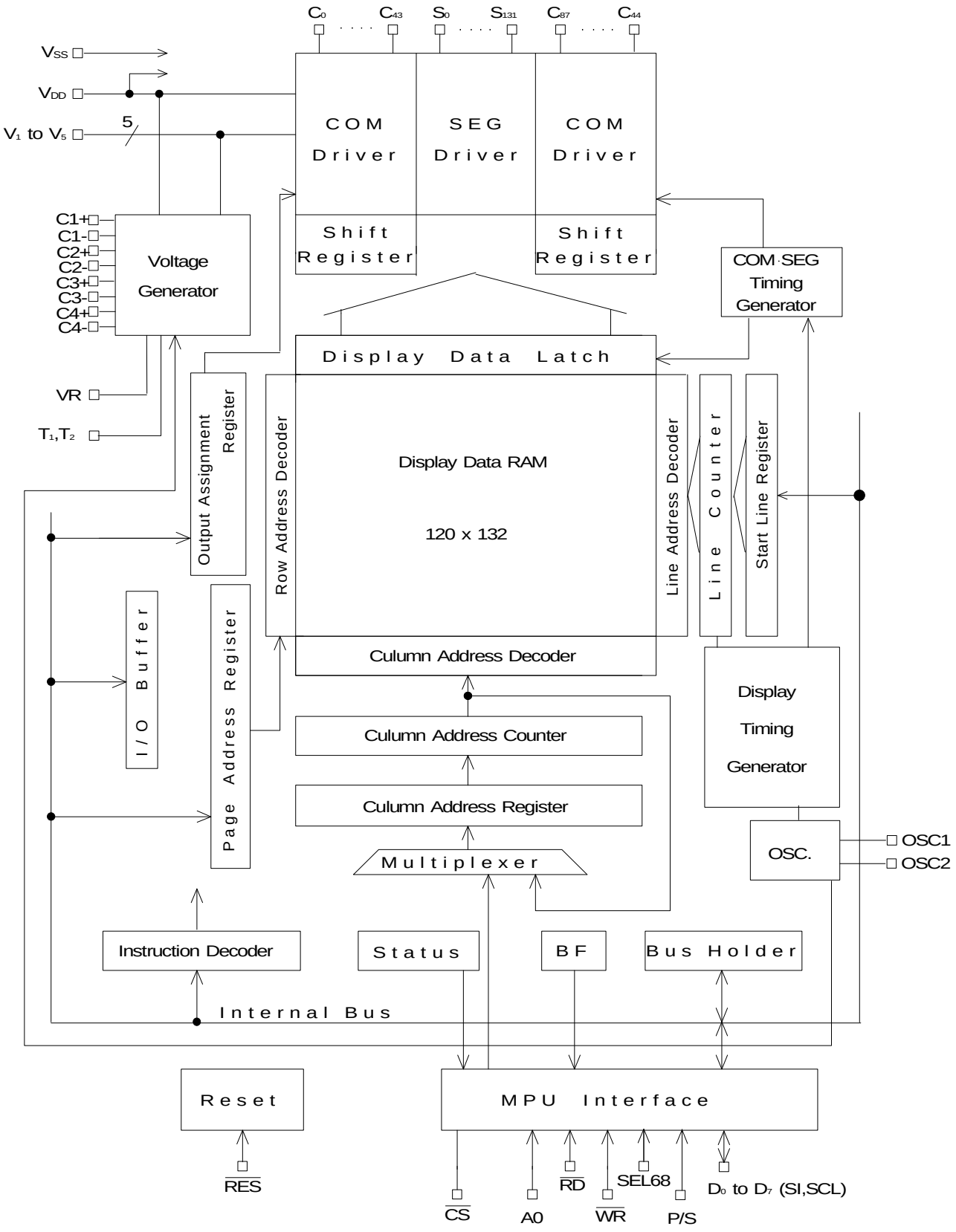
PAD No.	Terminal	X= um	Y= um
101	S12	3210.0	1305.0
102	S13	3150.0	1305.0
103	S14	3090.0	1305.0
104	S15	3030.0	1305.0
105	S16	2970.0	1305.0
106	S17	2910.0	1305.0
107	S18	2850.0	1305.0
108	S19	2790.0	1305.0
109	S20	2730.0	1305.0
110	S21	2670.0	1305.0
111	S22	2610.0	1305.0
112	S23	2550.0	1305.0
113	S24	2490.0	1305.0
114	S25	2430.0	1305.0
115	S26	2370.0	1305.0
116	S27	2310.0	1305.0
117	S28	2250.0	1305.0
118	S29	2190.0	1305.0
119	S30	2130.0	1305.0
120	S31	2070.0	1305.0
121	S32	2010.0	1305.0
122	S33	1950.0	1305.0
123	S34	1890.0	1305.0
124	S35	1830.0	1305.0
125	S36	1770.0	1305.0
126	S37	1710.0	1305.0
127	S38	1650.0	1305.0
128	S39	1590.0	1305.0
129	S40	1530.0	1305.0
130	S41	1470.0	1305.0
131	S42	1410.0	1305.0
132	S43	1350.0	1305.0
133	S44	1290.0	1305.0
134	S45	1230.0	1305.0
135	S46	1170.0	1305.0
136	S47	1110.0	1305.0
137	S48	1050.0	1305.0
138	S49	990.0	1305.0
139	S50	930.0	1305.0
140	S51	870.0	1305.0
141	S52	810.0	1305.0
142	S53	750.0	1305.0
143	S54	690.0	1305.0
144	S55	630.0	1305.0
145	S56	570.0	1305.0
146	S57	510.0	1305.0
147	S58	450.0	1305.0
148	S59	390.0	1305.0
149	S60	330.0	1305.0
150	S61	270.0	1305.0

PAD No.	Terminal	X= um	Y= um
151	S62	210.0	1305.0
152	S63	150.0	1305.0
153	S64	90.0	1305.0
154	S65	30.0	1305.0
155	S66	-30.0	1305.0
156	S67	-90.0	1305.0
157	S68	-150.0	1305.0
158	S69	-210.0	1305.0
159	S70	-270.0	1305.0
160	S71	-330.0	1305.0
161	S72	-390.0	1305.0
162	S73	-450.0	1305.0
163	S74	-510.0	1305.0
164	S75	-570.0	1305.0
165	S76	-630.0	1305.0
166	S77	-690.0	1305.0
167	S78	-750.0	1305.0
168	S79	-810.0	1305.0
169	S80	-870.0	1305.0
170	S81	-930.0	1305.0
171	S82	-990.0	1305.0
172	S83	-1050.0	1305.0
173	S84	-1110.0	1305.0
174	S85	-1170.0	1305.0
175	S86	-1230.0	1305.0
176	S87	-1290.0	1305.0
177	S88	-1350.0	1305.0
178	S89	-1410.0	1305.0
179	S90	-1470.0	1305.0
180	S91	-1530.0	1305.0
181	S92	-1590.0	1305.0
182	S93	-1650.0	1305.0
183	S94	-1710.0	1305.0
184	S95	-1770.0	1305.0
185	S96	-1830.0	1305.0
186	S97	-1890.0	1305.0
187	S98	-1950.0	1305.0
188	S99	-2010.0	1305.0
189	S100	-2070.0	1305.0
190	S101	-2130.0	1305.0
191	S102	-2190.0	1305.0
192	S103	-2250.0	1305.0
193	S104	-2310.0	1305.0
194	S105	-2370.0	1305.0
195	S106	-2430.0	1305.0
196	S107	-2490.0	1305.0
197	S108	-2550.0	1305.0
198	S109	-2610.0	1305.0
199	S110	-2670.0	1305.0
200	S111	-2730.0	1305.0

PAD No.	Terminal	X= um	Y= um
201	S112	-2790.0	1305.0
202	S113	-2850.0	1305.0
203	S114	-2910.0	1305.0
204	S115	-2970.0	1305.0
205	S116	-3030.0	1305.0
206	S117	-3090.0	1305.0
207	S118	-3150.0	1305.0
208	S119	-3210.0	1305.0
209	S120	-3270.0	1305.0
210	S121	-3330.0	1305.0
211	S122	-3390.0	1305.0
212	S123	-3450.0	1305.0
213	S124	-3510.0	1305.0
214	S125	-3570.0	1305.0
215	S126	-3630.0	1305.0
216	S127	-3690.0	1305.0
217	S128	-3750.0	1305.0
218	S129	-3810.0	1305.0
219	S130	-3870.0	1305.0
220	S131	-3995.0	1321.9
221	C87	-3995.0	1261.9
222	C86	-3995.0	1201.9
223	C85	-3995.0	1141.9
224	C84	-3995.0	1081.9
225	C83	-3995.0	1021.9
226	C82	-3995.0	961.9
227	C81	-3995.0	901.9
228	C80	-3995.0	841.9
229	C79	-3995.0	781.9
230	C78	-3995.0	721.9
231	C77	-3995.0	661.9
232	C76	-3995.0	601.9
233	C75	-3995.0	541.9
234	C74	-3995.0	481.9
235	C73	-3995.0	421.9
236	C72	-3995.0	361.9
237	C71	-3995.0	301.9
238	C70	-3995.0	241.9
239	C69	-3995.0	181.9
240	C68	-3995.0	121.9
241	C67	-3995.0	61.9
242	C66	-3995.0	1.9
243	C65	-3995.0	-58.1
244	C64	-3995.0	-118.1
245	C63	-3995.0	-178.1
246	C62	-3995.0	-238.1
247	C61	-3995.0	-298.1
248	C60	-3995.0	-358.1
249	C59	-3995.0	-418.1
250	C58	-3995.0	-478.1

PAD No.	Terminal	X= um	Y= um
251	C57	-3995.0	-538.1
252	C56	-3995.0	-598.1
253	C55	-3995.0	-658.1
254	C54	-3995.0	-718.1
255	C53	-3995.0	-778.1
256	C52	-3995.0	-838.1
257	C51	-3995.0	-898.1
258	C50	-3995.0	-958.1
259	C49	-3995.0	-1018.1
260	C48	-3995.0	-1078.1
261	C47	-3995.0	-1138.1
262	C46	-3995.0	-1198.1
263	C45	-3995.0	-1258.1
264	C44	-3995.0	-1318.1

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>1,41 to 44</td><td>DUMMY0
to
DUMMY4</td><td></td><td>Dummy Terminals.
These terminals are insulated.</td></tr>
<tr><td>2,33,40</td><td>V_{DD}</td><td>Power</td><td>V_{DD}=+3V</td></tr>
<tr><td>6,23</td><td>V_{SS}</td><td>GND</td><td>V_{SS}=0V</td></tr>
<tr><td>39,
38,
37,
36,
35</td><td>V_1
V_2
V_3
V_4
V_5</td><td>Power</td><td>LCD Driving Voltage Supplying Terminal. When the internal voltage booster is not used, supply each level of LCD driving voltage from outside with following relation.
VDD≧V1≧V2≧V3≧V4≧V5
When the internal power supply is on, the internal circuits generate and supply following LCD bias voltage from V_1 to V_4 terminals.
<table>
<tr><th>Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/4Bias</td><td>V5+3/4VLCD</td><td>V5+2/4VLCD</td><td>V5+2/4VLCD</td><td>V5+1/4VLCD</td></tr>
<tr><td>1/5Bias</td><td>V5+4/5VLCD</td><td>V5+3/5VLCD</td><td>V5+2/5VLCD</td><td>V5+1/5VLCD</td></tr>
<tr><td>1/6Bias</td><td>V5+5/6VLCD</td><td>V5+4/6VLCD</td><td>V5+2/6VLCD</td><td>V5+1/6VLCD</td></tr>
<tr><td>1/7Bias</td><td>V5+6/7VLCD</td><td>V5+5/7VLCD</td><td>V5+2/7VLCD</td><td>V5+1/7VLCD</td></tr>
<tr><td>1/8Bias</td><td>V5+7/8VLCD</td><td>V5+6/8VLCD</td><td>V5+2/8VLCD</td><td>V5+1/8VLCD</td></tr>
<tr><td>1/9Bias</td><td>V5+8/9VLCD</td><td>V5+7/9VLCD</td><td>V5+2/9VLCD</td><td>V5+1/9VLCD</td></tr>
<tr><td>1/10Bias</td><td>V5+9/10VLCD</td><td>V5+8/10VLCD</td><td>V5+2/10VLCD</td><td>V5+1/10VLCD</td></tr>
</table>
(V_{LCD}=V_{DD}-V_5)</td></tr>
<tr><td>31,32,
29,30,
27,28,
25,26</td><td>$C1^+$,$C1^-$
$C2^+$,$C2^-$
$C3^+$,$C3^-$
$C4^+$,$C4^-$</td><td>O</td><td>Step up capacitor connecting terminals.
Voltage booster circuit (Maximum 5-time)</td></tr>
<tr><td>24</td><td>V_{OUT}</td><td>O</td><td>Step up voltage output terminal. Connect the step up capacitor between this terminal and V_{SS}.</td></tr>
<tr><td>34</td><td>VR</td><td>I</td><td>Voltage adjust terminal. V_5 level is adjusted by external bleeder resistance connecting between V_{DD} and V_5 terminal.</td></tr>
<tr><td>8,
7</td><td>T_1
T_2</td><td>I</td><td>LCD bias voltage control terminals. (*:Don't Care)
<table>
<tr><th>T_1</th><th>T_2</th><th>Voltage booster Cir.</th><th>Voltage Adj.</th><th>V/F Cir.</th></tr>
<tr><td>L</td><td>*</td><td>Available</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>L</td><td>Not Avail.</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>H</td><td>Not Avail.</td><td>Not Avail.</td><td>Available</td></tr>
</table></td></tr>
<tr><td>15 to 22</td><td>D_0 to
D_7
(SI)
(SCL)</td><td>I/O</td><td>P/S="H" : Tri-state bi-directional Data I/O terminal in 8-bit parallel operation.
P/S="L" : D_7=Serial data input terminal. D_6=Serial data clock signal input terminal. Data from SI is loaded at the rising edge of SCL and latched as the parallel data at 8th rising edge of SCL.</td></tr>
<tr><td>12</td><td>A0</td><td>I</td><td>Connect to the Address bus of MPU. The data on the D_0 to D_7 is distinguished between Display data and Instruction by status of A0.
<table>
<tr><th>A0</th><th>H</th><th>L</th></tr>
<tr><td>Distin.</td><td>Display Data</td><td>Instruction</td></tr>
</table></td></tr>
<tr><td>5</td><td>RES</td><td>I</td><td>Reset terminal. When the RES terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of RES.</td></tr>
<tr><td>11</td><td>CS</td><td>I</td><td>Chip select terminal. Data Input/Output are available during CS ="L".</td></tr>
</table>

<table>
<tr><th>No</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>14</td><td>$\overline{RD}$(E)</td><td>I</td><td><In case of 80 Type MPU>
RD signal of 80 type MPU input terminal. Active "L"
During this signal is "L" , D_0 to D_7 terminals are output.
<In case of 68 Type MPU>
Enable signal of 68 type MPU input terminal. Active "H"</td></tr>
<tr><td>13</td><td>$\overline{WR}$(RW)</td><td>I</td><td><In case of 80 Type MPU>
Connect to the 80 type MPU WR signal. Actie "L".
The data on the data bus input syncronizing the rise edge of this signal.
<In case of 68 Type MPU>
The read/write control signal of 68 type MPU input terminal.
<table>
<tr><td>R/W</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>4</td><td>SEL68</td><td>I</td><td>MPU interface type selection terminal.
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>68 Type</td><td>80 Type</td></tr>
</table></td></tr>
<tr><td>3</td><td>P/S</td><td>I</td><td>serial or parallel interface selection terminal.
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>serial Clock</th></tr>
<tr><td>"H"</td><td>$\overline{CS}$</td><td>A</td><td>D_0 to D_7</td><td>$\overline{RD}$,$\overline{WR}$</td><td>-</td></tr>
<tr><td>"L"</td><td>$\overline{CS}$</td><td>A0</td><td>SI(D_7)</td><td>Write Only</td><td>SCL(D_6)</td></tr>
</table>
RAM data and status read operation do not work in mode of the serial interface.
In case of the serial interface (P/S="L"),$\overline{RD}$ and $\overline{WR}$ must be fixed "H" or "L", and D_0 to D_5 are high impedance.</td></tr>
<tr><td>9,
10</td><td>OSC_1
OSC_2</td><td>I</td><td>System clock input terminal for Maker testing.(This terminal should be Open)
For external clock operation, the clock shoud be input to OSC1 terminal.</td></tr>
<tr><td>45 to 88</td><td>C_0 to C_{43}</td><td>O</td><td rowspan="3">LCD driving signal output terminals.
Segmet output terminals:S_0 to S_{131}
Common output terminals:C_0 to C_{87}

Segment output terminal
The following output voltages are selected by the combination of FR and data in the RAM.(non of the n-line inverse functions)
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal</th><th>Reverse</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
</table>
Common output terminal
The following output voltages are selected by the combination of FR and status of common.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
</table></td></tr>
<tr><td>89 to 220</td><td>S_0 to S_{131}</td><td>O</td></tr>
<tr><td>264 to 221</td><td>C_{44} to C_{87}</td><td>O</td></tr>
</table>

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

While the internal circuits are operating, the busy flag (BF) is "1" and any instruction excepting for the status read are inhibited .

The busy flag goes to “1” from D_7 terminal when status read instruction is executed.

When enough cycle time over than t_{CYC} indicated in “ BUS TIMING CHARACTERISTICS” is ensured, no need to check the busy flag for reduction of the MPU loads.

(1-2)Display Start Line Register

The Display start Line Register is a pointer register which indicates the address in the Display Data RAM corresponding with COM_0(normally it display the top line in the LCD Panel). This register also operates for vertical display scroll, the display page change and so on. The Display Start Line Set instruction sets the display start address of the Display Data RAM represented in 8-bit to this register.

(1-3) Line Counter

The Line Counter generates the line address of display data RAM by the count up operation synchronizing the common cycle after the reset operation at the status change of internal FR signal.

(1-4) Column Address Counter

The column address counter is 8-bit pre-settable counter addressing the column address of display data RAM as shown in Fig. 1. It is incremented (+1) up to $(84)_H$ by the Display Data Read/Write instruction execution. It stops the count up operation at $(84)_H$, and it does not count up non existing address area over than $(84)_H$ by the count lock function. This count lock is released by new column address set.

The column address counter is independent of the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM corresponding to the Segment Driver.

(1-5) Page Register

The page register gives a page address of Display Data RAM as shown in Fig. 1. When the MPU accesses the data with the page change, the page address set instruction is required.

(1-6) Display Data RAM

Display Data RAM is the bit map RAM consisting of 15,840 bits to memorize the display data corresponding to each pixel of LCD panel. The each bit in the Display Data RAM corresponds to the each pixel of the LCD panel and controls the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM outputs 132-bit parallel data in the area addressed by the line counter, and these data are set into the Display Data Latch.

The access operation from MPU to the display data RAM and the data output from the display data RAM are so controlled to operate independently that the data rewriting does not influence with any malfunctions to the display.The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig.1.

(1-7) Common Driver Assignment

The scanning order can be assigned by mask option as shown on Table 1.

Table 1

	COM Outputs Terminals		
PAD No.	45 88		221 264
Pin name	C_0 C_{43}		C_{87} C_{44}
Ver.A	COM_0 → COM_{43}		COM_{87} ← COM_{44}
Ver.B	COM_{87} ← COM_{44}		COM_0 → COM_{43}

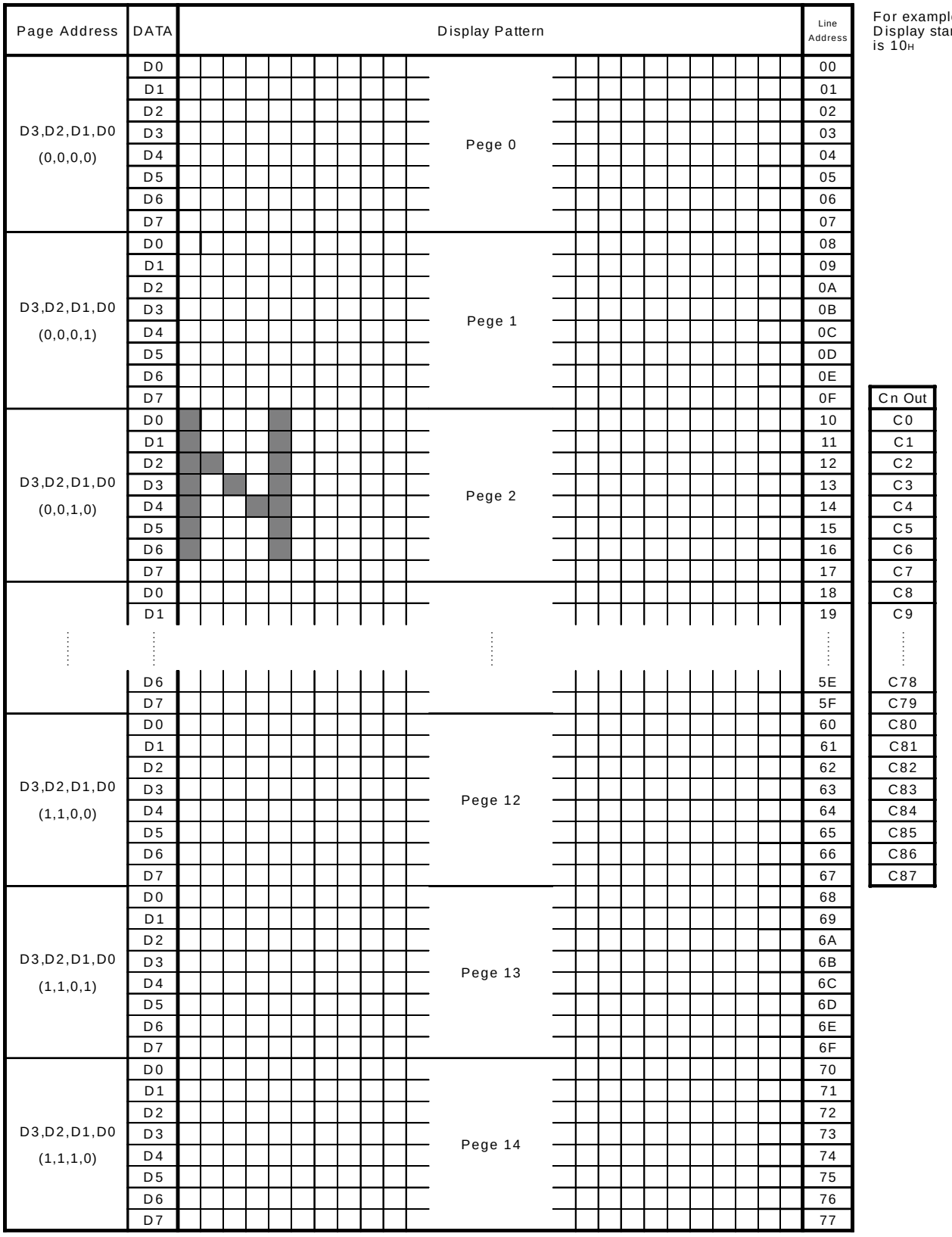


Fig.1 Correspondence with Display Data RAM Address

(1-8) Reset Circuit

Reset circuit operates the following initializations when the condition of $\overline{RES}$ terminal goes to "L" level.

Initialization

1. Display Off
2. Normal Display (Non-inverse display)
3. ADC Select : Normal (ADC Instruction D_0 ="0")
4. Read Modify Write Mode Off
5. Internal Power supply (Voltage Booster) circuits Off
6. Static Drive Off
7. Driver Output Off
8. Clear the serial interface register
9. Set the address$(00)_H$ to the Column Address Counter
10. Set the 1st Line in the Display Start Line Register.page $(00)_H$ to the Page Address Register
11. Set the page "0" to the Page Address Register
12. Set the EVR register to $(FF)_H$
13. Set the All display(1/88 duty)
14. Set the Bias select(1/10 Bias)
15. Set the 5-Time Voltage Booster
16. Set the n line turn over register $(0)_H$

The $\overline{RES}$ terminal should be connected to the Reset terminal of MPU for the initialization at the mean time with MPU as shown in "MPU Interface Example". The period of reset signal requires over than 10us $\overline{RES}$="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of $\overline{RES}$ signal, the operation goes to normal.
When the internal LCD power supply is not used, the external LCD power supply into the NJU6677 must be turned on during $\overline{RES}$ = "L". Although the condition of $\overline{RES}$="L" clear each registers and initialize as above, the oscillation circuit and the output terminal conditions (D_0 to D_7) are not influenced. The initialization must be performed using $\overline{RES}$ terminal at the power on, to prevent hung up or any incorrect operations. The reset Instruction performs the initialization procedures from No.9 to No.16 as shown in above.

Note) The noise into the $\overline{RES}$ terminal should be eliminated to avoid the error on the application with the careful design.

(1-9) LCD Driving

(a) LCD Driving Circuits

LCD driving circuits are consisted of 220 multiplexers which operate as 132 Segment drivers and 88 Common drivers. 88 Common drivers with the shift register scan the common display signal. The combination of the Display data, COM scan signal and FR signal form into the LCD driving output voltage. The output wave form is shown in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 132-bit display data temporarily which is output to LCD driver circuits at a common cycle from Display Data RAM addressed by Line Counter. The instructions of Display On/Off, Display inverse ON/OFF and Static Drive On/Off control only the data in Display Data Latch, therefore, the data in the Display Data RAM is not changed.

(c) Line Counter and Latch signal of Latch Circuits

The clock to Line Counter and latch signal to the Latch Circuits are generated from the internal display clock (CL). The line address of Display Data RAM is renewed synchronizing with display clock(CL). 132 bits display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

Display Timing Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR and LCD alternative signal generate LCD driving waveform of the two frame alternative driving method or n-Line inverse driving method.

(e)Common Timing Generation

The common timing is generated by display clock.

-Waveform of Display Timing(without the n-line inverse function, the line inverse register in set to 0)

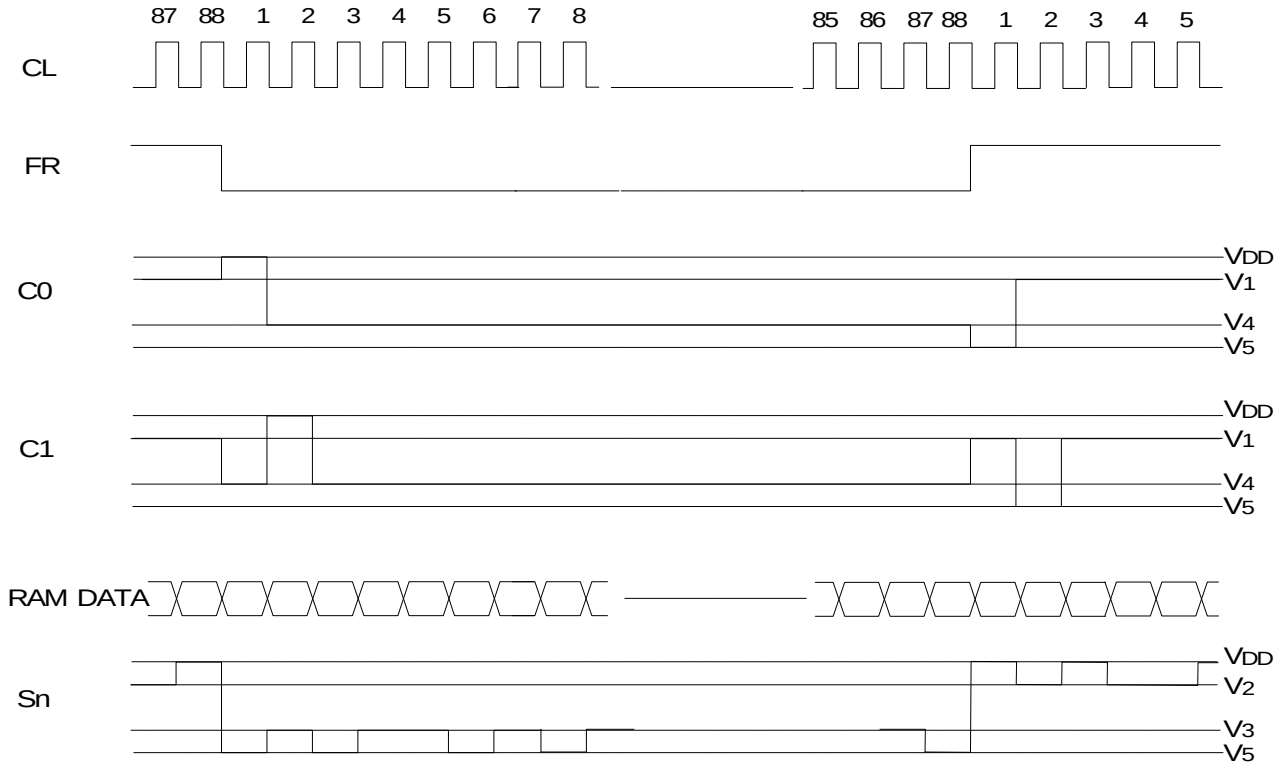


Fig.2

-Waveform of Display Timing(with the n-line inverse function, n=7, the line inverse register in set to 6)

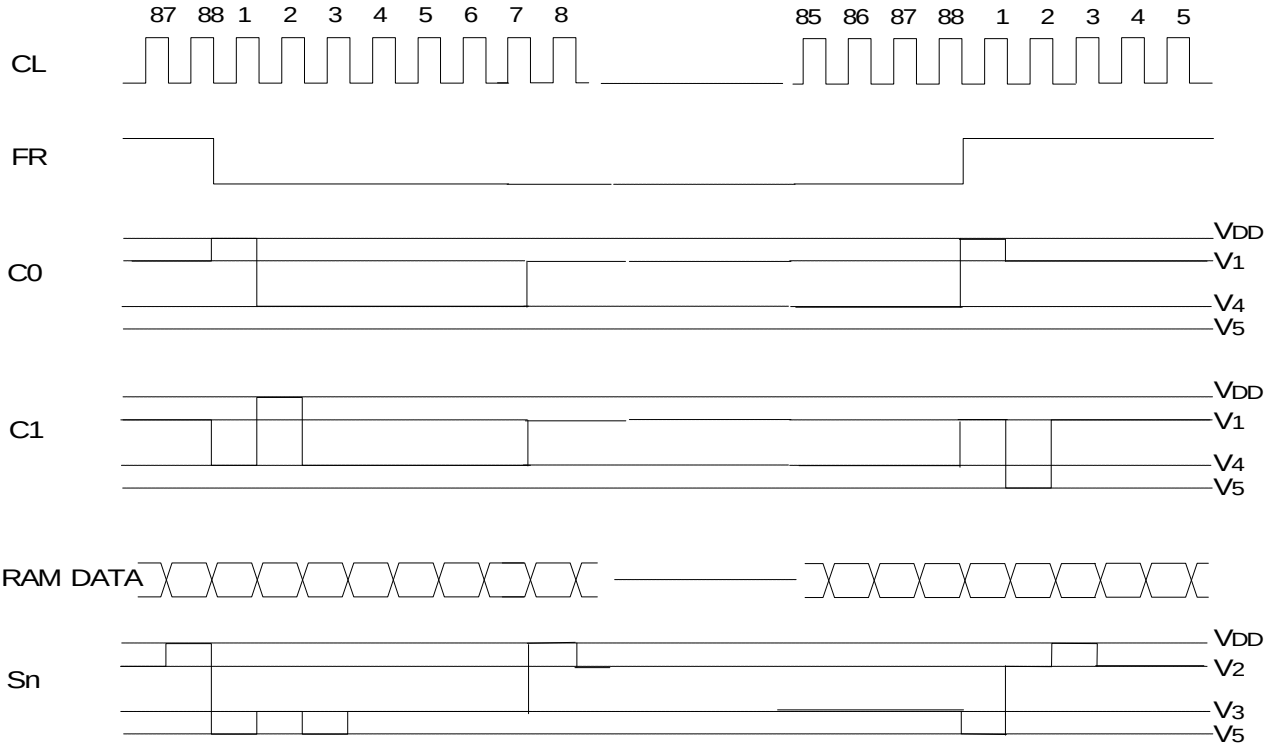


Fig.3

(f) Oscillation Circuit

The Oscillation Circuit is a low power CR oscillator incorporating with Resistor and Capacitor. It generates clocks for display timing signal source and voltage booster circuits. The oscillation circuit output frequency is divided as shown in below for display clock CL.

-The relation between duty and divide

Duty	1/8	1/16	1/24	1/32	1/40	1/48	1/56,64	1/72	1/80,88
Divide	1/44	1/22	1/15	1/11	1/9	1/7	1/6	1/5	1/4

(g) Power Supply Circuit

Internal Power Supply Circuit generate the High voltage and Bias voltage for the LCD. The power Supply Circuit consists of Voltage Booster (5-Time maximum) Circuits, Regulator Circuits, and Voltage Followers. The internal Power Supply is designed for small size LCD panel, therefore it is not suitable for the large size LCD panel application. If the contrast is not good in the large size LCD panel application, please supply the external.

The suitable values of the capacitors connecting to the V_1 to V_5 terminals and the voltage booster circuit, and the feedback resistors for V_5 operational amplifier depend on the LCD panel. And the power consumption with the LCD panel is depending on the display pattern. Please evaluate with actual LCD module.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the voltage booster circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD should be supplied from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$, $C4^+$, $C4^-$ and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminal. Furthermore the external power supply operates with some of internal power supply function.

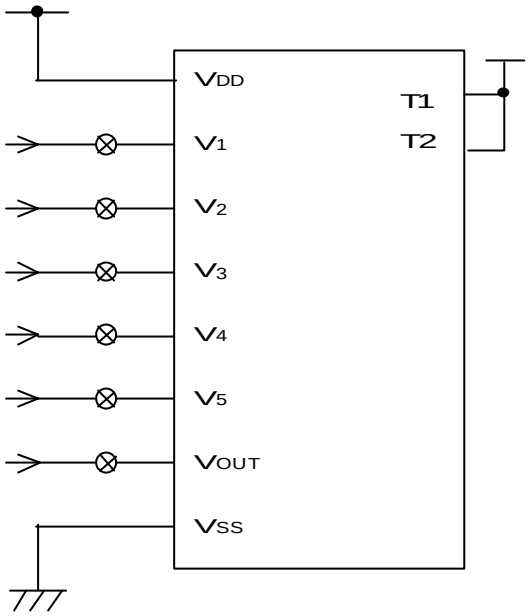
T_1	T_2	Voltage Booster	Voltage Adj.	Buffer(V/F)	Ext.Pow Supply	$C1^+$,$C1^-$ to $C4^+$,$C4^-$	VR Term.
L	L/H	ON	ON	ON	-		
H	L	OFF	ON	ON	V_{OUT}	Open	
H	H	OFF	OFF	ON	V_5,V_{OUT}	Open	Open

When (T_1, T_2)=(H, L), $C1^+$, $C1^-$, $C2^+$, $C2^-$,$C3^+$, $C3^-$, $C4^+$, $C4^-$ terminals for voltage booster circuits are open because the voltage booster circuits doesn't operate. Therefore LCD driving voltage to the V_{OUT} terminal should be supplied from outside.

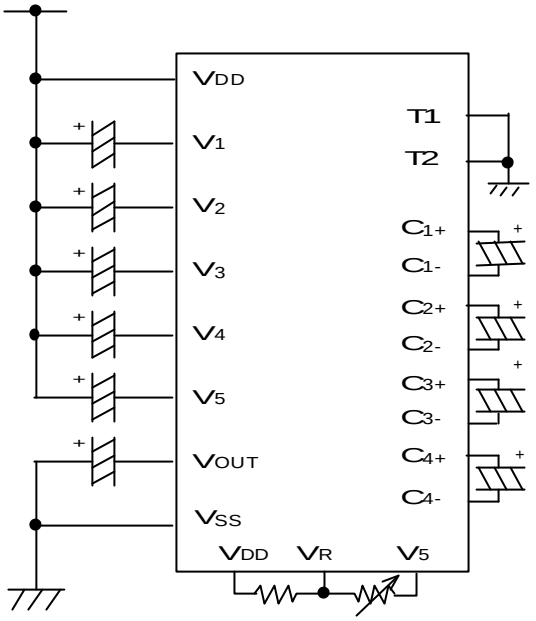
When (T_1, T_2)=(H, H), terminals for voltage booster circuits and VR are open, because the voltage booster circuits and Voltage adjust circuits do not operate.

○Power Supply applications

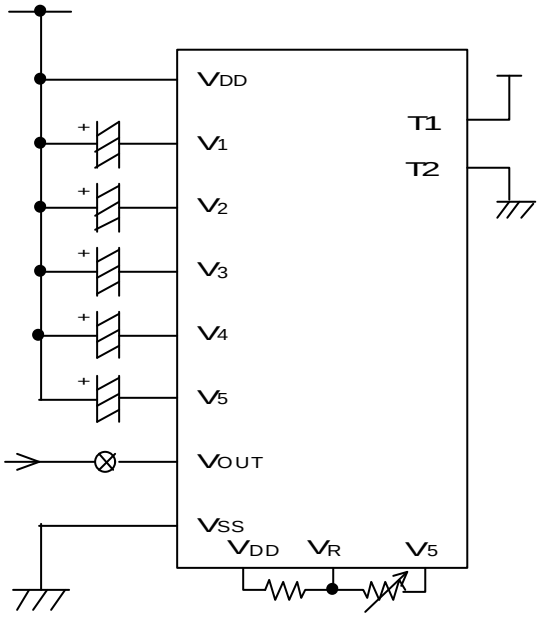
(1)External power supply operation.



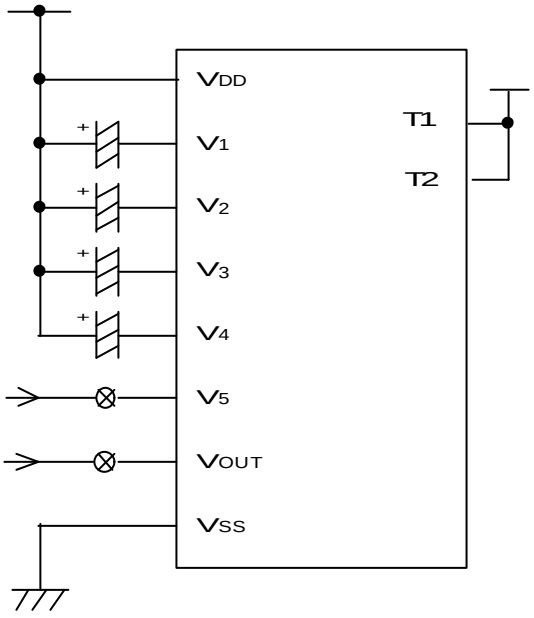
(2)Internal power supply operation.
(Voltage Booster, Voltage Adj., Buffer(V/F))
Internal power supply ON (instruction) (T1,T2)=(L,L)



(3)External power supply operation with
Voltage Adjustment,3 Buffer(V/F)
Internal power supply ON (Instruction) (T1,T2) = (H,L)



(4)External power supply operation adjusted
Voltage to V5.
Internal power supply (Instruction) (T1,T2) =(H,H)



⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6677 distinguishes the signal on the data bus by combination of A0, $\overline{RD}$ and $\overline{WR}$. The decode of the instruction and execution performs depending on the internal timing only neither the external clock. In case of serial interface, the data input as MSB first serially.

The Table. 4 shows the instruction codes of the NJU6677.

Table 4. Instruction Code (*:Don't Care)

Instruction		Code												Description
		A0	RD	W-R	D7	D6	D5	D4	D3	D2	D1	D0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1		LCD Display ON/OFF 0:OFF 1:ON
(2)	Display Start Line Set High Order 4bits	0	1	0	0	1	0	1	High Order Address					Determine the Display Line of RAM to the COM0. (Set the Higher order 4bits)
	Display Start Line Set Lower Order 4bits	0	1	0	0	1	1	0	Lower Order Address					Determine the Display Line of RAM to the COM0. (Set the Lower order 4bits)
(3)	Page Address Set 4bits	0	1	0	1	1	0	0	Page Address					Set the 4 bit page of DD RAM to the Page Address Register
(4)	Column Address Set High Order 4bits	0	1	0	0	0	0	1	High Order Column Add.					Set the Higher order 4 bits Column Address to the Reg.
	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Add.					Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status				0	0	0	0		Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data									Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data									Read the data from the Display Data RAM
(8)	Normal or Inverse of ON/OFF Set	0	1	0	1	0	1	0	0	1	1	0/1		Inverse the ON and OFF Display 0:Normal 1:Inverse
(9)	Whole Display ON /Normal Display	0	1	0	1	0	1	0	0	1	0	0/1		Whole Display Turns ON 0:Normal 1:Whole Disp. ON
(10)	Sub instruction table mode	0	1	0	0	1	1	1	0	0	0	0		Set the Sub instruction table.
(11)	Partial Display													
	1st Block, Set Start display unit	0	1	0	0	0	0	0	Start display unit					Set the Start display unit of 1st Block.
	1st Block, Set The number of display units	0	1	0	0	0	0	1	number of display units					Set the number of display units of 1st Block.
	2nd Block, Set Start display unit	0	1	0	0	0	1	0	Start display unit					Set the Start display unit of 2nd Block.
	2nd Block, Set The number of display units	0	1	0	0	0	1	1	number of display units					Set the number of display units of 2nd Block.
	Partial display on	0	1	0	0	1	0	0	0	0	0	0		It comes off the mode to set and a display is executed.
(12)	n-line Inverse Drive Set													
	Register Set Higher order 2 bits	0	1	0	0	1	0	1	*	*	higher order			Set the number of inverse drive line.
	Register Set Lower order 4 bits	0	1	0	0	1	1	0	Lower order					Set the number of inverse drive line.
	n-line Inverse Drive Set is executed.	0	1	0	0	1	1	1	0	0	0	0		The execution of the line inverse drive.
(13)	EVR Register Set													
	EVR Register Set Higher order 4 bits	0	1	0	1	0	0	0	EVR Data Higher order					Set the V_5 output level to the EVR register. (Higher order 4 bits)
	EVR Register Set Lower order 4 bits	0	1	0	1	0	0	1	EVR Data Lower order					Set the V_5 output level to the EVR register. (Lower order 4 bits)
	EVR Register Set is executed.	0	1	0	1	0	1	0	0	0	0	0		The execution of the EVR.
(14)	End of sub instruction table mode	0	1	0	0	1	1	1	0	0	0	1		It ends the setting of sub instruction table.

(*:Don't Care)

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(15)	Bias Select	0	1	0	1	0	1	1	*	Bias			Select the bias (7 Patterns)
(16)	Voltage Booster Circuits Multiple Select	0	1	0	0	0	1	1	0	0	Boost Multiple		Set the Booster circuits (2 to 5 times)
(17)	Read Modify Write /End	0	1	0	1	1	1	0	0	0	0	0 1	Read Modify Write mode D0=0:On D0=1:End
(18)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(19)	Internal Power Supply ON/OFF	0	1	0	0	0	1	0	0	0	0	0 1	0:Int. Power Supply OFF 1:Int. Power Supply ON
(20)	LCD Driving Voltage Set	0	1	0	0	0	1	0	0	0	1	0 1	Set LCD Driving Voltage after the internal (external) power supply is turned on
(21)	Power Save (Dual Command)												Set the Power Save Mode (LCD Display OFF +Whole Display Turns ON)
(22)	ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment D0=0:Normal D0=1:Inverse

(3) Explanation of Instruction Code

(3-1) Display On/Off

This instruction executes whole display On/Off without relationship of the data in the Display Data RAM and internal conditions.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D 0:Display Off

1:Display On

(3-2) Display Start Line

This instruction sets the line address of Display Data RAM corresponding the COM0 terminal (the highest position line of display in normal application). The display area is fixed automatically by number of display line which corresponds the display duty ratio from the pointed line address as the start line. This instruction realizes the vertical smooth scroll with extra display RAM or the page address change by dynamic line addressing. In this time, the contents of RAM are not changed.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	A7	A6	A5	A4
0	1	0	0	1	1	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line Address(HEX)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
			:					:
			:					:
0	1	1	1	0	1	1	1	77

(3-3) Page Address Set

When MPU accesses the Display Data RAM, the page address must be selected before the data writing. The access to the Display Data RAM is available by the page and column address set (Refer the Fig. 1). The page address change does not influence with the display.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	A2	A1	A0

(*:Don't Care)

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
		:		:
		:		:
1	1	1	0	14

(3-4) Column Address

When MPU accesses the Display Data RAM, the page address (refer(3-3)) and column address set are required before the data writing. The column address set requires twice address set which are higher order 4 bits address set and lower order 4 bits. When the MPU accesses the Display Data RAM sequentially, the column address is increase one by one automatically, therefore, the MPU can access only the data sequentially without address set.

After writing 1page data, page address setting is required due to page address doesn't increase automatically. The increment of the column address is stopped at the address of $(83)_H$ automatically, and the page address is not changed even if the column address increase to $(83)_H$ and stop. In this time the page address is not changed.

A0	$\overline{RD}$	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	0	0	1	A_7	A_6	A_5	A_4	Higher Order
0	1	0	0	0	0	0	A_3	A_2	A_1	A_0	Lower Order

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address(HEX)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
				:				:
1	0	0	0	0	0	1	1	83

(3-5) Status Read

This instruction reads out the internal status of "BUSY", “ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column (segment) address and segment driver.
0 :Counterclockwise Output (Inverse) Column Address 131-n <---> Segment Driver n
1 :Clockwise Output (Normal) Column Address n <---> Segment Driver n
(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initializing by $\overline{RES}$ signal or reset instruction.
0 : -
1 : Initialization Period

(3-6) Write Display Data

This instruction writes the 8-bit data on the data bus into the Display Data RAM. The column address increases "1" automatically after data writing, therefore, the MPU can write the 8-bit data into the Display Data RAM continuously without any address setting after the start address setting.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	WRITE DATA							

(3-7) Read Display Data

This instruction reads out the 8-bit data from Display Data RAM addressed by the column and page address. The column address increase "1" automatically after data reading out, therefore, the MPU can read out the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read must operate after column address set as the explanation in "(5-4) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data is not read out.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	READ DATA							

(3-8) Normal or Inverse On/Off Set

This instruction changes the condition of display turn on and off as normal or inverse. The contents of Display Data RAM is not changed by this instruction execution.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

D 0 : Normal RAM data "1" correspond to "On"

1 : Inverse RAM data "0" correspond to "On"

(3-9) Whole Display On

This instruction turns on the all pixels indipendent of the contents of Display Data RAM. In this time, the contents of Display Data RAM is not changed and kept. This instruction takes precedence over the "Normal or Inverse On/Off Set Instruction".

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

D 0 : Normal Display

1 : Whole Display turn on

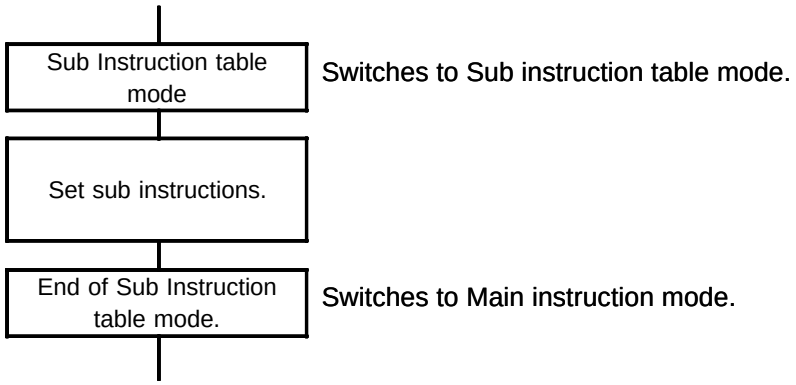
When Whole Display On Instruction is executed in the Display Off status, the internal circuits go to the power save mode (refer to the (s) Power Save).

(3-10) Sub Instruction table mode

This instruction switches the instruction table from the main to the sub. The sub instruction table contains instructions of partial display, n-line inverse drive set and EVR register set as mentioned in (11), (12) and (13). The instruction of sub instruction table mode must be executed before above 3 sub instructions execution. The instruction of end of sub instruction table mode (14) switches the instruction table from the sub to the main. If any main instructions are written in the sub instruction mode, the NJU6677 will malfunction.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	0

-Set sub Instruction table flow is shown below:



(3-11) Partial Display

This instruction divides the active display area in a LCD panel to 11 units consisting of 8 commons per unit and displays one or two blocks of active display area consisting of a unit or more. In the partial display mode, the display duty ratio is set automatically according to the number of unit in a block or two.
Therefore, the partial display function realizes to go down the LCD driving voltage according to the display duty ratio. As a result, the operation current of display system is much saved against the full display mode.

The display units

	UNIT	0	(8 commons)
	UNIT	1	
	UNIT	2	
	UNIT	3	
	UNIT	4	
	UNIT	5	
	UNIT	6	
	UNIT	7	
	UNIT	8	
	UNIT	9	
	UNIT	10	(8 commons)

88-common

132-segment

Partial display instruction

The partial display operates by the conbination of instructions which area unit number of start position start unit block in the display area and a number of display unit from start position to end as a block. The number of block is set up to two.

	A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
1st Block	0	1	0	0	0	0	0	D	D	D	D	Start display unit
	0	1	0	0	0	0	1	D	D	D	D	The number of display units
2nd Block	0	1	0	0	0	1	0	D	D	D	D	Start display unit
	0	1	0	0	0	1	1	D	D	D	D	The number of display units

After execution of the next instruction, the display mode is changed to the partial display and the duty is changed automatically.

0	1	0	0	1	0	0	0	0	0	0	Partial display on

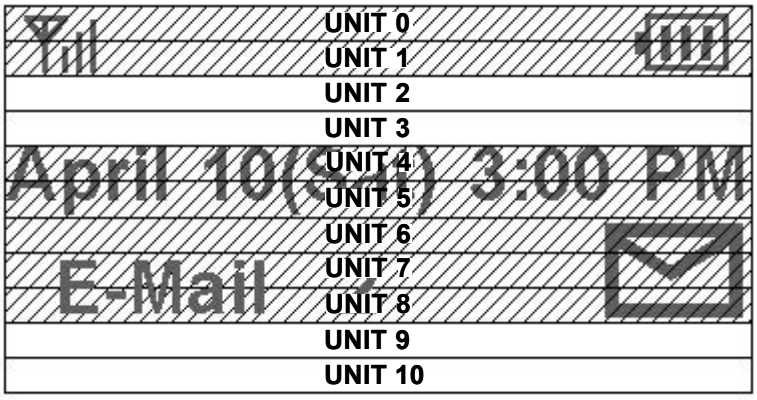
D :unit number (Hex.)

Note) Incase of full display (1/88 duty), all of units on the display are selected when the first start unit is set to “0” (0,0,0,0) and the second number of display unit is set to “11” (1,0,1,1). In this time, the second block settings are ignored.

In case of only one block display, the second block settings are ignored when the second start unit is set to “0” (0,0,0,0) and the second display unit number is set to “0” (0,0,0,0).

Keep the order of partial display instruction sequence.
Do not set over “UNIT 10” the display data in DD RAM are assigned continuously from page 0 for all of display block, even if non-display area is existed between the first block and the second.

The example of partial display setting



The above partial display condition is set as follows:

1)Set sub instruction mode

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set partial display conditions

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	0	0	0	0	0	1st Block, Set start display unit to ”0”
0	1	0	0	0	0	1	0	0	1	0	1st Block, Set the number of display units to ”2”
0	1	0	0	0	1	0	0	1	0	0	2nd Block, Set start display unit to ”4”
0	1	0	0	0	1	1	0	1	0	1	2nd Block, Set the number of display units to ”5”
0	1	0	0	1	0	0	0	0	0	0	Partial display on.

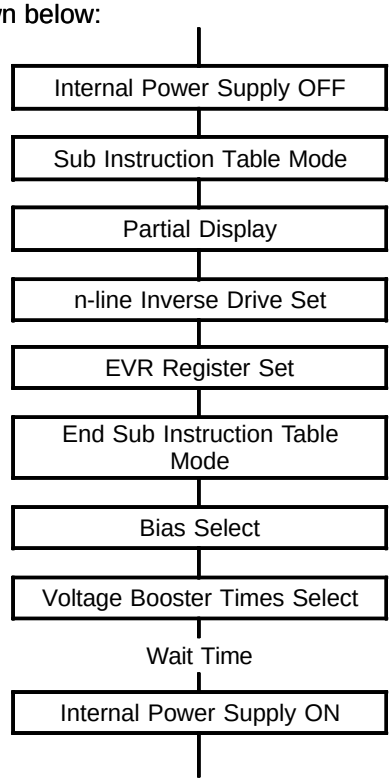
In this case, 1/56 duty. (Duty=1/(number of display units x 8))

3)End sub instruction mode

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

Although the partial display instruction changes duty cycle ratio automatically and display area, LCD driving voltage, Bias and others are not changed. Therefore, the instruction of LCD driving voltage “OFF” (D=0) must be set before partial display operation, and the other instructions such as the n-line inverse drive set, EVR register set, bias select and voltage booster select should be set for optimum display-contrast. The “End of sub instruction mode” is required before these instructions in order to prevent momentary flickering.

-Set Partial Display flow is shown below:



(3-12) n-line Inverse Drive Mode

This instruction sets a line number for inversion of LCD driving signal levels between “1” and “0”. It reduces the stripe shadow(crosstalk) and stabilizes display quality. The n-line inverse number is set according to the result of actual LCD panel display.

The instructions must be input in order of followings. These instructions are sub instruction sets and must be set after (3-10)Sub instruction table mode.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	0	1	*	*	A5	A4	Higher order
0	1	0	0	1	1	0	A3	A2	A1	A0	Low order

(*:Don't Care)

A5	A4	A3	A2	A1	A0	Inverse line
0	0	0	0	0	0	-
0	0	0	0	0	1	2
			:			:
			:			:
1	1	1	1	1	1	64

The actual operation starts after following instruction.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	0

(3-13) EVR Register Set

This instruction controls voltage adjustment circuits of internal LCD power supply and changes LCD driving voltage “V5”. Finally, it adjusts the contrast of LCD display. By setting a data into EVR register, V5 output voltage selects one condition out of 201-voltage conditions. The range of V_5 voltage is adjusted by setting external resistors as mentioned in "(4)(b) Voltage Adjust Circuits".

This instruction is sub instruction and it must be set after (3-10) Sub instruction table mode.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	A7	A6	A5	A4
0	1	0	1	0	0	1	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	VLCD
0	0	1	1	0	1	1	1	Low
				:				:
				:				:
1	1	1	1	1	1	1	1	High

$V_{LCD}=V_{DD}-V_5$

When EVR doesn't use, set the EVR register to (1,1,1,1,1,1,1,1).

The actual operation starts after following instruction.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0

(3-14) End of Sub instruction table mode

"End of sub instruction table mode" instruction switches instruction table from sub to main.

(11)Partial display, (12)n-line inverse drive mode, and (13)EVR are sub instruction sets on the sub instruction table. The instruction of “END of sub instruction mode” must be set after these sub instruction sets. The NJU6677 may occur in-correct operation if any main instructions on the main instruction table are input in mode of sub instruction table.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	1

(3-15) Bias Select

This instruction decides the value of LCD driving voltage bias ratio.

Especially, the bias should be selected for display quality in partial mode.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	*	A2	A1	A0	(*:Don't Care)

A2	A1	A0	Bias
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	*	1/10

(3-16) Voltage Booster Circuit Multiple Select

This instruction Selects a voltage boost time.

The multiple must be selected the voltage boost times according to the maximum boost times by the external capacitors connections or less. Especially, the multiple should be selected for display quality and saving operation current in partial display mode.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	0	A1	A0

Command		Booster Multiple			
A1	A0	5times external capacitors connections	4times external capacitors connections	3times external capacitors connections	2times external capacitors connections
0	0	2-time			
0	1	3-time	2-time		
1	0	4-time	3-time	2-time	
1	1	5-time	4-time	3-time	2-time

(3-17) Read Modify Write/End

This instruction sets the Read Modify Write Mode for the column address increment control. In mode of the Read Modify Write, the column address increases "1" automatically when the Display Data Write Instruction is executed, but the address does not change when the Display Data Read Instruction is executed. This status is continued until End instruction execution. When the End instruction (D=1) is input, the column address goes back to the start address before the Read Modify Write instruction input. This function reduces the load of MPU for repeating the display data change in the fixed area (ex. cursor blink).

D=”1” to release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

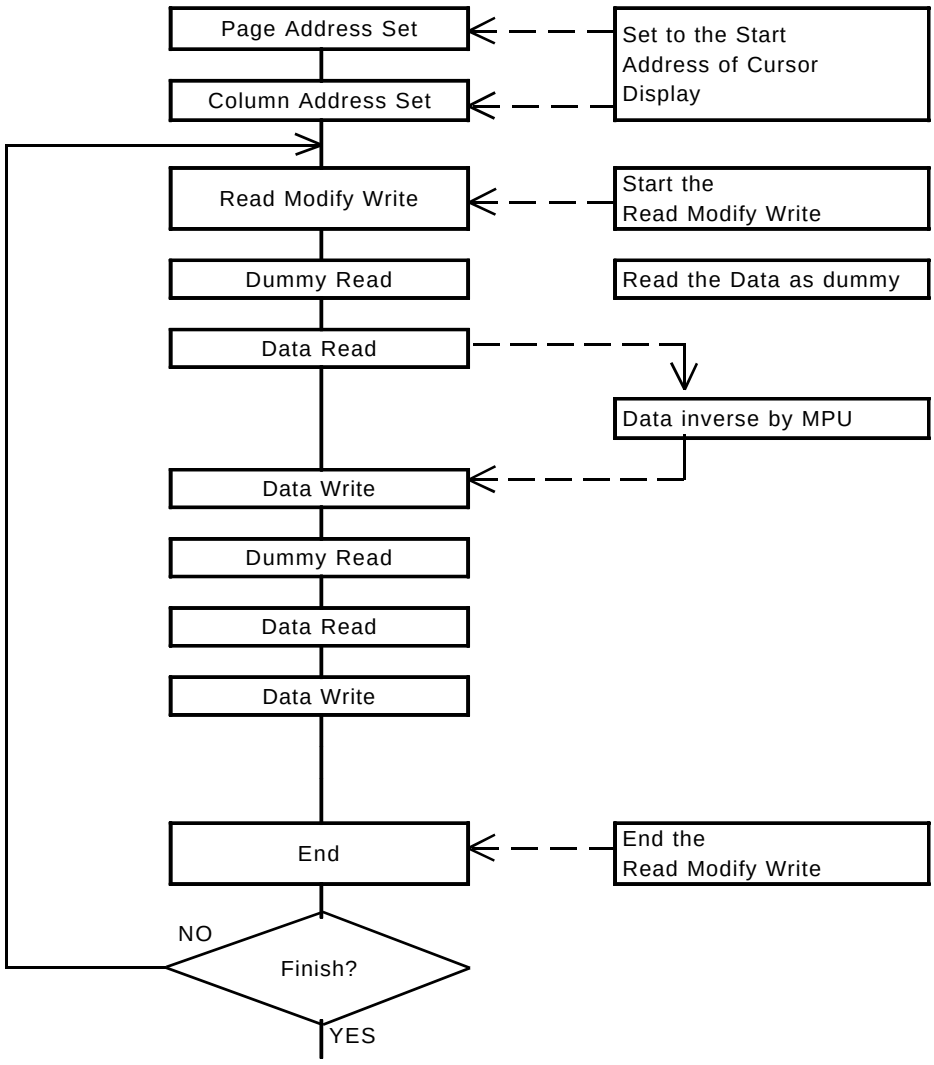
A0	$\overline{RD}$	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	1	1	0	0	0	0	D

D 0 : Read Modify Write On

1 : End

Note) In mode of the Read Modify Write, any instructions except for Column Address Set can execute.

- Sequence of cursor blink display



(3-18) Reset

This instruction executes the following initialization.

Initialization

(1) Set the Address (00)H into the Column Address Counter.
(2) Set the Address (00)H into the Display Start Line Register.
(3) Set the page "0" into the Page Address Register.
(4) Set 0 to the EVR Register to (FF)H.
(5) Set the All display(1/88 duty)
(6) Set the Bias select(1/10 Bias)
(7) Set the 5-Time Voltage Booster.
(8) Set the n-line inverse register (0)H

In this time, the Display Data RAM is not influenced.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal (hardware reset) must be input for the power on initialization. Reset instruction does not perform completely in stead of hardware reset using the $\overline{RES}$ terminal.

(3-19) Internal Power Supply ON/OFF

This instruction set the condition of internal Power Supply On/Off. Voltage Booster circuits, Voltage Regulator and Voltage Follower operate at On. To operate the voltage booster circuits, the oscillation circuits must be operating.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	D

D 0 : Internal Power Supply Off
1 : Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

*1 The set up period of internal power supply On depends on the step up capacitors, voltage stabilizer capacitors, VDD and VLCD.
Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the (4)(d) Fig.4)

(3-20) LCD Driving Voltage Set

This instruction controls LCD driving waveform output through the COM/SEG terminals.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	1	D

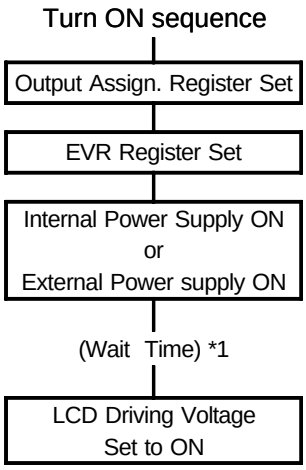
D 0 : LCD driving waveform output Off

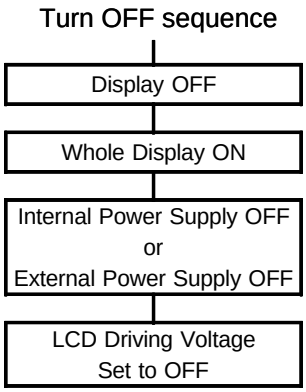
1 : LCD driving waveform output On

The NJU6677 contains low power LCD driving voltage generator circuit reducing own operation current. Therefore, it requires the following sequence procedures at power on for the power source stabilized operation.

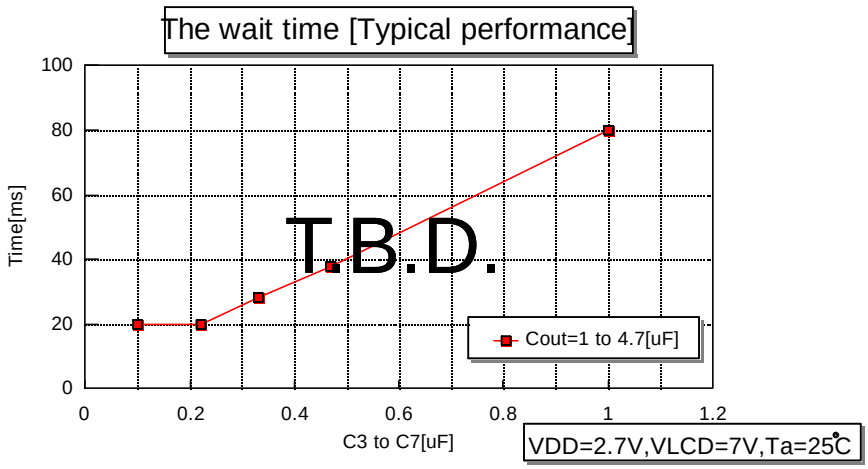
- LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is turned On/Off.
When the power supply is turned on again after the turn off (by the power save instruction), the power save release sequence ((3-21) Power Save) is required.





*1 The wait time depends on the C_1 to C_9, C_{OUT} capacitors (refer (4) (d)Fig.4), V_{DD} and V_{LCD} voltage. Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the following graph.)



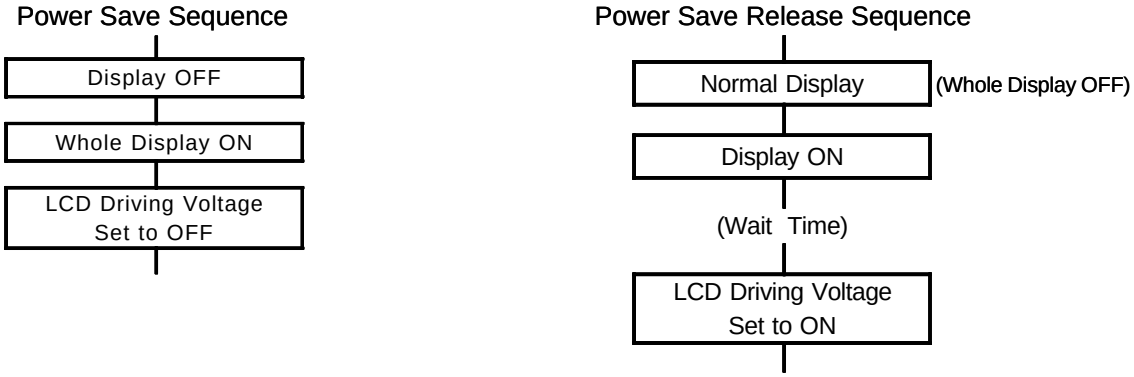
(3-21) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits go to the power save mode and the operating current is reduced as some as the stand by current.

The internal status in the Power Save Mode is shown in follows;

(1) Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
(2) Stop the LCD driving. Segment and Common drivers output V_{DD} level.
(3) Keep the display data and operating mode just before the power save mode.
(4) All of LCD driving bias voltage fix to the V_{DD} level.

The power save and its release perform according to the following sequences.



*1 In the power save sequence, the power save mode is started after the second instruction "whole Display ON".

*2 In the power save release sequence, the power save mode is released after the Normal Display instruction (Whole display OFF).
The instruction of display ON is input at any timing after the instruction of normal display in power save release sequence.

*3 Until "LCD driving voltage set to ON" execution, NJU6677 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously.

*4 In case of the external power supply for LCD driving, it should be turned off and made condition like as unconnection or connected to V_{DD} before the power save mode or at the same time. In this time, V_{OUT} terminal should be made condition like as disconnection or connected to the lowest voltage of the system (V_5 level from the external power supply).

(3-22) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

A0	$\overline{RD}$	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	0	0	D

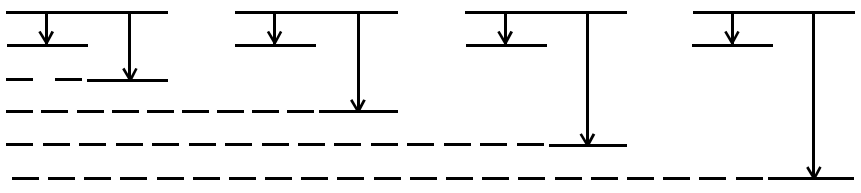
D 0 : Clockwise Output (Normal)
1 : Counterclockwise Output (Inverse)

(4) Internal Power Supply

(a) 5-time voltage booster circuits

5-time voltage booster circuits connecting five capacitors between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, $C3^+$ and $C3^-$, $C4^+$ and $C4^-$, V_{SS} and V_{OUT} boost the voltage of V_{DD} - V_{SS} to negative voltage (V_{DD} Common) and output the boosted voltage from the V_{OUT} terminal. It selects one of boost time from 2 to 5 times by external capacitors connection. Furthermore, it also selects one of boost time by "Voltage Booster circuits multiple select" instruction. The boost voltage and the voltage booster circuits are shown in below. Voltage Booster circuits requires the clock signals from internal oscillation circuit, therefore, the oscillation circuits must be operating when voltage boost operation. The boost voltage times are shown in below. When 5-time voltage boost operation, the operation voltage of V_{DD}-V_{OUT} should be less than 18V.

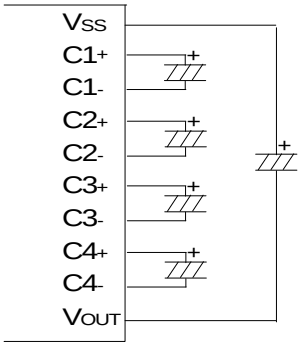
V_{DD}=+3V
V_{SS}=±0V
V_{OUT}=-V_{DD}=-3V
V_{OUT}=-2V_{DD}=-6V
V_{OUT}=-3V_{DD}=-9V
V_{OUT}=-4V_{DD}=-12V



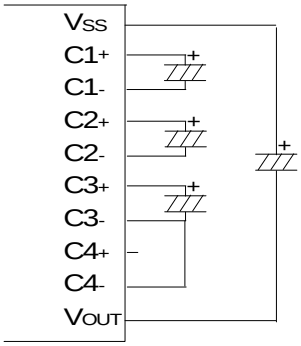
2-time voltage 3-time voltage 4-time voltage 5-time voltage

● Examples for connecting the capacitors

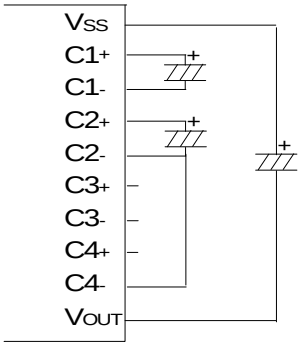
5-time voltage



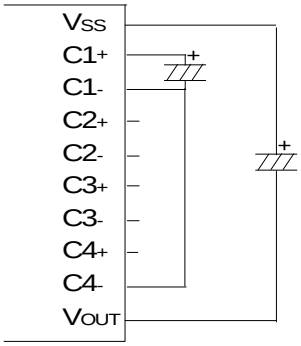
4-time voltage



3-time voltage



2-time voltage



(b)Voltage Adjust Circuits

The boosted voltage of V_{OUT} output from V_5 through the voltage adjust circuits for LCD driving. The output voltage of V_5 is adjusted by changing the Ra and Rb within the range of $|V_5| < |V_{OUT}|$. The output voltage is calculated by the following formula.

$$V_{LCD} = V_{DD}-V_5 = (1+Rb/Ra)V_{REG} \quad (1)$$

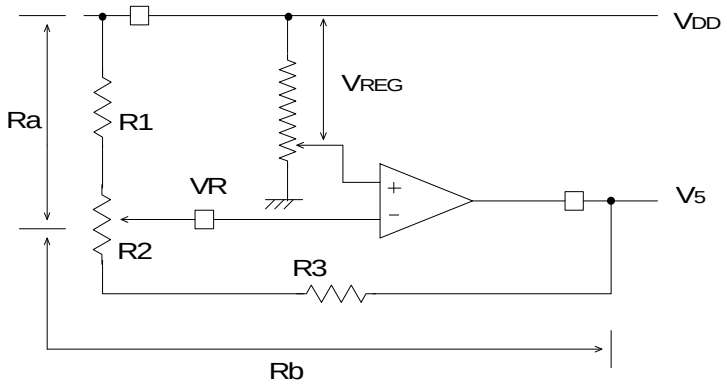


Fig. 3

The voltage of V_{REG} is a standard voltage produced from built-in bleeder resistance. V_{REG} is possible to be fine-adjusted by EVR functions mentioned in (c).
For fine-adjustment of V5, R2 as variable resistor, R1 and R3 as fixed constant should be connected to V_{DD} terminal, VR and V_5, as shown in Fig.3.

[Design example for R1, R2 and R3 / Reference]

- R1+R2+R3=5MΩ(Determined by the current flown between V_{DD}-V_5)
- Variable voltage range by the R2. -6V to -7.5V ($V_{LCD}=V_{DD}-V_5$ --> 9.0V to 10.5V)
  (Determined by the LCD electrical characteristics)
- V_{REG}=3V(In case of EVR=(FF)$_H$)
- R1, R2 and R3 are calculated by above conditions and the formula of (1) to below;
  R1=2.0MΩ, R2=0.5MΩ, R3=2.5MΩ

* If the power supply voltage between V_{DD} and V_{SS} changes, V_5 changes too. Therefore the power supply voltage should be stabilized for V_5 stable operation.

(c) Contrast Adjustment by the EVR function

The EVR controls voltage of V_{REG} by instruction and changes voltage of V_5.

As result, LCD display contrast is adjusted by V_5. The EVR selects a voltage of V_{REG} in the following 201 conditions by setting 6bits data into the EVR register.

In case of EVR operation, T_1 terminal and T_2 require to set couples of value as (L,L),(L,H) and (H,L) excepting for (H,H) and the internal power supply must turn on by instruction.

(37)H to (4F)H available for use. If keeping 3% precision set EVR over (4F)H.

EVR register		V_{REG}[V]	V_{LCD}
:	:	:	Low
:	:	:	:
(4F)H	(0,1,0,0,1,1,1,1)	(124/300) x (V_{DD}-V_{SS})	:
:	:	:	:
:	:	:	:
(FD)H	(1,1,1,1,1,1,0,1)	(298/300) x (V_{DD}-V_{SS})	:
(FE)H	(1,1,1,1,1,1,1,0)	(299/300) x (V_{DD}-V_{SS})	:
(FF)H	(1,1,1,1,1,1,1,1)	(300/300) x (V_{DD}-V_{SS})	High

● Adjustable range of the LCD driving voltage by EVR function

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors Ra and Rb.

[Design example for the adjustable range / Reference]

- Condition V_{DD}=3.0V, V_{SS}=0V

Ra=1MΩ, Rb=4MΩ (Ra:Rb=1:4)

The adjustable range and the step voltage are calculated as follows in the above condition.

In case of setting (4F)H in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra)V_{REG}

= (5/1) x [(100/300) x 3.0]

= 6.2V

In case of setting (FF)H in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra)V_{REG}

= (5/1) x [(300/300) x 3.0]

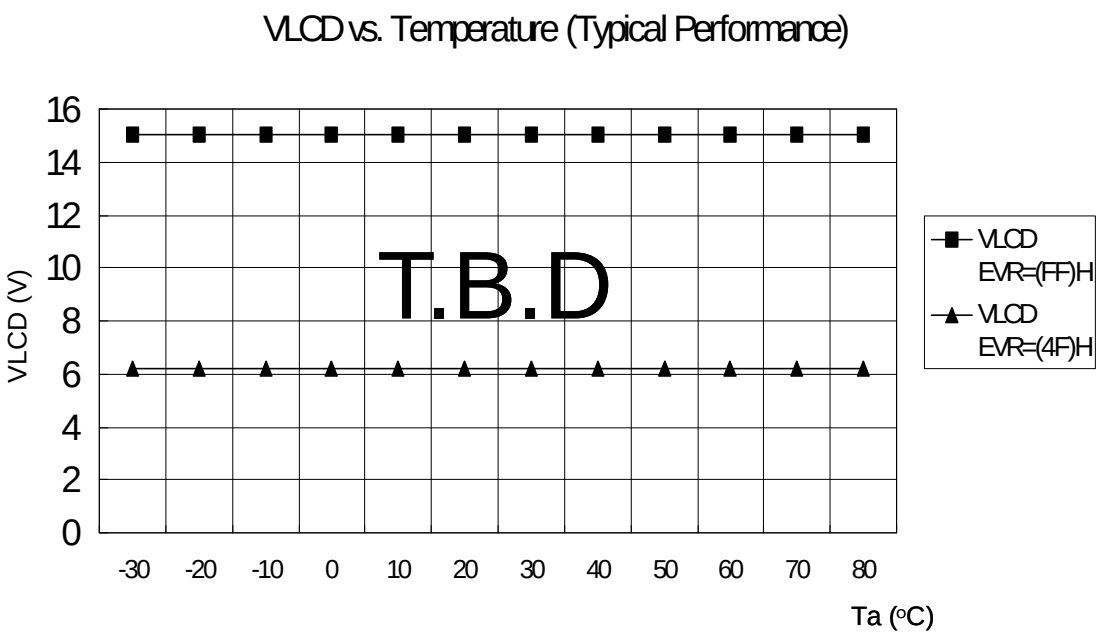
= 15.0V

	Min.(4F)H		Max.(FF)H
Adjustable Range	6.2	- - - - - - - - - - - - - - - - - -	15.0 [V]
Step Voltagre		50	[mV]

* In case of V_{DD}=3V

*) The V_{LCD} operating temperature. Please refer to the following graphs.

(conditions) V_{DD} = 3V
Ra=1MΩ, Rb=4MΩ (Ra:Rb = 1:4)
Five times voltage

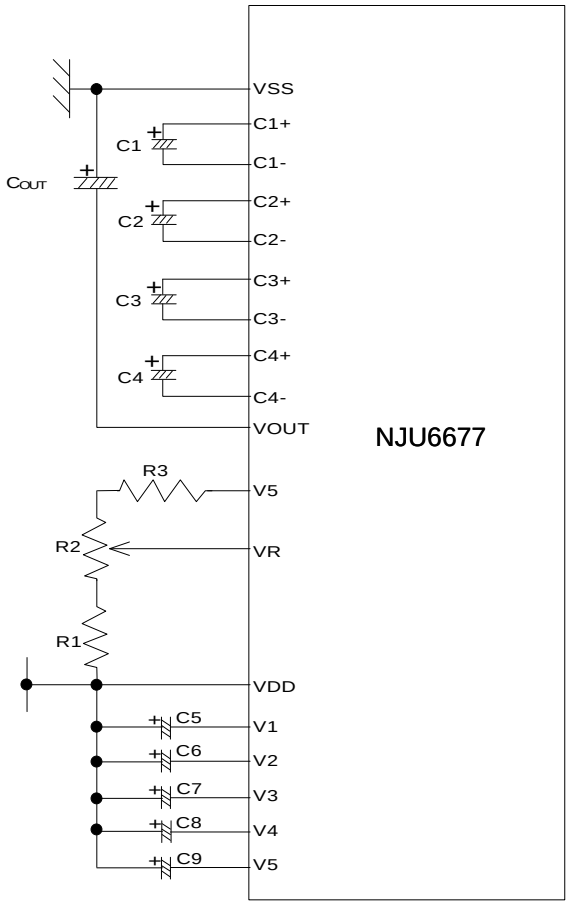


(d) LCD Driving Voltage Generation Circuits

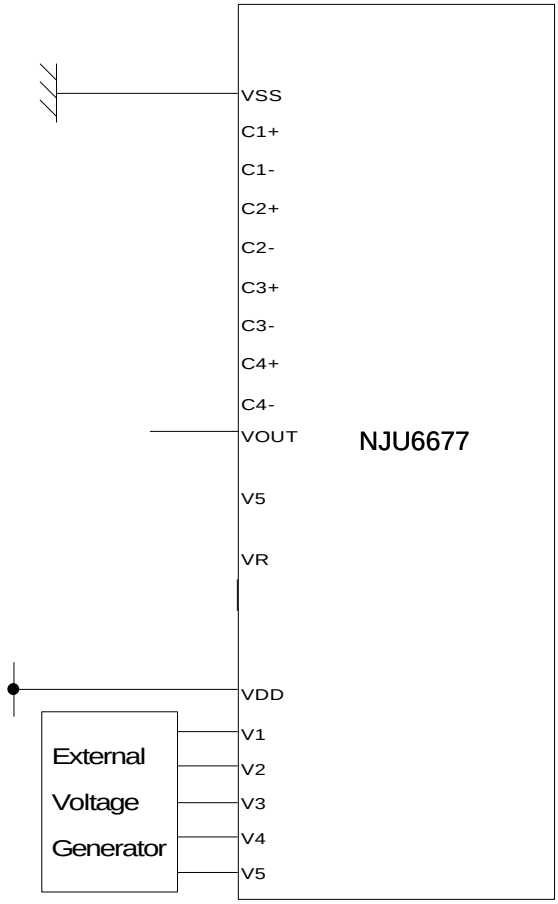
The LCD driving bias voltage of V_1,V_2,V_3,V_4 are generated internally by dividing the V_5 voltage with the internal bleeder resistance. And it is supplied to the LCD driving circuits after the impedance conversion with voltage follower circuit.

As shown in Fig. 4, Five capacitors are required to connect to each LCD driving voltage terminal for voltage stabilizing. And the value of capacitors C5, C6, C7, C8 and C9 are determined depending on the actual LCD panel display evaluation.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

VLCD=VDD-V5 = 9.0 to 10.5V

COUT	to 1.0uF
C1 to C4	to 1.0uF
C5 to C9	0.1 to 0.47uF
R1	2.0MΩ
R2	0.5MΩ
R3	2.5MΩ

Fig.4

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

*2 Following connection of V_{OUT} is required when external power supply using.

When $V_{SS} > V_5$ --- $V_{OUT}=V_5$

When $V_{SS} \leqq V_5$ --- $V_{OUT}=V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6677 interfaces with MPU by 8-bit bidirectional data bus (D_7 to D_0) or serial (SI:D_7). The 8 bit parallel or serial interface is determined by a condition of the P/S terminal connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out operation is impossible.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_7	D_6	D_0 to D_5
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_7	D_6	D_0 to D_5
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	Hi-Z

(5-2) Parallel Interface

The NJU6677 interfaces to 68 or 80 type MPU directly when the parallel interface (P/S="H") is selected. 68 type MPU or 80 is determined by the condition of SEL68 terminal connecting to "H" or "L" as shown in table 6.

Table 6

SEL68	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D_0 to D_7
H	68 type MPU	$\overline{CS}$	A0	E	R/W	D_0 to D_7
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D_0 to D_7

(5-3) Discrimination of Data Bus Signal

The NJU6677 discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminal $\overline{CS}$ set to "L"and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition when the chip is not selected. The data input from SI terminal is MSB first like as the order of D_7,D_6,- - - - D_0, and the data are entered into the shift register synchronizing with the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction of the serial input data is executed by the condition of A0 at the 8th serial clock rise edge. A0="H" is display data and A0="L" is instruction. When $\overline{RES}$ terminal becomes "L" or CS terminal becomes "H" before 8th serial clock rise edge, NJU6677 recognizes them as a instruction data incorrectly. Therefore a unit of serial data must be structured by 8-bit. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface

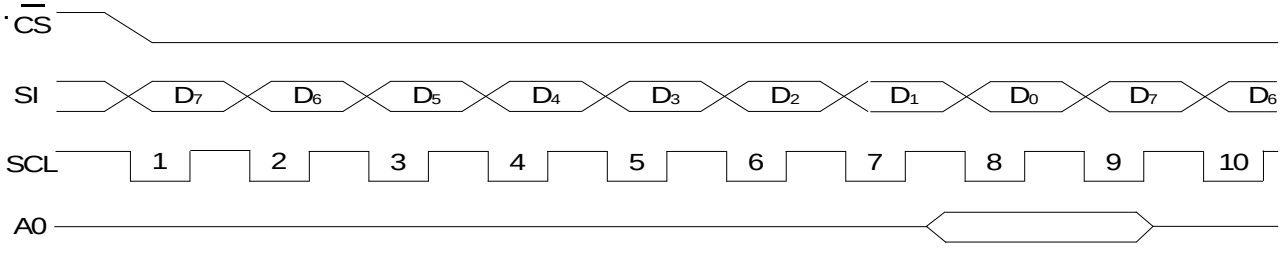


Fig. 5

(5-5) Access to the Display Data RAM and Internal Register.

The NJU6677 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU reads out the data from the Display Data RAM, the read out data in the data read cycle (dummy read) is held in the bus-holder, then it is read out from the bus-holder to the system bus at the next data read cycle. When the MPU writes the data into the Display Data RAM, the data is held in the bus-holder, then it is written into the Display Data RAM by the next data write cycle.

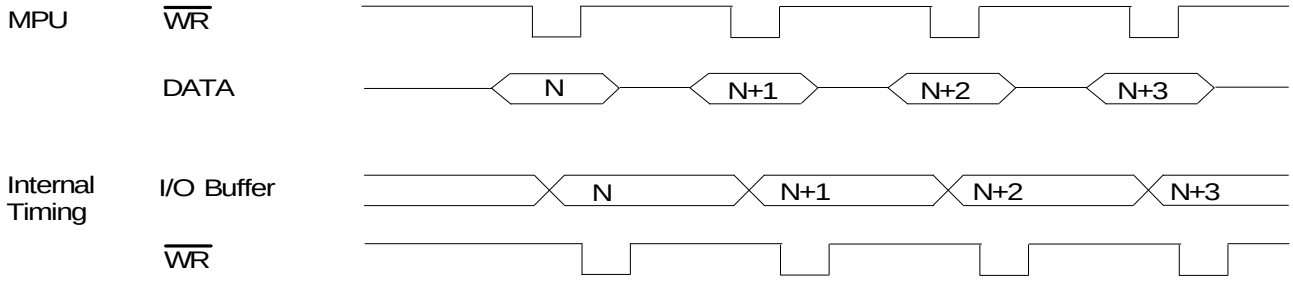
Therefore high speed data transmission between MPU and NJU6677 is available because of it is not limited by the t_{ACC} and t_{DS} as display data RAM access time and is limited by the system cycle time (R) or (W).

If the cycle time is not be kept in the MPU operation, NOP should be inserted to the system instead of the waiting operation.

The read out operation does not read out the data in the pointed address just after the address set operation. And second read out operation can read out the data correctly from the pointed address.

Therefore, one dummy read operation is required after address setting or write cycle as shown in FIG. 6.

● Write Operation



● Read Operation

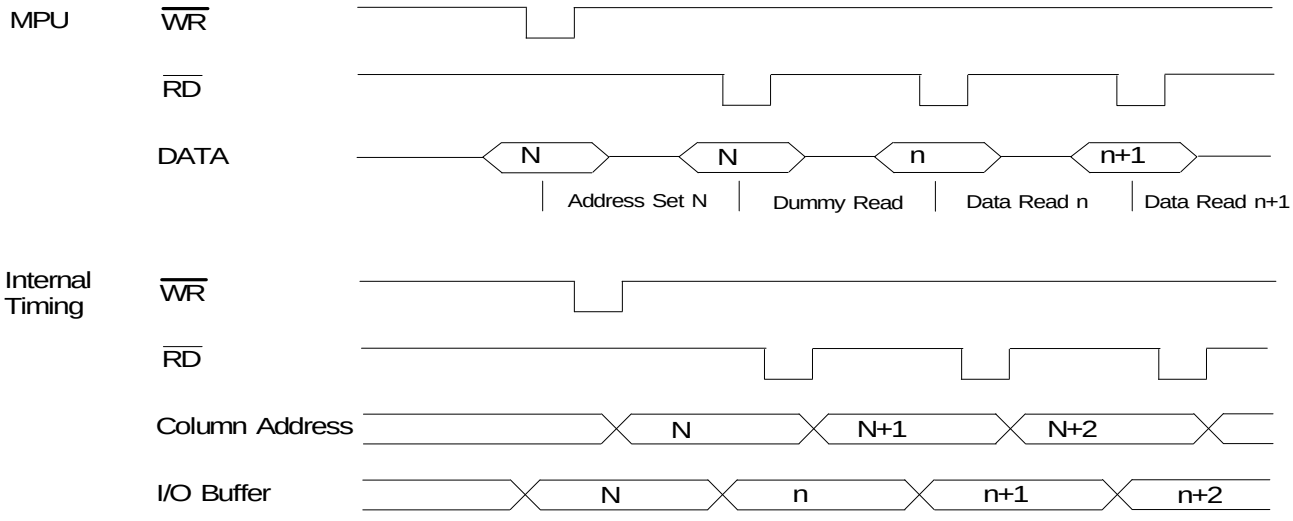


Fig.6

(5-6) Chip Select

$\overline{CS}$ is Chip Select terminal. In case of $\overline{CS}$="L", the interface with MPU is available. In case of $\overline{CS}$="H", the D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, D_7(SI) and D_6(SCL) inputs are ignored. If the serial interface is selected when $\overline{CS}$="H",the shift register and the counter are reset. However, the reset is always operated in any conditions of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	-0.3 to +5.0	V
Supply Voltage (2)	V_5	V_{DD}-18.0 to V_{DD}+0.3	V
Supply Voltage (3)	V_1 to V_4	V_5 to V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opr}	-30 to +80	°C
Storage Temperature	T_{stg}	-55 to +125 (Chip)	°C
		-55 to +100 (TCP)	

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS}=0 V.

Note 3) The relation : $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$; $V_{DD} > V_{SS} \geqq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1) (VDD=2.7V to 3.3V, VSS=0V, Ta=-30 to +80°C)

PARAMETE		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	Note
Operating Voltage(1)		V_{DD}			2.4		3.6	V	5
Operating Voltage(2)		V_5			V_{DD}-18.0		V_{DD}-6.0	V	
		V_1,V_2	V_{LCD}= V_{DD}-V_5		VDD-0.5VLCD		V_{DD}		
		V_3,V_4			V_5		VDD-0.5VLCD		
Input Voltage	High Level	V_{IHC1}	D_0...D_7,A0, CS,RES,RD,WR,SEL68, P/S Terminals		0.8V_{DD}		V_{DD}	V	
	Low Level	V_{ILC1}			V_{SS}		0.2V_{DD}	V	
Output Voltage	High Level	V_{OHC11}	D_0...D_7 Terminals	I_{OH}=-0.5mA	0.8V_{DD}		V_{DD}	V	
	Low Level	V_{OLC11}		I_{OL}= 0.5mA	V_{SS}		0.2V_{DD}	V	
Input Leakage Current		I_{LIO}	All Input terminals		- 1.0		1.0	uA	6
Driver On-resistance		R_{ON1}	Ta=25°C	V_{LCD}=15.0V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD}=8.0V		3.0	4.5		
Stand-by Current		I_{DDQ}	during Power save Mode			T.B.D.	T.B.D.	uA	8
Operating Current		I_{DD12}	Display V_{LCD}=12.0V			T.B.D.	T.B.D.	uA	
		I_{DD21}	Accessing f $_{CYC}$=200kHz			T.B.D.	T.B.D.		9

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Input Terminal Capacitance		C_{IN}	A0,$\overline{CS}$,$\overline{RES}$,$\overline{RD}$,$\overline{WR}$,SEL68, P/S,T1,T2,D_0...D_7 Ta=25°C		10		pF	
Oscillation Frequency		f_{OSC}	Ta=25°C		T.B.D.		kHz	
Voltage Booster	Output Volt.	V_{OUT1}	V_{SS}-Vout, 5-time voltage booster, V_{DD}=3V	VDD-15.0		VDD-14.5	V	
	On-resistance	R_{TRI}	V_{DD}=3V;C1-C4,C_{OUT}=4.7uF 5-time voltage booster		T.B.D.		Ω	
	Adjustment range of LCD Driving Volt.	V_{OUT2}	Voltage Booster Circuit "OFF"	V_{DD}-18.0V		V_{DD}-6.0V	V	10
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"	V_{DD}-18.0V		V_{DD}-6.0V	V	
	Operating Current	I_{OUT1}	V_{DD}=3V, V_{LCD}=12V COM/SEG Terminals Open No Access Display Checkered pattern		T.B.D.	T.B.D.	uA	11
		I_{OUT2}			T.B.D.	T.B.D.		
		I_{OUT3}			T.B.D.	T.B.D.		
	Voltage Reg.	V_{REG}%	V_{DD}=3V,Ta=25°C V_{REG}=4F to FF$_H$			T.B.D.	%	

Note 5) NJU6677 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of the D_0 to D_7 terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,11) Apply to current after "LCD Driving Voltage Set".

Note 8) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD01}.

Note 10) LCD driving voltage V_5 can be adjusted within the voltage follower operating range.

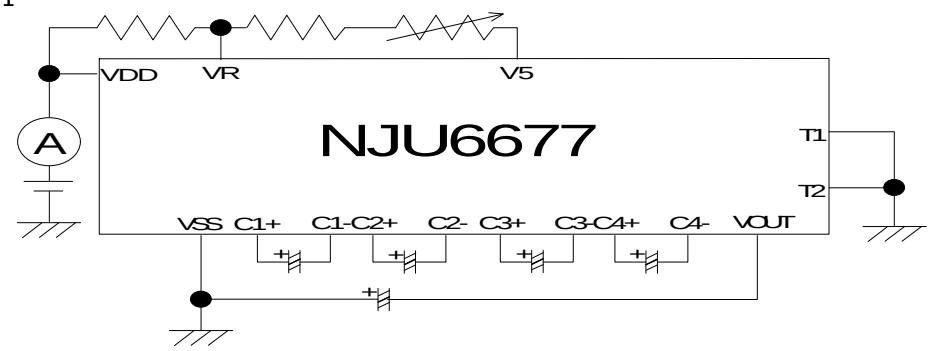
Note 11) Each operating current of voltage supply circuits block is specified under below table conditions.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T_1	T_2	Internal Oscillator	Voltage Booster	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT},V_5)

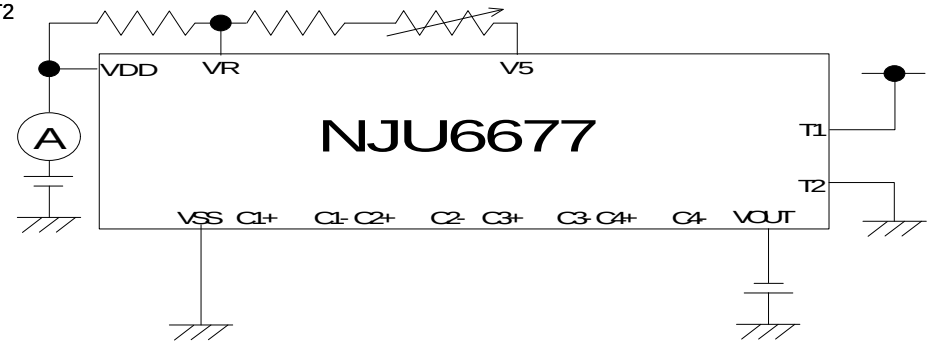
(* = Don't Care)

MEASUREMENT BLOCK DIAGRAM

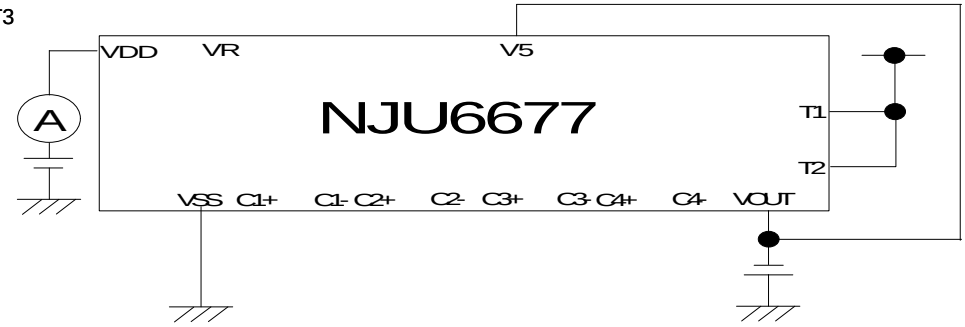
:IOUT1



:IOUT2



:IOUT3



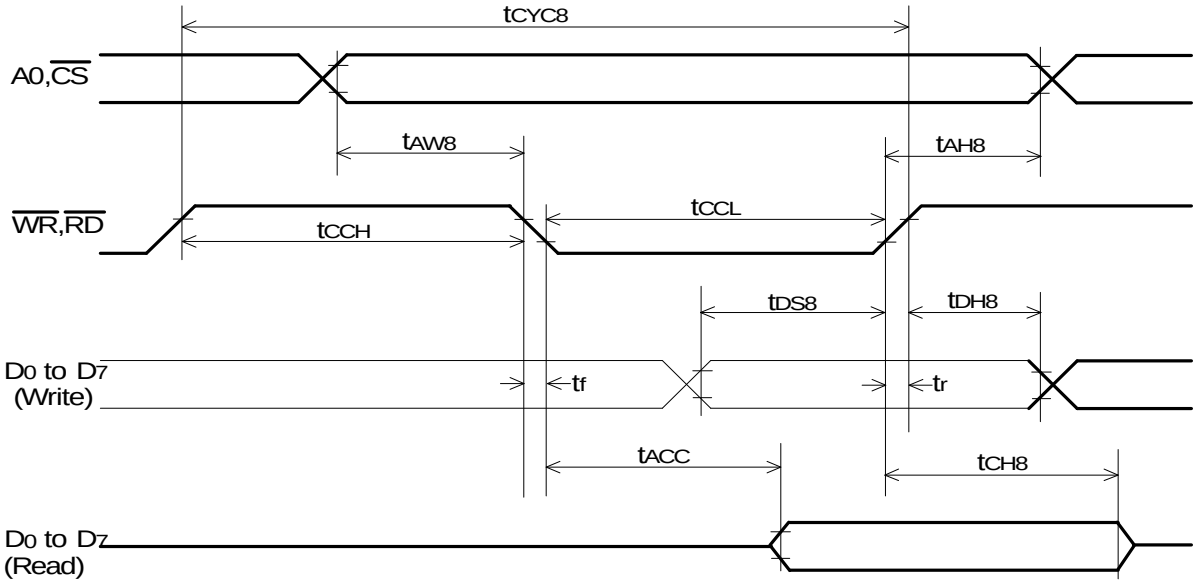
■ ELECTRICAL CHARACTERISTICS (2) (VDD=2.7V to 3.3V, VSS=0V, Ta=-30 to +80°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	12
Reset "L" Level Pulse Width	t_{RW}	$\overline{RES}$ Terminal	10			us	13

Note 12) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.
Note 13) Specified minimum pulse width of $\overline{RES}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

■ BUS TIMING CHARACTERISTICS

- Read/Write operation sequence (80 Type MPU)



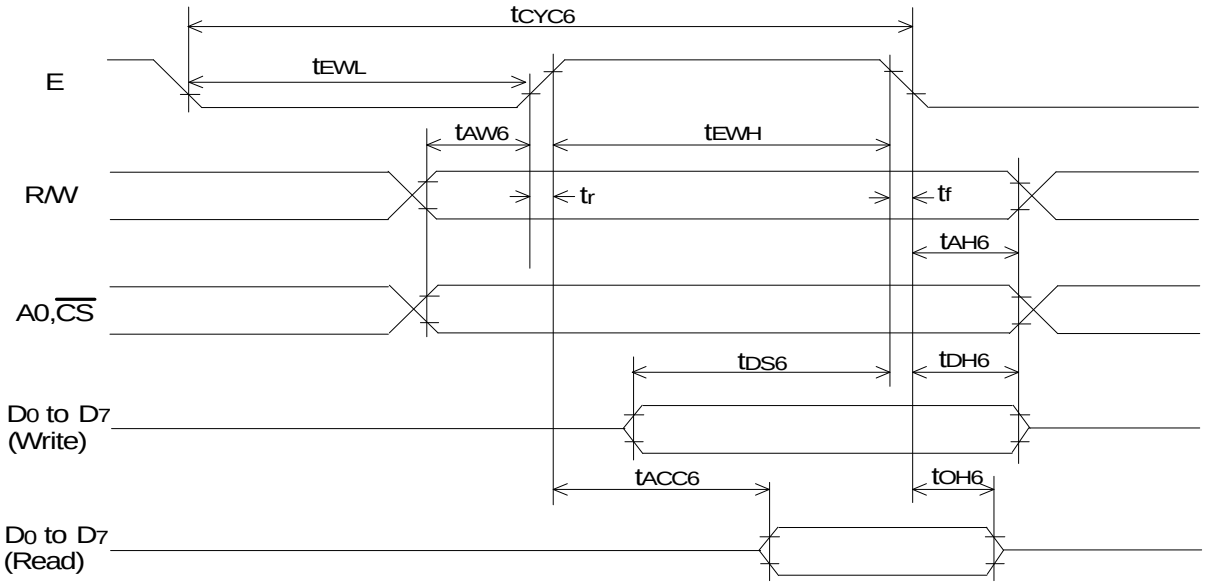
(VDD=2.4V to 3.6V,Ta=-30 to +80°C)

PARAMETER			SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS Terminals	tAH8		10			ns
Address Set Up Time			tAW8		0			ns
System Cycle Time	WR	WR,RD Terminals	tCYC8 (W)		220			ns
	RD		tCYC8 (R)		350			ns
Control Pulse Width	WR,"L"		tCCL(W)		50			ns
	RD,"L"		tCCL(R)		200			ns
	WR"H"		tCCH(W)		160			ns
	RD"-H"		tCCH(R)		160			ns
Data Set Up Time		D0 to D7 Terminals	tDS8		35			ns
Data Hold Time			tDH8		15			ns
RD Access Time			tACC8		120		CL=100pF	ns
Output Disable Time			tCH8		15			ns
Rise Time, Fall Time		CS, WR, RD, A0, D0 to D7 Terminals	tr,tf		15			ns

Note 14) Rise time (tr) and fall time (tf) of input signal should be less than 15ns.

Note 15) Each timing is specified based on 0.2xVDD and 0.8xVDD.

- Read/Write operation sequence (68 Type MPU)



(VDD=2.4V to 3.6V,Ta=-30 to +80°C)

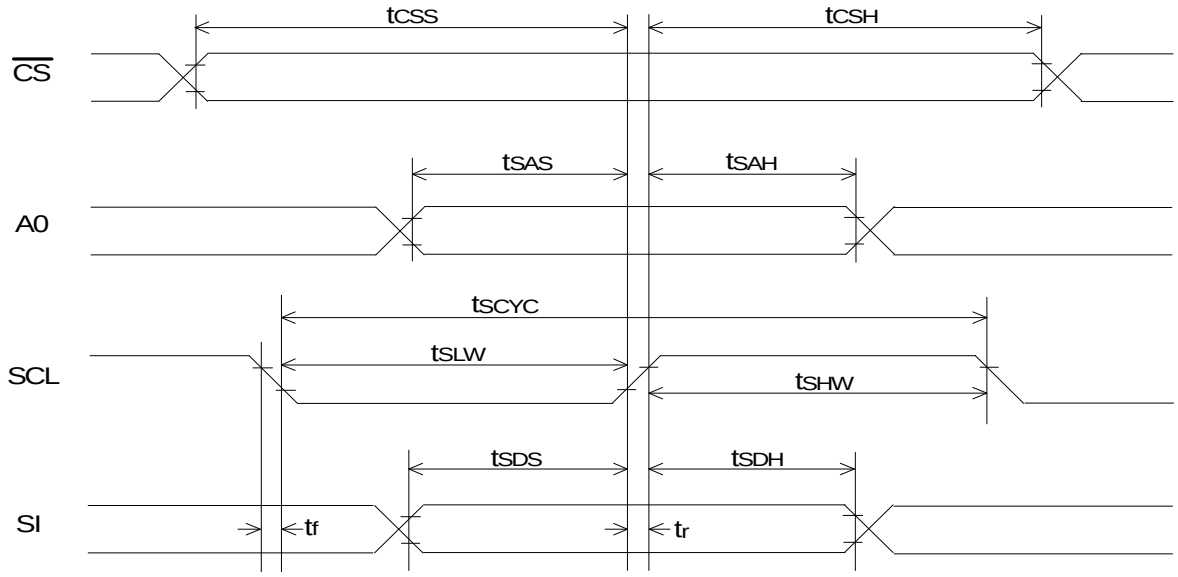
PARAMETER			SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS,R/W Terminals	tAH6		10			ns
Address Set Up Time			tAW6		0			ns
System Cycle Time(W)			tCYC6(W)		220			ns
System Cycle Time(R)			tCYC6(R)		350			ns
Enable Pulse Width	Read"H"	E Terminal	tEWH		200			ns
	Write"H"				50			ns
	Read"L"		tEWL		160			ns
	Write"H"				160			ns
Data Set Up Time		D0 to D7 Terminals	tDS6		35			ns
Data Hold Time			tDH6		15			ns
Access Time			tACC6		150		CL=100pF	ns
Output Disable Time			tOH6		20			ns
Rise Time, Fall Time		A0, CS, R/W, E, D0 to D7 Terminals	tr,tf		15			ns

Note 16) tCYC6 indicates the E signal cycle during the CS activation period. The System Cycle Time must be required after CS becomes active.

Note 17) Rise time (tr) and fall time (tf) of input signal should be less than 15ns.

Note 18) Each timing is specified based on 0.2xVDD and 0.8xVDD.

- Write operation sequence (Serial Interface)



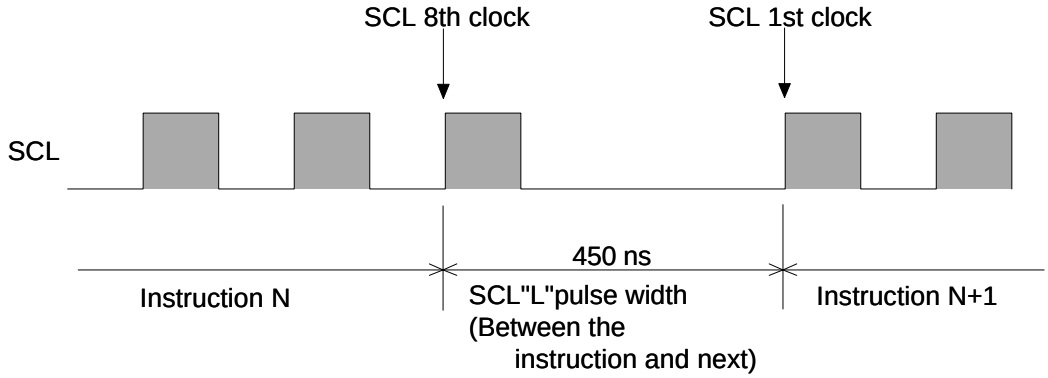
(VDD=2.4V to 3.6V,Ta=-30 to +80°C)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC		60			ns
SCL "H" pulse width		tSHW		30			ns
SCL "L" pulse width		tSLW		30			ns
Address Set Up Time	A0 Terminal	tSAS		0			ns
Address Hold Time		tSAH		150			ns
Data Set Up Time	SI Terminal	tSDS		25			ns
Data Hold Time		tSDH		10			ns
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	tCSS		10			ns
		tCSH		300			ns
Rise Time, Fall Time	SCL, A0, $\overline{CS}$, SI Terminals	tr,tf		15			ns

Note 19) Rise time (tr) and fall time (tf) of input signal should be less than 15ns.

Note 20) Each timing is specified based on 0.2xVDD and 0.8xVDD.

Note 21) In case of instruction set continuously, it is required to wait more than 450ns between the instruction and next as follows.



■ LCD DRIVING WAVEFORM

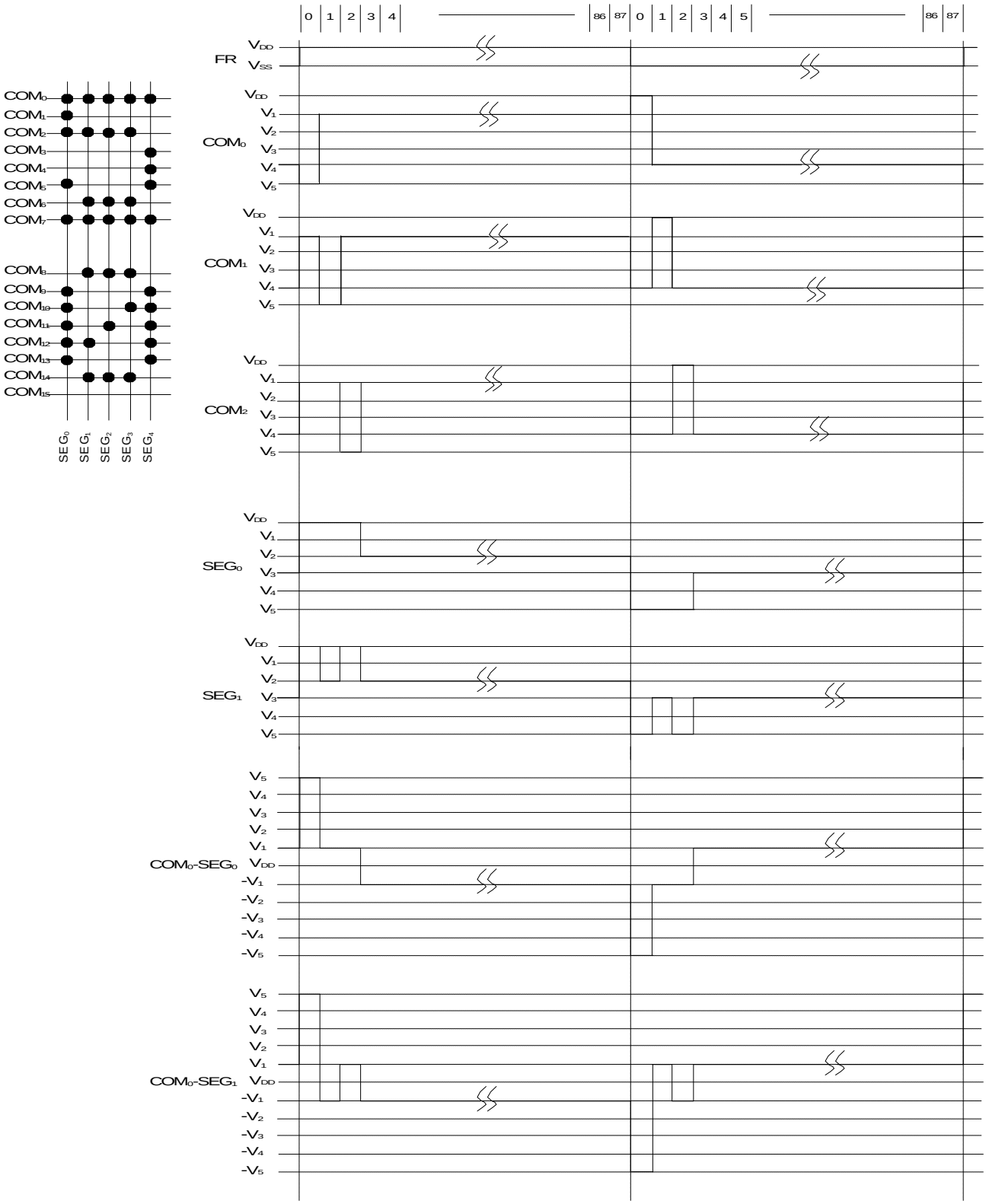


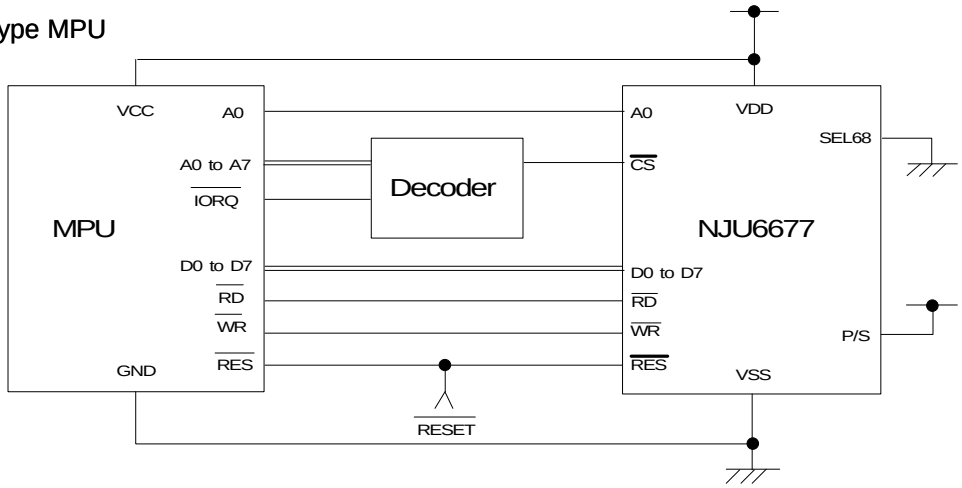
Fig.7

■ APPLICATION CIRCUIT

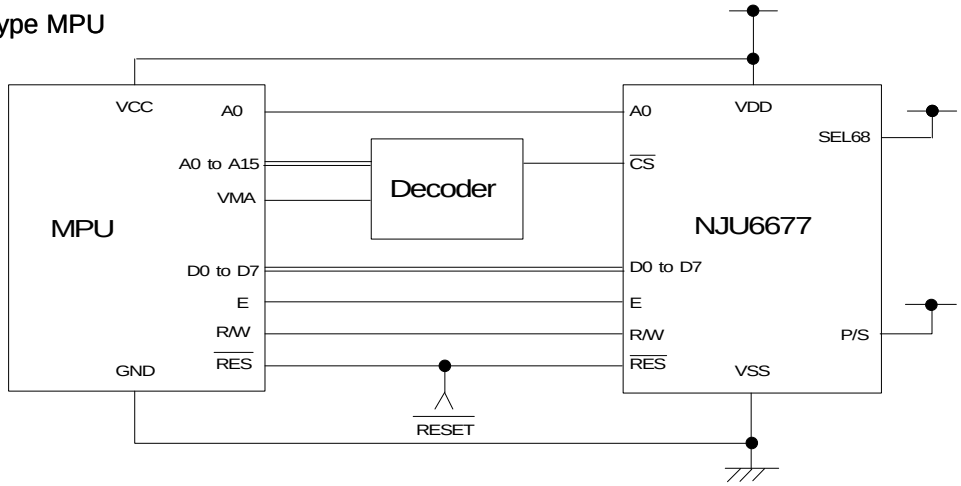
- Microprocessor Interface Example

The NJU6677 interfaces to 80 type or 68 type MPU directly.
And the serial interface also communicate with MPU.

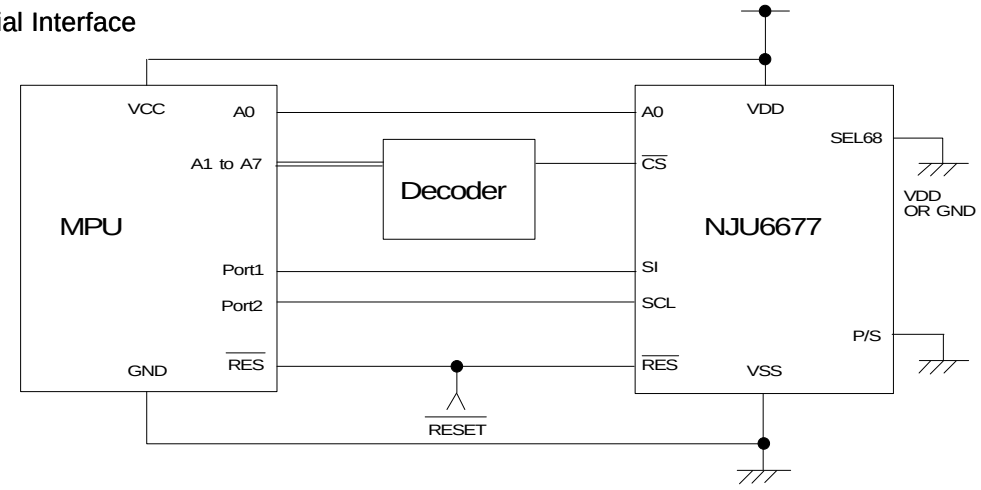
- 80 Type MPU



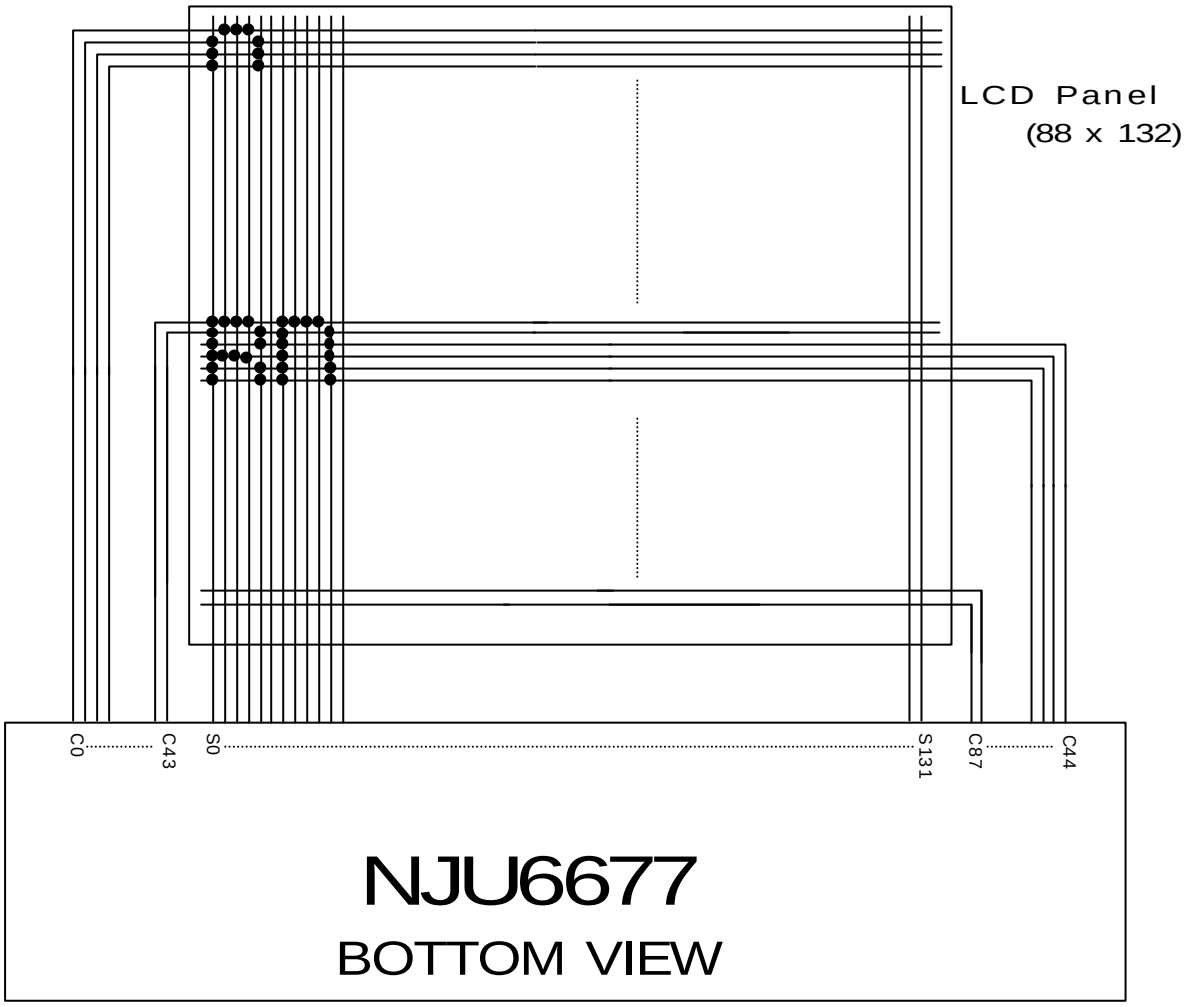
- 68 Type MPU



- Serial Interface



■ LCD Panel Interface Example



■ CAUTION

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