ICS1893 Brief

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3.3-V 10Base-T/100Base-TX Integrated PHYceiver™

General

The ICS1893 is a low-power, physical-layer device (PHY) that supports the ISO/IEC 10Base-T and 100Base-TX Carrier-Sense Multiple Access/Collision Detection (CSMA/CD) Ethernet standards. The ICS1893 architecture is based on the ICS1892. The ICS1893 supports managed or unmanaged node, repeater, and switch applications.

The ICS1893 incorporates digital signal processing (DSP) in its Physical Medium Dependent (PMD) sublayer. As a result, it can transmit and receive data on unshielded twisted-pair (UTP) category 5 cables with attenuation in excess of 24 dB at 100 MHz. With this ICS-patented technology, the ICS1893 can virtually eliminate errors from killer packets.

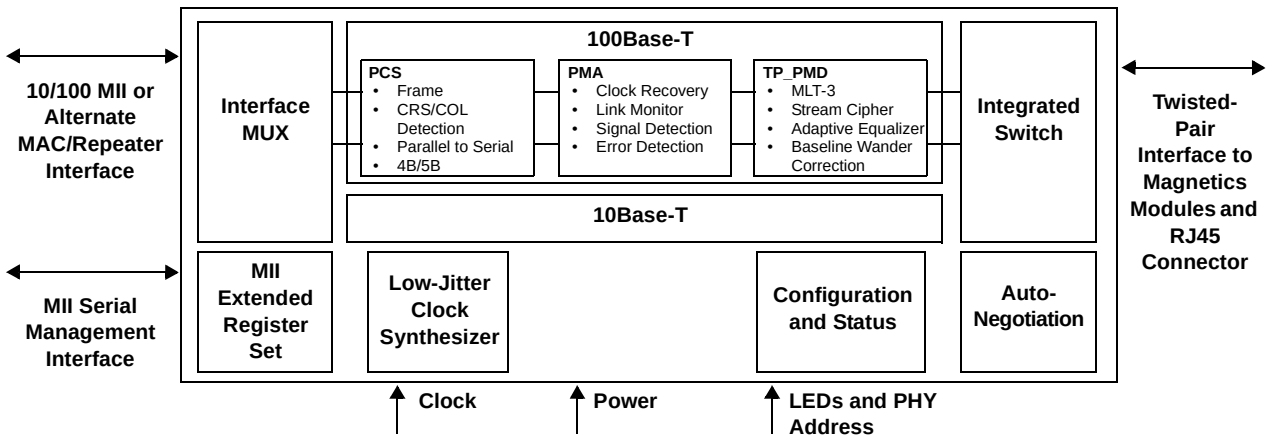
The ICS1893 provides a Serial Management Interface for exchanging command and status information with a Station Management (STA) entity.

The ICS1893 Media Dependent Interface (MDI) can be configured to provide either half- or full-duplex operation at data rates of 10 MHz or 100 MHz. The MDI configuration can be established manually (with input pins or control register settings) or automatically (using the Auto-Negotiation features). When the ICS1893 Auto-Negotiation sublayer is enabled, it exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode they have in common.

Features

- Supports category 5 cables with attenuation in excess of 24 dB at 100 MHz across a temperature range from -5° to +85° C
- DSP-based baseline wander correction to virtually eliminate killer packets across temperature range of from -5° to +85° C
- Low-power, 0.35-micron CMOS (typically 400 mW)
- Single 3.3-V power supply.
- Single-chip, fully integrated PHY provides PCS, PMA, PMD, and AUTONEG sublayers of IEEE standard
- 10Base-T and 100Base-TX IEEE 802.3 compliant
- Fully integrated, DSP-based PMD includes:
  - Adaptive equalization and baseline wander correction
  - Transmit wave shaping and stream cipher scrambler
  - MLT-3 encoder and NRZ/NRZI encoder
- Highly configurable design supports:
  - Node, repeater, and switch applications
  - Managed and unmanaged applications
  - 10M or 100M half- and full-duplex modes
  - Parallel detection
  - Auto-negotiation, with Next Page capabilities
- MAC/Repeater Interface can be configured as:
  - 10M or 100M Media Independent Interface
  - 100M Symbol Interface (bypasses the PCS)
  - 10M 7-wire Serial Interface
- Small Footprint 64-pin Thin Quad Flat Pack (TQFP)

ICS1893 Block Diagram



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

Chapter 3 ICS1893 Enhanced Features

The ICS1893 is an enhanced version of the ICS1890. In contrast to the ICS1890, the ICS1893 offers significant improvements in both performance and features while maintaining backward compatibility. The specific differences between these devices are listed below.

1. The ICS1893 employs an advanced digital signal processing (DSP) architecture that improves the 100Base-TX Receiver performance beyond that of any other PHY in the market. Specifically:
   a. The ICS1893 DSP-based, adaptive equalization process allows the ICS1893 to accommodate a maximum cable attenuation/insertion loss in excess of 24 dB, which is nearly equivalent to the attenuation loss of a 100-meter Category 5 cable.
   b. The ICS1893 DSP-based, baseline-wander correction process eliminates killer packets.
2. The analog 10Base-T Receive Phase-Locked Loop (PLL) of the ICS1890 is replaced with a digital PLL in the ICS1893, thereby resulting in lower jitter and improved stability.
3. The ICS1890 Frequency-Locked Loop (FLL) that is part of the 100Base-TX Clock and Data Recovery circuitry is replaced with a digital FLL in the ICS1893, also resulting in lower jitter and improved stability.
4. The ICS1893 transmit circuits are improved in contrast to the ICS1890, resulting in a decrease in the magnitude of the 10Base-T harmonic content generated during transmission. (See ISO/IEC 8802-3: 1993 clause 8.3.1.3.)
5. The ICS1893 supports the Auto-Negotiation Next Page functions described in IEEE Std 802.3u-1995 clause 28.2.3.4.
6. The ICS1893 supports Management Frame (MF) Preamble Suppression.
7. The ICS1893 provides the Remote Jabber capability.
8. The ICS1893 has an improved version of the ICS1890 10Base-T Squelch operation.
9. The ICS1893 “seeds” (that is, initializes) the Transmit Stream Cipher Shift register by using the ICS1893 PHY address from Table 8-16, which minimizes crosstalk and noise in repeater applications.
10. The ICS1893 offers an automatic 10Base-T power-down mode.
11. The enhanced features of the ICS1893 required some modifications to the ICS1890 Management Registers. However, the ICS1893 Management Registers are backward-compatible with the ICS1890 Management Registers. Table 3-1 summarizes the differences between the ICS1890 and the ICS1893 Management Registers.

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Table 3-1. Summary of Differences between ICS1890 and ICS1893 Registers

Register. Bit(s)	ICS1890		ICS1893	
	Function	**Default**	**Function**	**Default**
1.6	Reserved	0b (always)	Management Frame Preamble Suppression	0b
3.9:4	Model Number	000010b	Model Number	000011b
3.3:0	Revision Number	0011b	Revision Number	0000b
6.2	Next Page Able	0b (always)	Next Page Able	1b
7.15:0	Not applicable (N/A)	N/A	Auto-Negotiate Next Page Transmit Register	2001h
8.15:0	N/A	N/A	Auto-Negotiate Next Page Link Partner Ability	0000h
9.15:0 through 15.15:0	IEEE reserved.	0000h	IEEE reserved. **Note:** Although the default value is changed, this response more accurately reflects an MDIO access to registers 9–15.	FFFFh
18.15	Reserved	0b	Remote Jabber	0b
19.1	Reserved	0b	Automatic 10Base-T Power Down	1b
20.15:0 through 31.15:0	N/A	N/A	ICS test registers. (There is no claim of backward compatibility for these registers.)	See specific registers and bits.

Note:

1. There are new registers and bits. For example:
   a. Registers 7 and 8 are new (that is, the ICS1890 does not have these registers).
   b. Registers 20 through 31 are new ICS test registers.
2. For some bits (such as the model number and revision number bits), the default values are changed.

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Chapter 4 Overview of the ICS1893

The ICS1893 is a stream processor. During data transmission, it accepts sequential nibbles from its MAC (Media Access Control)/Repeater Interface, converts them into a serial bit stream, encodes them, and transmits them over the medium through an external isolation transformer. When receiving data, the ICS1893 converts and decodes a serial bit stream (acquired from an isolation transformer that interfaces with the medium) into sequential nibbles. It subsequently presents these nibbles to its MAC/Repeater Interface.

The ICS1893 implements the OSI model's physical layer, consisting of the following, as defined by the ISO/IEC 8802-3 standard:

- Physical Coding sublayer (PCS)
- Physical Medium Attachment sublayer (PMA)
- Physical Medium Dependent sublayer (PMD)
- Auto-Negotiation sublayer

The ICS1893 is transparent to the next layer of the OSI model, the link layer. The link layer has two sublayers: the Logical Link Control sublayer and the MAC sublayer. The ICS1893 can interface directly to the MAC and offers multiple, configurable modes of operation. Alternately, this configurable interface can be connected to a repeater, which extends the physical layer of the OSI model.

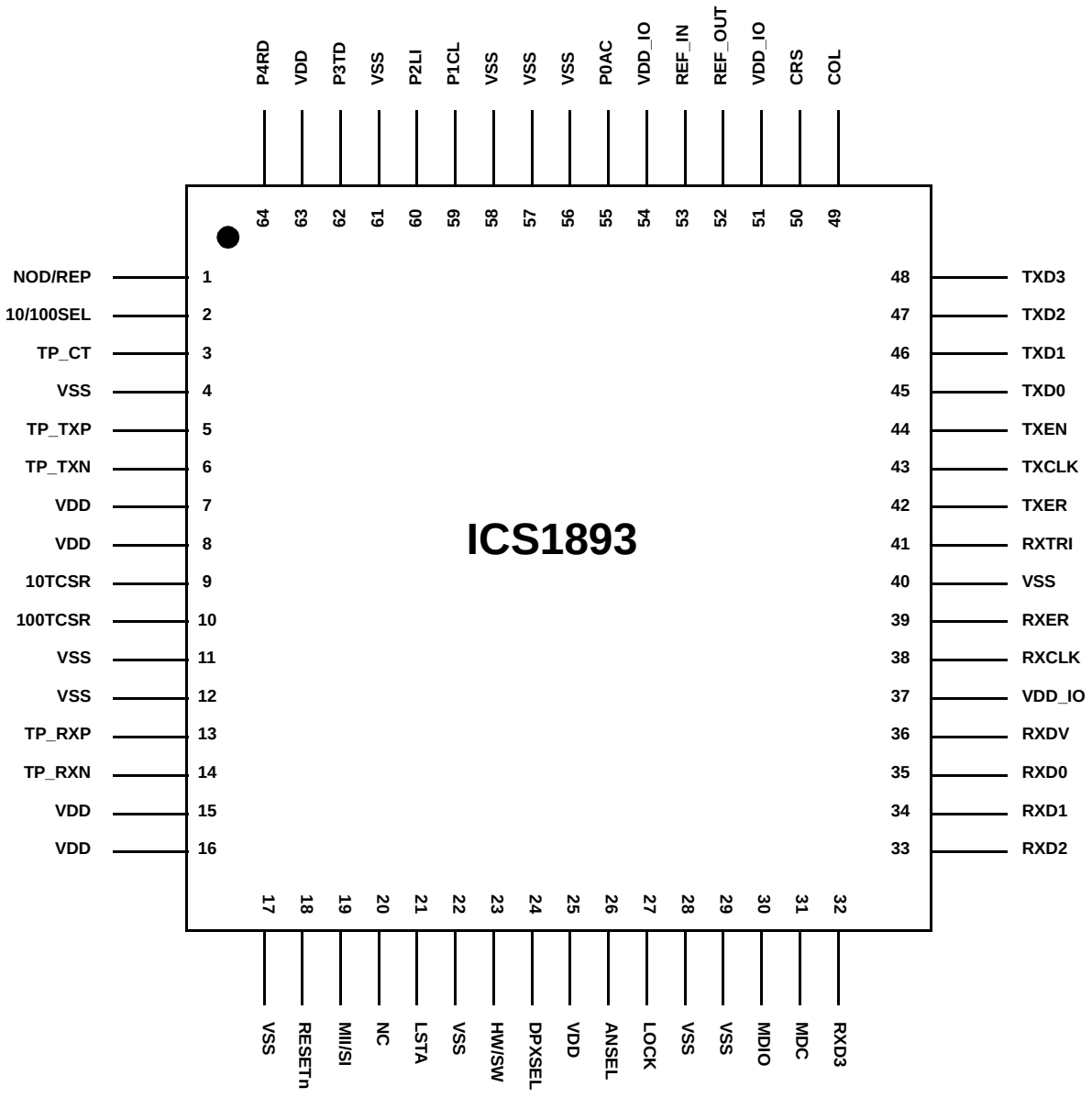
The ICS1893 transmits framed packets acquired from its MAC/Repeater Interface and receives encapsulated packets from another PHY, which it translates and presents to its MAC/Repeater Interface.

Note: As per the ISO/IEC standard, the ICS1893 does not affect, nor is it affected by, the underlying structure of the MAC/repeater frame it is conveying.

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Chapter 9 Pin Diagram, Listings, and Descriptions

9.1 ICS1893 Pin Diagram



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10.4 DC Operating Characteristics

This section lists the ICS1893 DC operating characteristics.

10.4.1 DC Operating Characteristics for Supply Current

Table 10-4 lists the DC operating characteristics for the supply current to the ICS1893 under various conditions.

Note: All VDD_IO measurements are taken with respect to VSS (which equals 0 V).

Table 10-4. DC Operating Characteristics for Supply Current

Parameter	Operating Mode	Symbol	Min.	Typ.	Max.	Units
Supply Current†	100Base-TX‡	IDD_IO	–	8	11	mA
		IDD	–	110	125	mA
Supply Current†	10Base-T‡	IDD_IO	–	5	8	mA
		IDD	–	150	160	mA
Supply Current†	Auto-Negotiation	IDD_IO	–	5	8	mA
		IDD	–	80	90	mA
Supply Current†	Power-Down	IDD_IO	–	3	5	mA
		IDD	–	40	50	mA
Supply Current†	Reset	IDD	–	50	60	mA

† These supply current parameters are measured through VDD pins to the ICS1893. The supply current parameters include external transformer currents.

‡ Measurements taken with 100% data transmission and the minimum inter-packet gap.

10.4.2 DC Operating Characteristics for TTL Inputs and Outputs

Table 10-5 lists the 3.3-V DC operating characteristics of the ICS1893 TTL inputs and outputs.

Note: All VDD_IO measurements are taken with respect to VSS (which equals 0 V).

Table 10-5. 3.3-V DC Operating Characteristics for TTL Inputs and Outputs

Parameter	Symbol	Conditions		Min.	Max.	Units
TTL Input High Voltage	V_{IH}	VDD_IO = 3.47 V	–	2.0	–	V
TTL Input Low Voltage	V_{IL}	VDD_IO = 3.47 V	–	–	0.8	V
TTL Output High Voltage	V_{OH}	VDD_IO = 3.14 V	I_{OH} = –4 mA	2.4	–	V
TTL Output Low Voltage	V_{OL}	VDD_IO = 3.14 V	I_{OL} = +4 mA	–	0.4	V
TTL Driving CMOS, Output High Voltage	V_{OH}	VDD_IO = 3.14 V	I_{OH} = –4 mA	2.4	–	V
TTL Driving CMOS, Output Low Voltage	V_{OL}	VDD_IO = 3.14 V	I_{OL} = +4 mA	–	0.4	V

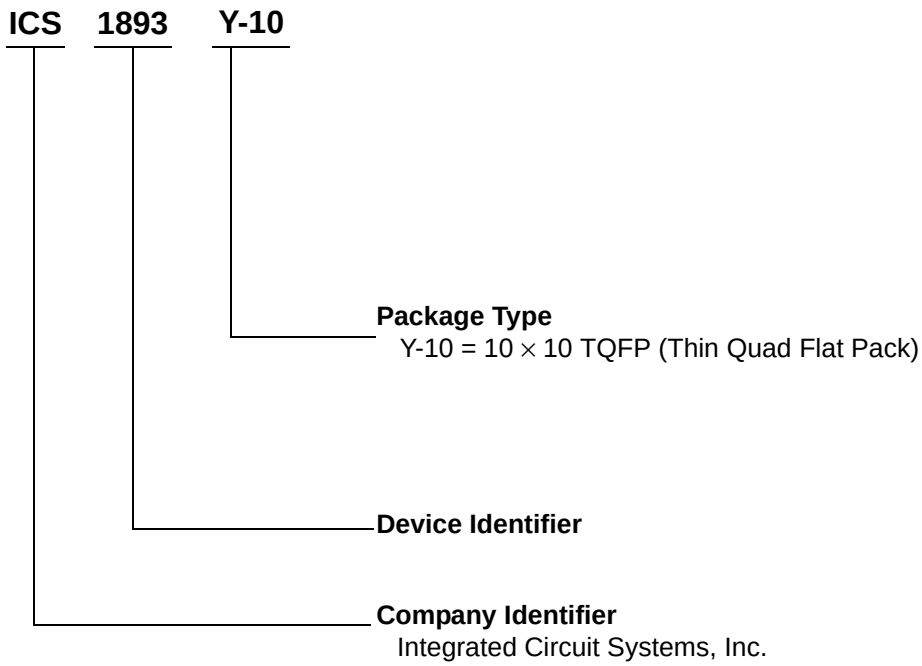
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Chapter 12 Ordering Information

Figure 12-1 shows ordering information for the ICS1893 package:

- ICS1893Y-10

Figure 12-1. ICS1893 Ordering Information



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