# 1. Cyclone III Device Datasheet

CIII52001-3.5

This chapter describes the electric characteristics, switching characteristics, and I/O timing for Cyclone® III devices. A glossary is also included for your reference.

## Electrical Characteristics

The following sections provide information about the absolute maximum ratings, recommended operating conditions, DC characteristics, and other specifications for Cyclone III devices.

### Operating Conditions

When Cyclone III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone III devices, system designers must consider the operating requirements in this document. Cyclone III devices are offered in commercial, industrial, and automotive grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades. Industrial and automotive devices are offered only in –7 speed grade.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with "C" prefix, industrial with "I" prefix, and automotive with "A" prefix. Commercial devices are therefore indicated as C6, C7, and C8 per respective speed grades. Industrial and automotive devices are indicated as I7 and A7, respectively.

#### Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone III devices.

© 2012 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

ISO 9001:2008 Registered

Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

**Table 1–1. Cyclone III Devices Absolute Maximum Ratings** *(1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic | –0.5 | 1.8 | V |
| $V_{CCIO}$ | Supply voltage for output buffers | –0.5 | 3.9 | V |
| $V_{CCA}$ | Supply voltage (analog) for phase-locked loop (PLL) regulator | –0.5 | 3.75 | V |
| $V_{CCD_PLL}$ | Supply voltage (digital) for PLL | –0.5 | 1.8 | V |
| $V_I$ | DC input voltage | –0.5 | 3.95 | V |
| $I_{OUT}$ | DC output current, per pin | –25 | 40 | mA |
| $V_{ESDHBM}$ | Electrostatic discharge voltage using the human body model | — | ±2000 | V |
| $V_{ESDCDM}$ | Electrostatic discharge voltage using the charged device model | — | ±500 | V |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |

**Note to Table 1–1:**

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

### Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as percentage of high-time over the lifetime of the device.

A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.2 V can only be at 4.2 V for 10.74% over the lifetime of the device; for device lifetime of 10 years, this amounts to 10.74/10ths of a year.

**Table 1–2. Cyclone III Devices Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame** *(1)*

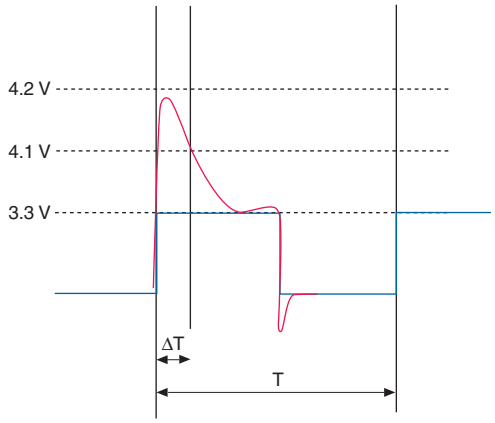
| Symbol | Parameter | Condition | Overshoot Duration as % of High Time | Unit |
|---|---|---|---|---|
| $V_i$ | AC Input Voltage | $V_I$ = 3.95 V | 100 | % |
| | | $V_I$ = 4.0 V | 95.67 | % |
| | | $V_I$ = 4.05 V | 55.24 | % |
| | | $V_I$ = 4.10 V | 31.97 | % |
| | | $V_I$ = 4.15 V | 18.52 | % |
| | | $V_I$ = 4.20 V | 10.74 | % |
| | | $V_I$ = 4.25 V | 6.23 | % |
| | | $V_I$ = 4.30 V | 3.62 | % |
| | | $V_I$ = 4.35 V | 2.1 | % |
| | | $V_I$ = 4.40 V | 1.22 | % |
| | | $V_I$ = 4.45 V | 0.71 | % |
| | | $V_I$ = 4.50 V | 0.41 | % |
| | | $V_I$ = 4.60 V | 0.14 | % |
| | | $V_I$ = 4.70 V | 0.047 | % |

**Note to Table 1–2:**

(1) Figure 1–1 shows the methodology to determine the overshoot duration. In the example in Figure 1–1, overshoot voltage is shown in red and is present on the input pin of the Cyclone III device at over 4.1 V but below 4.2 V. From Table 1–1, for an overshoot of 4.1 V, the percentage of high time for the overshoot can be as high as 31.97% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1 shows the methodology to determine the overshoot duration.

**Figure 1–1. Cyclone III Devices Overshoot Duration**



## Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone III devices. The steady-state voltage and current values expected from Cyclone III devices are provided in Table 1–3. All supplies must be strictly monotonic without plateaus.

**Table 1–3. Cyclone III Devices Recommended Operating Conditions** *(1), (2)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCINT}$ *(3)* | Supply voltage for internal logic | — | 1.15 | 1.2 | 1.25 | V |
| $V_{CCIO}$ *(3), (4)* | Supply voltage for output buffers, 3.3-V operation | — | 3.135 | 3.3 | 3.465 | V |
| | Supply voltage for output buffers, 3.0-V operation | — | 2.85 | 3 | 3.15 | V |
| | Supply voltage for output buffers, 2.5-V operation | — | 2.375 | 2.5 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | — | 1.71 | 1.8 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | — | 1.425 | 1.5 | 1.575 | V |
| | Supply voltage for output buffers, 1.2-V operation | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCA}$ *(3)* | Supply (analog) voltage for PLL regulator | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD_PLL}$ *(3)* | Supply (digital) voltage for PLL | — | 1.15 | 1.2 | 1.25 | V |
| $V_I$ | Input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | — | 85 | °C |
| | | For industrial use | –40 | — | 100 | °C |
| | | For extended temperature | –40 | — | 125 | °C |
| | | For automotive use | –40 | — | 125 | °C |
| $t_{RAMP}$ | Power supply ramp time | Standard power-on reset (POR) *(5)* | 50 µs | — | 50 ms | — |
| | | Fast POR *(6)* | 50 µs | — | 3 ms | — |
| $I_{Diode}$ | Magnitude of DC current across PCI-clamp diode when enabled | — | — | — | 10 | mA |

**Notes to Table 1–3:**

(1) $V_{CCIO}$ for all I/O banks must be powered up during device operation. All $V_{CCA}$ pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

(2) $V_{CCD_PLL}$ must always be connected to $V_{CCINT}$ through a decoupling capacitor and ferrite bead.

(3) The $V_{CC}$ must rise monotonically.

(4) All input buffers are powered by the $V_{CCIO}$ supply.

(5) POR time for Standard POR ranges between 50–200 ms. Each individual power supply should reach the recommended operating range within 50 ms.

(6) POR time for Fast POR ranges between 3–9 ms. Each individual power supply should reach the recommended operating range within 3 ms.

## DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone III devices.

### Supply Current

Standby current is the current the device draws after the device is configured with no inputs or outputs toggling and no activity in the device. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary largely with the resources used. Table 1–4 lists I/O pin leakage current for Cyclone III devices.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 1–4. Cyclone III Devices I/O Pin Leakage Current** *(1), (2)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I$ = 0 V to $V_{CCIOMAX}$ | –10 | — | 10 | µA |
| $I_{OZ}$ | Tristated I/O pin leakage current | $V_O$ = 0 V to $V_{CCIOMAX}$ | –10 | — | 10 | µA |

**Notes to Table 1–4:**

(1) This value is specified for normal device operation. The value varies during device power-up. This applies for all $V_{CCIO}$ settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

### Bus Hold

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–5 lists bus hold specifications for Cyclone III devices.

**Table 1–5. Cyclone III Devices Bus Hold Parameter** ***(Part 1 of 2)*** *(1)*

| Parameter | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold low, sustaining current | $V_{IN} > V_{IL}$ (maximum) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus-hold high, sustaining current | $V_{IN} < V_{IL}$ (minimum) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |

**Table 1–5. Cyclone III Devices Bus Hold Parameter *(Part 2 of 2)*** (1)

| Parameter | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold low, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus-hold high, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |
| Bus-hold trip point | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

**Note to Table 1–5:**

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

## OCT Specifications

Table 1–6 lists the variation of OCT without calibration across process, temperature, and voltage.

**Table 1–6. Cyclone III Devices Series OCT without Calibration Specifications**

| Description | $V_{CCIO}$ (V) | Resistance Tolerance | | Unit |
|---|---|---|---|---|
| | | Commercial Max | Industrial and Automotive Max | |
| Series OCT without calibration | 3.0 | ±30 | ±40 | % |
| | 2.5 | ±30 | ±40 | % |
| | 1.8 | +40 | ±50 | % |
| | 1.5 | +50 | ±50 | % |
| | 1.2 | +50 | ±50 | % |

OCT calibration is automatically performed at device power-up for OCT enabled I/Os.

Table 1–7 lists the OCT calibration accuracy at device power-up.

**Table 1–7. Cyclone III Devices Series OCT with Calibration at Device Power-Up Specifications**

| Description | $V_{CCIO}$ (V) | Calibration Accuracy | | Unit |
|---|---|---|---|---|
| | | Commercial Max | Industrial and Automotive Max | |
| Series OCT with calibration at device power-up | 3.0 | ±10 | ±10 | % |
| | 2.5 | ±10 | ±10 | % |
| | 1.8 | ±10 | ±10 | % |
| | 1.5 | ±10 | ±10 | % |
| | 1.2 | ±10 | ±10 | % |

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up. Use Table 1–8 and Equation 1–1 to determine the final OCT resistance considering the variations after calibration at device power-up. Table 1–8 lists the change percentage of the OCT resistance with voltage and temperature.

**Table 1–8. Cyclone III Devices OCT Variation After Calibration at Device Power-Up**

| Nominal Voltage | dR/dT (%/°C) | dR/dV (%/mV) |
|---|---|---|
| 3.0 | 0.262 | –0.026 |
| 2.5 | 0.234 | –0.039 |
| 1.8 | 0.219 | –0.086 |
| 1.5 | 0.199 | –0.136 |
| 1.2 | 0.161 | –0.288 |

**Equation 1–1.** *(1), (2), (3), (4), (5), (6)*

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV \quad (7)$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \quad (8)$$

$$\text{For } \Delta R_x < 0;\ MF_x = 1/(|\Delta R_x|/100 + 1) \quad (9)$$

$$\text{For } \Delta R_x > 0;\ MF_x = \Delta R_x/100 + 1 \quad (10)$$

$$MF = MF_V \times MF_T \quad (11)$$

$$R_{final} = R_{initial} \times MF \quad (12)$$

**Notes to Equation 1–1:**

(1) $T_2$ is the final temperature.
(2) $T_1$ is the initial temperature.
(3) MF is multiplication factor.
(4) $R_{final}$ is final resistance.
(5) $R_{initial}$ is initial resistance.
(6) Subscript × refers to both $_V$ and $_T$.
(7) $\Delta R_V$ is variation of resistance with voltage.
(8) $\Delta R_T$ is variation of resistance with temperature.
(9) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
(10) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
(11) $V_2$ is final voltage.
(12) $V_1$ is the initial voltage.

Example 1–1 shows you the example to calculate the change of 50 Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V:

**Example 1–1.**

$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$

$\Delta R_T = (85 - 25) \times 0.262 = 15.72$

Because $\Delta R_V$ is negative,

$MF_V = 1 / (3.83/100 + 1) = 0.963$

Because $\Delta R_T$ is positive,

$MF_T = 15.72/100 + 1 = 1.157$

$MF = 0.963 \times 1.157 = 1.114$

$R_{final} = 50 \times 1.114 = 55.71\ \Omega$

## Pin Capacitance

Table 1–9 lists the pin capacitance for Cyclone III devices.

**Table 1–9. Cyclone III Devices Pin Capacitance**

| Symbol | Parameter | Typical – QFP | Typical – FBGA | Unit |
|---|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on top/bottom I/O pins | 7 | 6 | pF |
| $C_{IOLR}$ | Input capacitance on left/right I/O pins | 7 | 5 | pF |
| $C_{LVDSLR}$ | Input capacitance on left/right I/O pins with dedicated LVDS output | 8 | 7 | pF |
| $C_{VREFLR}$ (1) | Input capacitance on left/right dual-purpose VREF pin when used as $V_{REF}$ or user I/O pin | 21 | 21 | pF |
| $C_{VREFTB}$ (1) | Input capacitance on top/bottom dual-purpose VREF pin when used as $V_{REF}$ or user I/O pin | 23 (2) | 23 (2) | pF |
| $C_{CLKTB}$ | Input capacitance on top/bottom dedicated clock input pins | 7 | 6 | pF |
| $C_{CLKLR}$ | Input capacitance on left/right dedicated clock input pins | 6 | 5 | pF |

**Notes to Table 1–9:**

(1) When VREF pin is used as regular input or output, a reduced performance of toggle rate and $t_{CO}$ is expected due to higher pin capacitance.

(2) $C_{VREFTB}$ for EP3C25 is 30 pF.

### Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1–10 lists the weak pull-up and pull-down resistor values for Cyclone III devices.

**Table 1–10. Cyclone III Devices Internal Weak Pull-Up and Weak Pull-Down Resistor** *(1)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{_PU}$ | Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled | $V_{CCIO}$ = 3.3 V ± 5% *(2), (3)* | 7 | 25 | 41 | kΩ |
| | | $V_{CCIO}$ = 3.0 V ± 5% *(2), (3)* | 7 | 28 | 47 | kΩ |
| | | $V_{CCIO}$ = 2.5 V ± 5% *(2), (3)* | 8 | 35 | 61 | kΩ |
| | | $V_{CCIO}$ = 1.8 V ± 5% *(2), (3)* | 10 | 57 | 108 | kΩ |
| | | $V_{CCIO}$ = 1.5 V ± 5% *(2), (3)* | 13 | 82 | 163 | kΩ |
| | | $V_{CCIO}$ = 1.2 V ± 5% *(2), (3)* | 19 | 143 | 351 | kΩ |
| $R_{_PD}$ | Value of I/O pin pull-down resistor before and during configuration | $V_{CCIO}$ = 3.3 V ± 5% *(4)* | 6 | 19 | 30 | kΩ |
| | | $V_{CCIO}$ = 3.0 V ± 5% *(4)* | 6 | 22 | 36 | kΩ |
| | | $V_{CCIO}$ = 2.5 V ± 5% *(4)* | 6 | 25 | 43 | kΩ |
| | | $V_{CCIO}$ = 1.8 V ± 5% *(4)* | 7 | 35 | 71 | kΩ |
| | | $V_{CCIO}$ = 1.5 V ± 5% *(4)* | 8 | 50 | 112 | kΩ |

**Notes to Table 1–10:**

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pin. Weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(3) $R_{_PU} = (V_{CCIO} – V_I)/I_{R_PU}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, $V_I = V_{CC}$ + 5% – 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, $V_I$ = 0 V;
Maximum condition: 125°C; $V_{CCIO} = V_{CC}$ – 5%, $V_I$ = 0 V; in which $V_I$ refers to the input voltage at the I/O pin.

(4) $R_{_PD} = V_I/I_{R_PD}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, $V_I$ = 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, $V_I = V_{CC}$ – 5%;
Maximum condition: 125°C; $V_{CCIO} = V_{CC}$ – 5%, $V_I = V_{CC}$ – 5%; in which $V_I$ refers to the input voltage at the I/O pin.

### Hot Socketing

Table 1–11 lists the hot-socketing specifications for Cyclone III devices.

**Table 1–11. Cyclone III Devices Hot-Socketing Specifications**

| Symbol | Parameter | Maximum |
|---|---|---|
| $I_{IOPIN(DC)}$ | DC current per I/O pin | 300 µA |
| $I_{IOPIN(AC)}$ | AC current per I/O pin | 8 mA *(1)* |

**Note to Table 1–11:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which C is I/O pin capacitance and dv/dt is the slew rate.

### Schmitt Trigger Input

Cyclone III devices support Schmitt trigger input on TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate. Table 1–12 lists the hysteresis specifications across supported $V_{CCIO}$ range for Schmitt trigger inputs in Cyclone III devices.

**Table 1–12. Hysteresis Specifications for Schmitt Trigger Input in Cyclone III Devices**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{SCHMITT}$ | Hysteresis for Schmitt trigger input | $V_{CCIO}$ = 3.3 V | 200 | — | — | mV |
| | | $V_{CCIO}$ = 2.5 V | 200 | — | — | mV |
| | | $V_{CCIO}$ = 1.8 V | 140 | — | — | mV |
| | | $V_{CCIO}$ = 1.5 V | 110 | — | — | mV |

## I/O Standard Specifications

The following tables list input voltage sensitivities ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Cyclone III devices. Table 1–13 through Table 1–18 provide the I/O standard specifications for Cyclone III devices.

**Table 1–13. Cyclone III Devices Single-Ended I/O Standard Specifications** *(1), (2)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3-V LVTTL *(3)* | 3.135 | 3.3 | 3.465 | — | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | –4 |
| 3.3-V LVCMOS *(3)* | 3.135 | 3.3 | 3.465 | — | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 2 | –2 |
| 3.0-V LVTTL *(3)* | 2.85 | 3.0 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | 0.45 | 2.4 | 4 | –4 |
| 3.0-V LVCMOS *(3)* | 2.85 | 3.0 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5-V LVTTL and LVCMOS *(3)* | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2.0 | 1 | –1 |
| 1.8-V LVTTL and LVCMOS | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | 2.25 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5-V LVCMOS | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |
| 1.2-V LVCMOS | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |
| 3.0-V PCI | 2.85 | 3.0 | 3.15 | — | 0.3 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 * $V_{CCIO}$ | 0.9 * $V_{CCIO}$ | 1.5 | –0.5 |
| 3.0-V PCI-X | 2.85 | 3.0 | 3.15 | — | 0.35* $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 * $V_{CCIO}$ | 0.9 * $V_{CCIO}$ | 1.5 | –0.5 |

**Notes to Table 1–13:**

(1) For voltage referenced receiver input waveform and explanation of terms used in Table 1–13, refer to "Single-ended Voltage referenced I/O Standard" in "Glossary" on page 1–27.

(2) AC load CL = 10 pF.

(3) For more detail about interfacing Cyclone III devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards, refer to *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL and LVCMOS I/O Systems*.

**Table 1–14. Cyclone III Devices Single-Ended SSTL and HSTL I/O Reference Voltage Specifications** *(1)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) *(2)* | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 1.19 | 1.25 | 1.31 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | 0.85 | 0.9 | 0.95 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.71 | 0.75 | 0.79 | 0.71 | 0.75 | 0.79 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.48 * $V_{CCIO}$ *(3)*<br>0.47 * $V_{CCIO}$ *(4)* | 0.5 * $V_{CCIO}$ *(3)*<br>0.5 * $V_{CCIO}$ *(4)* | 0.52 * $V_{CCIO}$ *(3)*<br>0.53 * $V_{CCIO}$ *(4)* | — | 0.5 * $V_{CCIO}$ | — |

**Notes to Table 1–14:**

(1) For an explanation of terms used in Table 1–14, refer to "Glossary" on page 1–27.
(2) $V_{TT}$ of transmitting device must track $V_{REF}$ of the receiving device.
(3) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.
(4) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

**Table 1–15. Cyclone III Devices Single-Ended SSTL and HSTL I/O Standards Signal Specifications**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | | $V_{IH(AC)}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Max | Min | | |
| SSTL-2 Class I | — | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | — | — | $V_{REF}$ – 0.35 | $V_{REF}$ + 0.35 | — | $V_{TT}$ – 0.57 | $V_{TT}$ + 0.57 | 8.1 | –8.1 |
| SSTL-2 Class II | — | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | — | — | $V_{REF}$ – 0.35 | $V_{REF}$ + 0.35 | — | $V_{TT}$ – 0.76 | $V_{TT}$ + 0.76 | 16.4 | –16.4 |
| SSTL-18 Class I | — | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | — | — | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | — | $V_{TT}$ – 0.475 | $V_{TT}$ + 0.475 | 6.7 | –6.7 |
| SSTL-18 Class II | — | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | — | — | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | — | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | –0.24 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.24 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | –0.24 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.24 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 14 | –14 |

For more illustrations of receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *High-Speed Differential Interfaces in Cyclone III Devices* chapter.

**Table 1–16. Cyclone III Devices Differential SSTL I/O Standard Specifications** *(1)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{Swing(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{Swing(AC)}$ (V) | | $V_{OX(AC)}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.36 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.2$ | — | $V_{CCIO}/2 + 0.2$ | 0.7 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.125$ | — | $V_{CCIO}/2 + 0.125$ |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.90 | 0.25 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.175$ | — | $V_{CCIO}/2 + 0.175$ | 0.5 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.125$ | — | $V_{CCIO}/2 + 0.125$ |

**Note to Table 1–16:**

(1) Differential SSTL requires a $V_{REF}$ input.

**Table 1–17. Cyclone III Devices Differential HSTL I/O Standard Specifications** *(1)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.85 | — | 0.95 | 0.85 | — | 0.95 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.71 | — | 0.79 | 0.71 | — | 0.79 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ | 0.48 * $V_{CCIO}$ | — | 0.52 * $V_{CCIO}$ | 0.48 * $V_{CCIO}$ | — | 0.52 * $V_{CCIO}$ | 0.3 | 0.48 * $V_{CCIO}$ |

**Note to Table 1–17:**

(1) Differential HSTL requires a $V_{REF}$ input.

**Table 1–18. Cyclone III Devices Differential I/O Standard Specifications** *(1)* **(Part 1 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | $V_{ICM}$ (V) *(2)* | | | $V_{OD}$ (mV) *(3)* | | | $V_{OS}$ (V) *(3)* | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| LVPECL (Row I/Os) *(4)* | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | | | | | | |
| LVPECL (Column I/Os) *(4)* | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | | | | | | |
| LVDS (Row I/Os) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | 247 | — | 600 | 1.125 | 1.25 | 1.375 |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | | | | | | |

**Table 1–18. Cyclone III Devices Differential I/O Standard Specifications (1) (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | $V_{IcM}$ (V) (2) | | | $V_{OD}$ (mV) (3) | | | $V_{OS}$ (V) (3) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| LVDS (Column I/Os) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | 247 | — | 600 | 1.125 | 1.25 | 1.375 |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | | | | | | |
| BLVDS (Row I/Os) (5) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |
| BLVDS (Column I/Os) (5) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |
| mini-LVDS (Row I/Os) (6) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1.0 | 1.2 | 1.4 |
| mini-LVDS (Column I/Os) (6) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1.0 | 1.2 | 1.4 |
| RSDS® (Row I/Os) (6) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 |
| RSDS (Column I/Os) (6) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 |
| PPDS® (Row I/Os) (6) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 |
| PPDS (Column I/Os) (6) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 |

**Notes to Table 1–18:**

(1) For an explanation of terms used in Table 1–18, refer to "Transmitter Output Waveform" in "Glossary" on page 1–27.
(2) $V_{IN}$ range: 0 V $\leq V_{IN} \leq$ 1.85 V.
(3) $R_L$ range: 90 $\leq R_L \leq$ 110 Ω.
(4) LVPECL input standard is only supported at clock input. Output standard is not supported.
(5) No fixed $V_{IN}$, $V_{OD}$, and $V_{OS}$ specifications for BLVDS. They are dependent on the system topology.
(6) Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins for Cyclone III devices.

## Power Consumption

You can use the following methods to estimate power for a design:

- the Excel-based EPE.
- the Quartus II PowerPlay power analyzer feature.

The interactive Excel-based EPE is used prior to designing the device to get a magnitude estimate of the device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay power analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

# Switching Characteristics

This section provides the performance characteristics of the core and periphery blocks for Cyclone III devices. All data is final and is based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

## Core Performance Specifications

### Clock Tree Specifications

Table 1–19 lists the clock tree specifications for Cyclone III devices.

**Table 1–19. Cyclone III Devices Clock Tree Performance**

| Device | Performance | | | Unit |
|---|---|---|---|---|
| | C6 | C7 | C8 | |
| EP3C5 | 500 | 437.5 | 402 | MHz |
| EP3C10 | 500 | 437.5 | 402 | MHz |
| EP3C16 | 500 | 437.5 | 402 | MHz |
| EP3C25 | 500 | 437.5 | 402 | MHz |
| EP3C40 | 500 | 437.5 | 402 | MHz |
| EP3C55 | 500 | 437.5 | 402 | MHz |
| EP3C80 | 500 | 437.5 | 402 | MHz |
| EP3C120 | (1) | 437.5 | 402 | MHz |

**Note to Table 1–19:**

(1) EP3C120 offered in C7, C8, and I7 grades only.

## PLL Specifications

Table 1–20 describes the PLL specifications for Cyclone III devices when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), and the automotive junction temperature range (–40°Cto 125°C). For more information about PLL block, refer to "PLL Block" in "Glossary" on page 1–27.

**Table 1–20. Cyclone III Devices PLL Specifications (1) (Part 1 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ (2) | Input clock frequency | 5 | — | 472.5 | MHz |
| $f_{INPFD}$ | PFD input frequency | 5 | — | 325 | MHz |
| $f_{VCO}$ (3) | PLL internal VCO operating range | 600 | — | 1300 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | — | 60 | % |
| $t_{INJITTER_CCJ}$ (4) | Input clock cycle-to-cycle jitter for $F_{INPFD} \geq 100$ MHz | — | — | 0.15 | UI |
| | Input clock cycle-to-cycle jitter for $F_{INPFD} < 100$ MHz | — | — | ±750 | ps |
| $f_{OUT_EXT}$ (external clock output) (2) | PLL output frequency | — | — | 472.5 | MHz |
| $f_{OUT}$ (to global clock) | PLL output frequency (–6 speed grade) | — | — | 472.5 | MHz |
| | PLL output frequency (–7 speed grade) | — | — | 450 | MHz |
| | PLL output frequency (–8 speed grade) | — | — | 402.5 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| $t_{LOCK}$ | Time required to lock from end of device configuration | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted) | — | — | 1 | ms |
| $t_{OUTJITTER_PERIOD_DEDCLK}$ (5) | Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER_CCJ_DEDCLK}$ (5) | Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER_PERIOD_IO}$ (5) | Regular I/O period jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{OUTJITTER_CCJ_IO}$ (5) | Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{PLL_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on areset signal. | 10 | — | — | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chains for PLLs | — | 3.5 (6) | — | SCANCLK cycles |

**Table 1–20. Cyclone III Devices PLL Specifications (1) (Part 2 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCANCLK}$ | scanclk frequency | — | — | 100 | MHz |

**Notes to Table 1–20:**

(1) $V_{CCD_PLL}$ should always be connected to $V_{CCINT}$ through decoupling capacitor and ferrite bead.
(2) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
(3) The $V_{CO}$ frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the $V_{CO}$ post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.
(4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.
(5) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.
(6) With 100 MHz scanclk frequency.

## Embedded Multiplier Specifications

Table 1–21 describes the embedded multiplier specifications for Cyclone III devices.

**Table 1–21. Cyclone III Devices Embedded Multiplier Specifications**

| Mode | Resources Used | Performance | | | Unit |
|---|---|---|---|---|---|
| | Number of Multipliers | C6 | C7, I7, A7 | C8 | |
| 9 × 9-bit multiplier | 1 | 340 | 300 | 260 | MHz |
| 18 × 18-bit multiplier | 1 | 287 | 250 | 200 | MHz |

## Memory Block Specifications

Table 1–22 describes the M9K memory block specifications for Cyclone III devices.

**Table 1–22. Cyclone III Devices Memory Block Performance Specifications**

| Memory | Mode | Resources Used | | Performance | | | |
|---|---|---|---|---|---|---|---|
| | | LEs | M9K Memory | C6 | C7, I7, A7 | C8 | Unit |
| M9K Block | FIFO 256 × 36 | 47 | 1 | 315 | 274 | 238 | MHz |
| | Single-port 256 × 36 | 0 | 1 | 315 | 274 | 238 | MHz |
| | Simple dual-port 256 × 36 CLK | 0 | 1 | 315 | 274 | 238 | MHz |
| | True dual port 512 × 18 single CLK | 0 | 1 | 315 | 274 | 238 | MHz |

## Configuration and JTAG Specifications

Table 1–23 lists the configuration mode specifications for Cyclone III devices.

**Table 1–23. Cyclone III Devices Configuration Mode Specifications**

| Programming Mode | DCLK $F_{max}$ | Unit |
|---|---|---|
| Passive Serial (PS) | 133 | MHz |
| Fast Passive Parallel (FPP) (1) | 100 | MHz |

**Note to Table 1–23:**

(1) EP3C40 and smaller density members support 133 MHz.

Table 1–24 lists the active configuration mode specifications for Cyclone III devices.

**Table 1–24. Cyclone III Devices Active Configuration Mode Specifications**

| Programming Mode | DCLK Range | Unit |
|---|---|---|
| Active Parallel (AP) | 20 – 40 | MHz |
| Active Serial (AS) | 20 – 40 | MHz |

Table 1–25 lists the JTAG timing parameters and values for Cyclone III devices.

**Table 1–25. Cyclone III Devices JTAG Timing Parameters** *(1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 40 | — | ns |
| $t_{JCH}$ | TCK clock high time | 20 | — | ns |
| $t_{JCL}$ | TCK clock low time | 20 | — | ns |
| $t_{JPSU_TDI}$ | JTAG port setup time for TDI | 1 | — | ns |
| $t_{JPSU_TMS}$ | JTAG port setup time for TMS | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 10 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output *(2)* | — | 15 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output *(2)* | — | 15 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance *(2)* | — | 15 | ns |
| $t_{JSSU}$ | Capture register setup time | 5 | — | ns |
| $t_{JSH}$ | Capture register hold time | 10 | — | ns |
| $t_{JSCO}$ | Update register clock to output | — | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | — | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | — | 25 | ns |

**Notes to Table 1–25:**

(1) For more information about JTAG waveforms, refer to "JTAG Waveform" in "Glossary" on page 1–27.

(2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the JTAG port clock to output time is 16 ns.

## Periphery Performance

This section describes periphery performance, including high-speed I/O, external memory interface, and IOE programmable delay.

I/O performance supports several system interfacing, for example, the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/O using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds with typical DDR SDRAM memory interface setup. I/O using general-purpose I/O standards such as 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.



Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

Table 1–26 through Table 1–31 list the high-speed I/O timing for Cyclone III devices. For definitions of high-speed timing specifications, refer to "Glossary" on page 1–27.

**Table 1–26. Cyclone III Devices RSDS Transmitter Timing Specifications** *(1), (2)*

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×8 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×7 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×4 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×2 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×1 | 5 | — | 360 | 5 | — | 311 | 5 | — | 311 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 360 | 100 | — | 311 | 100 | — | 311 | Mbps |
| | ×8 | 80 | — | 360 | 80 | — | 311 | 80 | — | 311 | Mbps |
| | ×7 | 70 | — | 360 | 70 | — | 311 | 70 | — | 311 | Mbps |
| | ×4 | 40 | — | 360 | 40 | — | 311 | 40 | — | 311 | Mbps |
| | ×2 | 20 | — | 360 | 20 | — | 311 | 20 | — | 311 | Mbps |
| | ×1 | 10 | — | 360 | 10 | — | 311 | 10 | — | 311 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ *(3)* | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–26:**

(1) Applicable for true RSDS and emulated RSDS_E_3R transmitter.

(2) True RSDS transmitter is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6). Emulated RSDS transmitter is supported at the output pin of all I/O banks.

(3) $t_{LOCK}$ is the time required for the PLL to lock from the end of device configuration.

**Table 1–27. Cyclone III Devices Emulated RSDS_E_1R Transmitter Timing Specifications** *(1)* **(Part 1 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | ×8 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | ×7 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | ×4 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | ×2 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | ×1 | 5 | — | 170 | 5 | — | 170 | 5 | — | 170 | MHz |

**Table 1–27. Cyclone III Devices Emulated RSDS_E_1R Transmitter Timing Specifications (1) (Part 2 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Device operation in Mbps | ×10 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | Mbps |
| | ×8 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | Mbps |
| | ×7 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | Mbps |
| | ×4 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | Mbps |
| | ×2 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | Mbps |
| | ×1 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ (2) | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–27:**

(1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O banks.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end of device configuration.

**Table 1–28. Cyclone III Devices Mini-LVDS Transmitter Timing Specifications (1), (2) (Part 1 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×8 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×7 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×4 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×2 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | MHz |
| | ×1 | 5 | — | 400 | 5 | — | 311 | 5 | — | 311 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 400 | 100 | — | 311 | 100 | — | 311 | Mbps |
| | ×8 | 80 | — | 400 | 80 | — | 311 | 80 | — | 311 | Mbps |
| | ×7 | 70 | — | 400 | 70 | — | 311 | 70 | — | 311 | Mbps |
| | ×4 | 40 | — | 400 | 40 | — | 311 | 40 | — | 311 | Mbps |
| | ×2 | 20 | — | 400 | 20 | — | 311 | 20 | — | 311 | Mbps |
| | ×1 | 10 | — | 400 | 10 | — | 311 | 10 | — | 311 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | ps |

**Table 1–28. Cyclone III Devices Mini-LVDS Transmitter Timing Specifications (1), (2) (Part 2 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ (3) | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–28:**

(1) Applicable for true and emulated mini-LVDS transmitter.

(2) True mini-LVDS transmitter is only supported at the output pin of Row I/O (Banks 1, 2, 5, and 6). Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.

(3) $t_{LOCK}$ is the time required for the PLL to lock from the end of device configuration.

**Table 1–29. Cyclone III Devices True LVDS Transmitter Timing Specifications** *(1)*

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | 420 | 5 | 370 | 5 | 320 | MHz |
| | ×8 | 5 | 420 | 5 | 370 | 5 | 320 | MHz |
| | ×7 | 5 | 420 | 5 | 370 | 5 | 320 | MHz |
| | ×4 | 5 | 420 | 5 | 370 | 5 | 320 | MHz |
| | ×2 | 5 | 420 | 5 | 370 | 5 | 320 | MHz |
| | ×1 | 5 | 420 | 5 | 402.5 | 5 | 402.5 | MHz |
| HSIODR | ×10 | 100 | 840 | 100 | 740 | 100 | 640 | Mbps |
| | ×8 | 80 | 840 | 80 | 740 | 80 | 640 | Mbps |
| | ×7 | 70 | 840 | 70 | 740 | 70 | 640 | Mbps |
| | ×4 | 40 | 840 | 40 | 740 | 40 | 640 | Mbps |
| | ×2 | 20 | 840 | 20 | 740 | 20 | 640 | Mbps |
| | ×1 | 10 | 420 | 10 | 402.5 | 10 | 402.5 | Mbps |
| $t_{DUTY}$ | — | 45 | 55 | 45 | 55 | 45 | 55 | % |
| TCCS | — | — | 200 | — | 200 | — | 200 | ps |
| Output jitter (peak to peak) | — | — | 500 | — | 500 | — | 550 | ps |
| $t_{LOCK}$ *(2)* | — | — | 1 | — | 1 | — | 1 | ms |

**Notes to Table 1–29:**

(1) True LVDS transmitter is only supported at the output pin of Row I/O (Banks 1, 2, 5, and 6).

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end of device configuration.

**Table 1–30. Cyclone III Devices Emulated LVDS Transmitter Timing Specifications** *(1)* **(Part 1 of 2)**

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | 320 | 5 | 320 | 5 | 275 | MHz |
| | ×8 | 5 | 320 | 5 | 320 | 5 | 275 | MHz |
| | ×7 | 5 | 320 | 5 | 320 | 5 | 275 | MHz |
| | ×4 | 5 | 320 | 5 | 320 | 5 | 275 | MHz |
| | ×2 | 5 | 320 | 5 | 320 | 5 | 275 | MHz |
| | ×1 | 5 | 402.5 | 5 | 402.5 | 5 | 402.5 | MHz |
| HSIODR | ×10 | 100 | 640 | 100 | 640 | 100 | 550 | Mbps |
| | ×8 | 80 | 640 | 80 | 640 | 80 | 550 | Mbps |
| | ×7 | 70 | 640 | 70 | 640 | 70 | 550 | Mbps |
| | ×4 | 40 | 640 | 40 | 640 | 40 | 550 | Mbps |
| | ×2 | 20 | 640 | 20 | 640 | 20 | 550 | Mbps |
| | ×1 | 10 | 402.5 | 10 | 402.5 | 10 | 402.5 | Mbps |
| $t_{DUTY}$ | — | 45 | 55 | 45 | 55 | 45 | 55 | % |
| TCCS | — | — | 200 | — | 200 | — | 200 | ps |

**Table 1–30. Cyclone III Devices Emulated LVDS Transmitter Timing Specifications (1) (Part 2 of 2)**

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Output jitter (peak to peak) | — | — | 500 | — | 500 | — | 550 | ps |
| $t_{LOCK}$ (2) | — | — | 1 | — | 1 | — | 1 | ms |

**Notes to Table 1–30:**

(1) Emulated LVDS transmitter is supported at the output pin of all I/O banks.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end of device configuration.

**Table 1–31. Cyclone III Devices LVDS Receiver Timing Specifications (1)**

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | 437.5 | 5 | 370 | 5 | 320 | MHz |
| | ×8 | 5 | 437.5 | 5 | 370 | 5 | 320 | MHz |
| | ×7 | 5 | 437.5 | 5 | 370 | 5 | 320 | MHz |
| | ×4 | 5 | 437.5 | 5 | 370 | 5 | 320 | MHz |
| | ×2 | 5 | 437.5 | 5 | 370 | 5 | 320 | MHz |
| | ×1 | 5 | 437.5 | 5 | 402.5 | 5 | 402.5 | MHz |
| HSIODR | ×10 | 100 | 875 | 100 | 740 | 100 | 640 | Mbps |
| | ×8 | 80 | 875 | 80 | 740 | 80 | 640 | Mbps |
| | ×7 | 70 | 875 | 70 | 740 | 70 | 640 | Mbps |
| | ×4 | 40 | 875 | 40 | 740 | 40 | 640 | Mbps |
| | ×2 | 20 | 875 | 20 | 740 | 20 | 640 | Mbps |
| | ×1 | 10 | 437.5 | 10 | 402.5 | 10 | 402.5 | Mbps |
| SW | — | — | 400 | — | 400 | — | 400 | ps |
| Input jitter tolerance | — | — | 500 | — | 500 | — | 550 | ps |
| $t_{LOCK}$ (2) | — | — | 1 | — | 1 | — | 1 | ms |

**Notes to Table 1–31:**

(1) LVDS receiver is supported at all banks.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end of device configuration.

## External Memory Interface Specifications

Cyclone III devices support external memory interfaces up to 200 MHz. The external memory interfaces for Cyclone III devices are auto-calibrating and easy to implement.

For more information about external memory system performance specifications, board design guidelines, timing analysis, simulation, and debugging information, refer to *Literature: External Memory Interfaces*.

Table 1–32 lists the FPGA sampling window specifications for Cyclone III devices.

**Table 1–32. Cyclone III Devices FPGA Sampling Window (SW) Requirement – Read Side (1)**

| Memory Standard | Column I/Os | | Row I/Os | | Wraparound Mode | |
|---|---|---|---|---|---|---|
| | Setup | Hold | Setup | Hold | Setup | Hold |
| *C6* | | | | | | |
| DDR2 SDRAM | 580 | 550 | 690 | 640 | 850 | 800 |
| DDR SDRAM | 585 | 535 | 700 | 650 | 870 | 820 |
| QDRII SRAM | 785 | 735 | 805 | 755 | 905 | 855 |
| *C7* | | | | | | |
| DDR2 SDRAM | 705 | 650 | 770 | 715 | 985 | 930 |
| DDR SDRAM | 675 | 620 | 795 | 740 | 970 | 915 |
| QDRII SRAM | 900 | 845 | 910 | 855 | 1085 | 1030 |
| *C8* | | | | | | |
| DDR2 SDRAM | 785 | 720 | 930 | 870 | 1115 | 1055 |
| DDR SDRAM | 800 | 740 | 915 | 855 | 1185 | 1125 |
| QDRII SRAM | 1050 | 990 | 1065 | 1005 | 1210 | 1150 |
| *I7* | | | | | | |
| DDR2 SDRAM | 765 | 710 | 855 | 800 | 1040 | 985 |
| DDR SDRAM | 745 | 690 | 880 | 825 | 1000 | 945 |
| QDRII SRAM | 945 | 890 | 955 | 900 | 1130 | 1075 |
| *A7* | | | | | | |
| DDR2 SDRAM | 805 | 745 | 1020 | 960 | 1145 | 1085 |
| DDR SDRAM | 880 | 820 | 955 | 935 | 1220 | 1160 |
| QDRII SRAM | 1090 | 1030 | 1105 | 1045 | 1250 | 1190 |

**Note to Table 1–32:**

(1) Column I/Os refer to top and bottom I/Os. Row I/Os refer to right and left I/Os. Wraparound mode refers to the combination of column and row I/Os.

Table 1–33 lists the transmitter channel-to-channel skew specifications for Cyclone III devices.

**Table 1–33. Cyclone III Devices Transmitter Channel-to-Channel Skew (TCCS) – Write Side (1) (Part 1 of 2)**

| Memory Standard | I/O Standard | Column I/Os (ps) | | Row I/Os (ps) | | Wraparound Mode (ps) | |
|---|---|---|---|---|---|---|---|
| | | Lead | Lag | Lead | Lag | Lead | Lag |
| *C6* | | | | | | | |
| DDR2 SDRAM | SSTL-18 Class I | 790 | 380 | 790 | 380 | 890 | 480 |
| | SSTL-18 Class II | 870 | 490 | 870 | 490 | 970 | 590 |
| DDR SDRAM | SSTL-2 Class I | 750 | 320 | 750 | 320 | 850 | 420 |
| | SSTL-2 Class II | 860 | 350 | 860 | 350 | 960 | 450 |
| QDRII SRAM | 1.8 V HSTL Class I | 780 | 410 | 780 | 410 | 880 | 510 |
| | 1.8 V HSTL Class II | 830 | 510 | 830 | 510 | 930 | 610 |
| *C7* | | | | | | | |

**Table 1–33. Cyclone III Devices Transmitter Channel-to-Channel Skew (TCCS) – Write Side (1) (Part 2 of 2)**

| Memory Standard | I/O Standard | Column I/Os (ps) | | Row I/Os (ps) | | Wraparound Mode (ps) | |
|---|---|---|---|---|---|---|---|
| | | Lead | Lag | Lead | Lag | Lead | Lag |
| DDR2 SDRAM | SSTL-18 Class I | 915 | 410 | 915 | 410 | 1015 | 510 |
| | SSTL-18 Class II | 1025 | 545 | 1025 | 545 | 1125 | 645 |
| DDR SDRAM | SSTL-2 Class I | 880 | 340 | 880 | 340 | 980 | 440 |
| | SSTL-2 Class II | 1010 | 380 | 1010 | 380 | 1110 | 480 |
| QDRII SRAM | 1.8 V HSTL Class I | 910 | 450 | 910 | 450 | 1010 | 550 |
| | 1.8 V HSTL Class II | 1010 | 570 | 1010 | 570 | 1110 | 670 |
| *C8* | | | | | | | |
| DDR2 SDRAM | SSTL-18 Class I | 1040 | 440 | 1040 | 440 | 1140 | 540 |
| | SSTL-18 Class II | 1180 | 600 | 1180 | 600 | 1280 | 700 |
| DDR SDRAM | SSTL-2 Class I | 1010 | 360 | 1010 | 360 | 1110 | 460 |
| | SSTL-2 Class II | 1160 | 410 | 1160 | 410 | 1260 | 510 |
| QDRII SRAM | 1.8 V HSTL Class I | 1040 | 490 | 1040 | 490 | 1140 | 590 |
| | 1.8 V HSTL Class II | 1190 | 630 | 1190 | 630 | 1290 | 730 |
| *I7* | | | | | | | |
| DDR2 SDRAM | SSTL-18 Class I | 961 | 431 | 961 | 431 | 1061 | 531 |
| | SSTL-18 Class II | 1076 | 572 | 1076 | 572 | 1176 | 672 |
| DDR SDRAM | SSTL-2 Class I | 924 | 357 | 924 | 357 | 1024 | 457 |
| | SSTL-2 Class II | 1061 | 399 | 1061 | 399 | 1161 | 499 |
| QDRII SRAM | 1.8 V HSTL Class I | 956 | 473 | 956 | 473 | 1056 | 573 |
| | 1.8 V HSTL Class II | 1061 | 599 | 1061 | 599 | 1161 | 699 |
| *A7* | | | | | | | |
| DDR2 SDRAM (2) | SSTL-18 Class I | 1092 | 462 | 1092 | 462 | 1192 | 562 |
| | SSTL-18 Class II | 1239 | 630 | 1239 | 630 | 1339 | 730 |
| DDR SDRAM | SSTL-2 Class I | 1061 | 378 | 1061 | 378 | 1161 | 478 |
| | SSTL-2 Class II | 1218 | 431 | 1218 | 431 | 1318 | 531 |
| QDRII SRAM | 1.8 V HSTL Class I | 1092 | 515 | 1092 | 515 | 1192 | 615 |
| | 1.8 V HSTL Class II | 1250 | 662 | 1250 | 662 | 1350 | 762 |

**Notes to Table 1–33:**

(1) Column I/O banks refer to top and bottom I/Os. Row I/O banks refer to right and left I/Os. Wraparound mode refers to the combination of column and row I/Os.

(2) For DDR2 SDRAM write timing performance on Columns I/O for C8 and A7 devices, 97.5 degree phase offset is required.

Table 1–34 lists the memory output clock jitter specifications for Cyclone III devices.

**Table 1–34. Cyclone III Devices Memory Output Clock Jitter Specifications (1), (2) (Part 1 of 2)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Clock period jitter | $t_{JIT(per)}$ | -125 | 125 | ps |
| Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | -200 | 200 | ps |

**Table 1–34. Cyclone III Devices Memory Output Clock Jitter Specifications (1), (2) (Part 2 of 2)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Duty cycle jitter | $t_{JIT(duty)}$ | -150 | 150 | ps |

**Notes to Table 1–34:**

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock network.

## Duty Cycle Distortion Specifications

Table 1–35 lists the worst case duty cycle distortion for Cyclone III devices.

**Table 1–35. Duty Cycle Distortion on Cyclone III Devices I/O Pins (1), (2)**

| Symbol | C6 | | C7, I7 | | C8, A7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

**Notes to Table 1–35:**

(1) Duty cycle distortion specification applies to clock outputs from PLLs, global clock tree, and IOE driving dedicated and general purpose I/O pins.

(2) Cyclone III devices meet specified duty cycle distortion at maximum output toggle rate for each combination of I/O standard and current strength.

## OCT Calibration Timing Specification

Table 1–36 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone III devices.

**Table 1–36. Cyclone III Devices Timing Specification for Series OCT with Calibration at Device Power-Up (1)**

| Symbol | Description | Maximum | Unit |
|---|---|---|---|
| $t_{OCTCAL}$ | Duration of series OCT with calibration at device power-up | 20 | µs |

**Notes to Table 1–36:**

(1) OCT calibration takes place after device configuration, before entering user mode.

## IOE Programmable Delay

Table 1–37 and Table 1–38 list IOE programmable delay for Cyclone III devices.

**Table 1–37. Cyclone III Devices IOE Programmable Delay on Column Pins (1), (2) (Part 1 of 2)**

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | | |
| | | | | A7, I7 | C6 | C6 | C7 | C8 | I7 | A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.211 | 1.314 | 2.175 | 2.32 | 2.386 | 2.366 | 2.49 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.203 | 1.307 | 2.19 | 2.387 | 2.54 | 2.43 | 2.545 | ns |

**Table 1–37. Cyclone III Devices IOE Programmable Delay on Column Pins (1), (2) (Part 2 of 2)**

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | | |
| | | | | A7, I7 | C6 | C6 | C7 | C8 | I7 | A7 | |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.479 | 0.504 | 0.915 | 1.011 | 1.107 | 1.018 | 1.048 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.664 | 0.694 | 1.199 | 1.378 | 1.532 | 1.392 | 1.441 | ns |

**Notes to Table 1–37:**

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Quartus II software.

**Table 1–38. Cyclone III Devices IOE Programmable Delay on Row Pins (1), (2)**

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | | |
| | | | | A7, I7 | C6 | C6 | C7 | C8 | I7 | A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.209 | 1.314 | 2.174 | 2.335 | 2.406 | 2.381 | 2.505 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.207 | 1.312 | 2.202 | 2.402 | 2.558 | 2.447 | 2.557 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.51 | 0.537 | 0.962 | 1.072 | 1.167 | 1.074 | 1.101 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.669 | 0.698 | 1.207 | 1.388 | 1.542 | 1.403 | 1.45 | ns |

**Notes to Table 1–38:**

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Quartus II software

# I/O Timing

You can use the following methods to determine the I/O timing:

- the Excel-based I/O Timing.
- the Quartus II timing analyzer.

The Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Excel-based I/O Timing spreadsheet is downloadable from Cyclone III Devices Literature website.

# Glossary

Table 1–39 lists the glossary for this chapter.

**Table 1–39. Glossary (Part 1 of 5)**

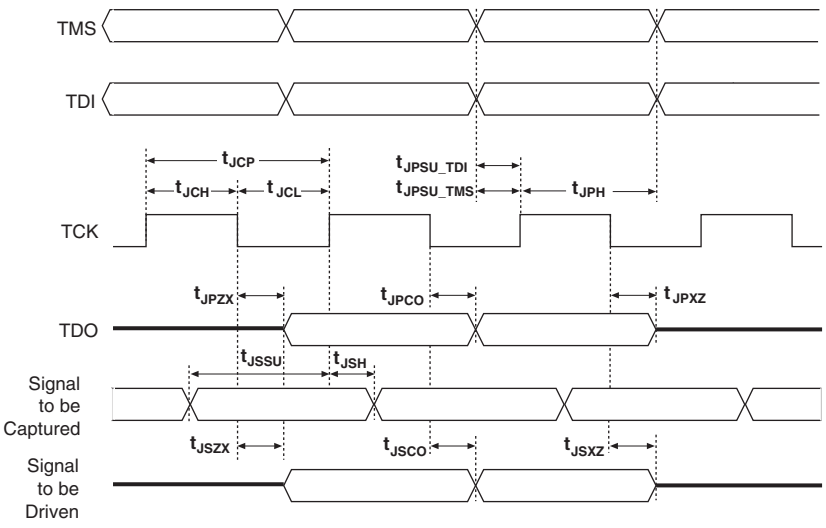
| Letter | Term | Definitions |
|---|---|---|
| A | — | — |
| B | — | — |
| C | — | — |
| D | — | — |
| E | — | — |
| F | $f_{HSCLK}$ | HIGH-SPEED I/O Block: High-speed receiver/transmitter input and output clock frequency. |
| G | GCLK | Input pin directly to Global Clock network. |
| | GCLK PLL | Input pin to Global Clock network through PLL. |
| H | HSIODR | HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI). |
| I | Input Waveforms for the SSTL Differential I/O Standard |  |
| J | JTAG Waveform |  |
| K | — | — |
| L | — | — |
| M | — | — |

**Table 1–39. Glossary (Part 2 of 5)**

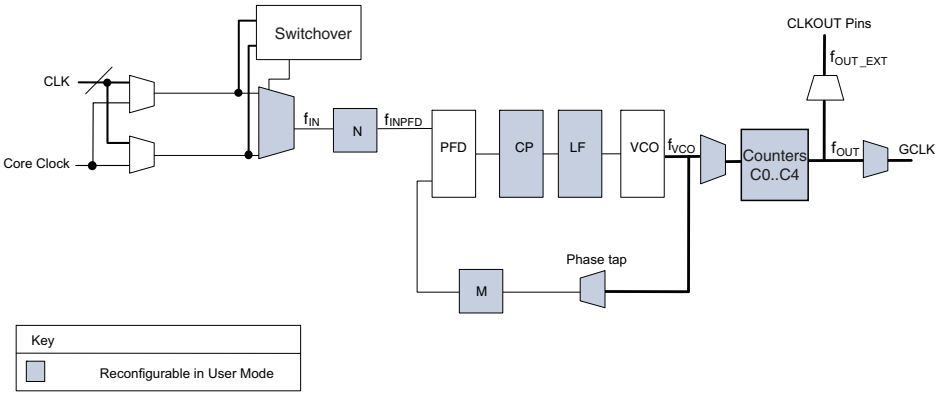
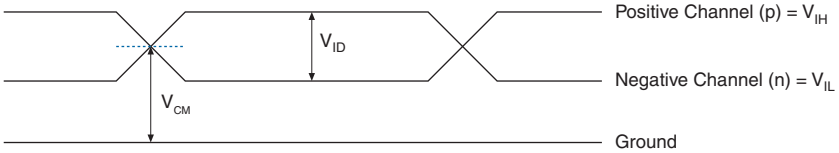
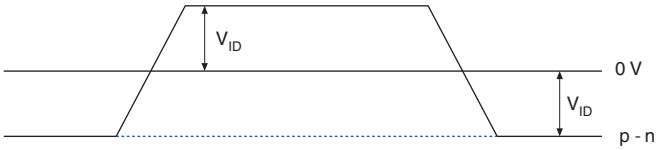
| Letter | Term | Definitions |
|---|---|---|
| N | — | — |
| O | — | — |
| P | PLL Block | The following block diagram highlights the PLL Specification parameters.<br> |
| Q | — | — |
| R | $R_L$ | Receiver differential input discrete resistor (external to Cyclone III devices). |
| | Receiver Input Waveform | Receiver Input Waveform for LVDS and LVPECL Differential Standards.<br>**Single-Ended Waveform**<br><br>**Differential Waveform (Mathematical Function of Positive & Negative Channel)**<br> |
| | RSKM (Receiver input skew margin) | HIGH-SPEED I/O Block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2. |

**Table 1–39. Glossary (Part 3 of 5)**

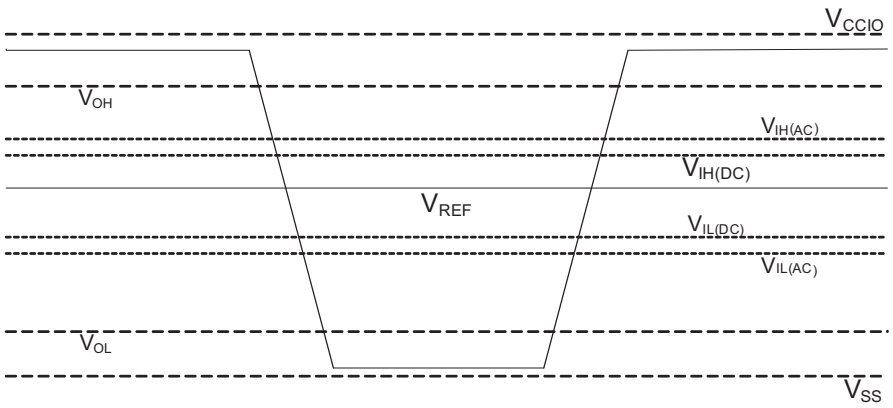
| Letter | Term | Definitions |
|---|---|---|
| S | Single-ended Voltage referenced I/O Standard | <br>The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform *ringing*. |
| | SW (Sampling Window) | HIGH-SPEED I/O Block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. |
| T | $t_C$ | High-speed receiver/transmitter input and output clock period. |
| | TCCS (Channel-to-channel-skew) | HIGH-SPEED I/O Block: The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew. The clock is included in the TCCS measurement. |
| | tcin | Delay from clock pad to I/O input register. |
| | $t_{CO}$ | Delay from clock pad to I/O output. |
| | tcout | Delay from clock pad to I/O output register. |
| | $t_{DUTY}$ | HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock. |
| | $t_{FALL}$ | Signal High-to-low transition time (80–20%). |
| | $t_H$ | Input register hold time. |
| | Timing Unit Interval (TUI) | HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = $t_C$/w). |
| | $t_{INJITTER}$ | Period jitter on PLL clock input. |
| | $t_{OUTJITTER_DEDCLK}$ | Period jitter on dedicated clock output driven by a PLL. |
| | $t_{OUTJITTER_IO}$ | Period jitter on general purpose I/O driven by a PLL. |
| | tpllcin | Delay from PLL inclk pad to I/O input register. |
| | tpllcout | Delay from PLL inclk pad to I/O output register. |

**Table 1–39. Glossary (Part 4 of 5)**

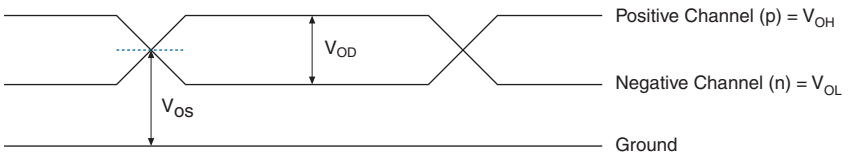
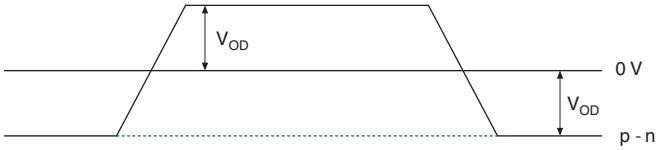
| Letter | Term | Definitions |
|---|---|---|
| | Transmitter Output Waveform | Transmitter Output Waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards<br>**Single-Ended Waveform**<br><br><br>**Differential Waveform (Mathematical Function of Positive & Negative Channel)**<br><br> |
| | $t_{RISE}$ | Signal Low-to-high transition time (20–80%). |
| | $t_{SU}$ | Input register setup time. |
| **U** | — | — |

**Table 1–39. Glossary (Part 5 of 5)**

| Letter | Term | Definitions |
|---|---|---|
| V | $V_{CM(DC)}$ | DC Common Mode Input Voltage. |
| | $V_{DIF(AC)}$ | AC differential Input Voltage: The minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential Input Voltage: The minimum DC input differential voltage required for switching. |
| | $V_{ICM}$ | Input Common Mode Voltage: The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{IH}$ | Voltage Input High: The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage. |
| | $V_{IH(DC)}$ | High-level DC input voltage. |
| | $V_{IL}$ | Voltage Input Low: The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL\ (AC)}$ | Low-level AC input voltage. |
| | $V_{IL\ (DC)}$ | Low-level DC input voltage. |
| | $V_{IN}$ | DC input voltage. |
| | $V_{OCM}$ | Output Common Mode Voltage: The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$. |
| | $V_{OH}$ | Voltage Output High: The maximum positive voltage from an output which the device considers is accepted as the minimum positive high level. |
| | $V_{OL}$ | Voltage Output Low: The maximum positive voltage from an output which the device considers is accepted as the maximum positive low level. |
| | $V_{OS}$ | Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$. |
| | $V_{OX\ (AC)}$ | AC differential Output cross point voltage: The voltage at which the differential output signals must cross. |
| | $V_{REF}$ | Reference voltage for SSTL, HSTL I/O Standards. |
| | $V_{REF\ (AC)}$ | AC input reference voltage for SSTL, HSTL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on $V_{REF}$ should not exceed 2% of $V_{REF(DC)}$. |
| | $V_{REF\ (DC)}$ | DC input reference voltage for SSTL, HSTL I/O Standards. |
| | $V_{SWING\ (AC)}$ | AC differential Input Voltage: AC Input differential voltage required for switching. For the SSTL Differential I/O Standard, refer to Input Waveforms. |
| | $V_{SWING\ (DC)}$ | DC differential Input Voltage: DC Input differential voltage required for switching. For the SSTL Differential I/O Standard, refer to Input Waveforms. |
| | $V_{TT}$ | Termination voltage for SSTL, HSTL I/O Standards. |
| | $V_{X\ (AC)}$ | AC differential Input cross point Voltage: The voltage at which the differential input signals must cross. |
| W | — | — |
| X | — | — |
| Y | — | — |
| Z | — | — |

# Document Revision History

Table 1–40 lists the revision history for this document.

**Table 1–40. Document Revision History (Part 1 of 3)**

| Date | Version | Changes |
|---|---|---|
| July 2012 | 3.5 | Updated minimum $f_{HSCLK}$ value to 5 MHz. |
| December 2011 | 3.4 | ■ Updated "Supply Current" on page 1–5 and "Periphery Performance" on page 1–17.<br>■ Updated Table 1–3, Table 1–4, Table 1–13, Table 1–16, Table 1–17, Table 1–20, and Table 1–25. |
| January 2010 | 3.3 | ■ Removed Table 1-32 and Table 1-33.<br>■ Added *Literature: External Memory Interfaces reference*. |
| December 2009 | 3.2 | Minor changes to the text. |
| July 2009 | 3.1 | Minor edit to the hyperlinks. |
| June 2009 | 3.0 | ■ Changed chapter title from DC and Switching Characteristics to "Cyclone III Device Data Sheet" on page 1–1.<br>■ Updated *(Note 1)* to Table 1–23 on page 1–17.<br>■ Updated "External Memory Interface Specifications" on page 1–23.<br>■ Replaced Table 1–32 on page 1–23.<br>■ Replaced Table 1–33 on page 1–23.<br>■ Added Table 1–36 on page 1–26.<br>■ Updated "I/O Timing" on page 1–28.<br>■ Removed "Typical Design Performance" section.<br>■ Removed "I/O Timing" subsections. |
| October 2008 | 2.2 | ■ Updated chapter to new template.<br>■ Updated Table 1–1, Table 1–3, and Table 1–18.<br>■ Added *(Note 7)* to Table 1–3.<br>■ Added the "OCT Calibration Timing Specification" section.<br>■ Updated "Glossary" section. |
| July 2008 | 2.1 | ■ Updated Table 1–38.<br>■ Added BLVDS information (I/O standard) into Table 1–39, Table 1–40, Table 1–41, Table 1–42.<br>■ Updated Table 1–43, Table 1–46, Table 1–47, Table 1–48, Table 1–49, Table 1–50, Table 1–51, Table 1–52, Table 1–53, Table 1–54, Table 1–55, Table 1–56, Table 1–57, Table 1–58, Table 1–59, Table 1–60, Table 1–61, Table 1–62, Table 1–63, Table 1–68, Table 1–69, Table 1–74, Table 1–75, Table 1–80, Table 1–81, Table 1–86, Table 1–87, Table 1–92, Table 1–93, Table 1–94, Table 1–95, Table 1–96, Table 1–97, Table 1–98, and Table 1–99. |

**Table 1–40. Document Revision History (Part 2 of 3)**

| Date | Version | Changes |
|---|---|---|
| May 2008 | 2.0 | ■ Updated "Operating Conditions" section and included information on automotive device.<br>■ Updated Table 1–3, Table 1–6, and Table 1–7, and added automotive information.<br>■ Under "Pin Capacitance" section, updated Table 1–9 and Table 1–10.<br>■ Added new "Schmitt Trigger Input" section with Table 1–12.<br>■ Under "I/O Standard Specifications" section, updated Table 1–13, 1–12 and 1–12.<br>■ Under "Switching Characteristics" section, updated Table 1–19, 1–15, 1–16, 1–16, 1–17, 1–18, 1–19, 1–20, 1–21, 1–21, 1–23, 1–23, 1–23, 1–24, and 1–25.<br>■ Updated Figure 1–5 and 1–29.<br>■ Deleted previous Table 1-35 "DDIO Outputs Half-Period Jitter".<br>■ Under "I/O Timing" section, updated Table 1–38, 1–29, 1–32, 1–33, 1–26, and 1–26.<br>■ Under "Typical Design Performance" section updated Table 1–46 through 1–145. |
| December 2007 | 1.5 | ■ Under "Core Performance Specifications", updated Tables 1-18 and 1-19.<br>■ Under "Preliminary, Correlated, and Final Timing", updated Table 1-37.<br>■ Under "Typical Design Performance", updated Tables 1-45, 1-46, 1-51, 1-52, 1-57, 1-58, Tables 1-63 through 1-68. 1-69, 1-70, 1-75, 1-76, 1-81, 1-82, Tables 1-87 through 1-92, Tables 1-99, 1-100, 1-107, and 1-108. |
| October 2007 | 1.4 | ■ Updated the $C_{VREFTB}$ value in Table 1-9.<br>■ Updated Table 1-21.<br>■ Under "High-Speed I/O Specification" section, updated Tables 1-25 through 1-30.<br>■ Updated Tables 1-31 through 1-38.<br>■ Added new Table 1-32.<br>■ Under "Maximum Input and Output Clock Toggle Rate" section, updated Tables 1-40 through 1-42.<br>■ Under "IOE Programmable Delay" section, updated Tables 1-43 through 1-44.<br>■ Under "User I/O Pin Timing Parameters" section, updated Tables 1-45 through 1-92.<br>■ Under "Dedicated Clock Pin Timing Parameters" section, updated Tables 1-93 through 1-108. |
| July 2007 | 1.3 | ■ Updated Table 1-1 with $V_{ESDHBM}$ and $V_{ESDCDM}$ information.<br>■ Updated $R_{CONF_PD}$ information in Tables 1-10.<br>■ Added *Note (3)* to Table 1-12.<br>■ Updated $t_{DLOCK}$ information in Table 1-19.<br>■ Updated Table 1-43 and Table 1-44.<br>■ Added "Document Revision History" section. |
| June 2007 | 1.2 | Updated Cyclone III graphic in cover page. |

**Table 1–40. Document Revision History (Part 3 of 3)**

| Date | Version | Changes |
|---|---|---|
| May 2007 | 1.1 | ■ Corrected current unit in Tables 1-1, 1-12, and 1-14.<br>■ Added *Note (3)* to Table 1-3.<br>■ Updated Table 1-4 with $I_{CCINT0}$, $I_{CCA0}$, $I_{CCD_PLL0}$, and $I_{CCIO0}$ information.<br>■ Updated Table 1-9 and added *Note (2)*.<br>■ Updated Table 1-19.<br>■ Updated Table 1-22 and added *Note (1)*.<br>■ Changed I/O standard from 1.5-V LVTTL/LVCMOS and 1.2-V LVTTL/LVCMOS to 1.5-V LVCMOS and 1.2-V LVCMOS in Tables 1-41, 1-42, 1-43, 1-44, and 1-45.<br>■ Updated Table 1-43 with changes to LVPEC and LVDS and added *Note (5)*.<br>■ Updated Tables 1-46, 1-47, Tables 1-54 through 1-95, and Tables 1-98 through 1-111.<br>■ Removed speed grade –6 from Tables 1-90 through 1-95, and from Tables 1-110 through 1-111.<br>■ Added a waveform (Receiver Input Waveform) in glossary under letter “R” (Table 1-112). |
| March 2007 | 1.0 | Initial release. |