



## Data Sheet

# AD9970

**1.8 V analog and digital core supply voltage**  
**Serial data link with reduced range LVDS outputs**  
**Correlated double sampler (CDS) with -3 dB, 0 dB, +3 dB, and +6 dB gain**  
**6 dB to 42 dB, 10-bit variable gain amplifier (VGA)**  
**14-bit, 65 MHz ADC**  
**Black level clamp with variable level control**  
**Complete on-chip timing generator**  
***Precision Timing core with 240 ps resolution at 65 MHz***  
**On-chip, 3 V horizontal and RGO drivers**  
**5 mm × 5 mm, 32-lead LFCSP VQ**

Professional HDTV camcorders  
Professional/high end digital cameras  
Broadcast cameras  
Industrial high speed cameras  
High speed data acquisition systems

The [AD9970](#) is a highly integrated CCD signal processor for high speed digital video camera applications. Specified at pixel rates of up to 65 MHz, the [AD9970](#) consists of a complete analog front end with analog-to-digital conversion combined with a programmable timing driver. The *Precision Timing* core allows adjustment of high speed clocks with 240 ps resolution at 65 MHz operation. The [AD9970](#) also contains a reduced range LVDS interface for data outputs.

The analog front end includes black level clamping, CDS, VGA, and a 65 MSPS, 14-bit ADC. The timing driver provides the high speed CCD clock drivers for RG, HL, and H1 to H4. Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving 5 mm × 5 mm, 32-lead LFCSP\_VQ, the [AD9970](#) is specified over an operating temperature range of -25°C to +85°C.

For more information about the [AD9970](#), contact Analog Devices via email at [afe.ccd@analog.com](mailto:afe.ccd@analog.com).

The diagram illustrates the internal architecture of the AD9970 camera interface IC. The main signal path starts with the CCD input (CCDIN) entering a CDS (Correlated Double Sampling) stage, which is configured for gains of -3, 0, +3, and +6 dB. The output of the CDS stage then passes through a VGA (Variable Gain Amplifier) stage, which can be configured for gains from 6 dB to 42 dB. The output of the VGA stage is then fed into a 14-bit ADC (Analog-to-Digital Converter). The ADC output is then processed by a reduced range LVDS output block, which provides the final digital output signals (TCLKP, TCLKN, DOUT0, DOUT1, DOUT2, DOUT3). The IC also includes a precision timing generator and a sync generator, which are used to generate internal clocks and sync signals. The horizontal drivers are also shown, which are used to drive the horizontal clock (H1 to H4) and the vertical clock (V1 to V4). The IC is powered by VREF and CLAMP, and has various control pins like REFT, REF, HD, VD, CL, SL, SCK, and SDATA.

Figure 1.

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