

HID & SYSTEM MANAGEMENT PRODUCTS, H/PC IC FAMILY

DESCRIPTION

The UR5HCSPi-06 keyboard encoder and power management IC is designed specifically for handheld PCs (H/PCs). The off-the-shelf UR5HCSPi-06 will readily work with CPUs designed for Windows CE®, saving OEMs significant development time and money as well as minimizing time-to-market for the new generations of handheld products.

Three main design features of the UR5HCSPi-06 make it the ideal companion for the new generation of Windows CE® -compatible, single-chip computers: low-power consumption; real estate-saving size; and special keyboard modes.

“Quasi” Zero-Power™ consumption (less than 2µA @ 3V), a must for H/PCs, provides the host system with both power management and I/O flexibility, with almost no battery drainage.

Finally, special keyboard modes and built-in power management features allow the SPICoder™ 06 to operate in harmony with the power management modes of Windows CE®, resulting in more user flexibility and longer battery life.

The UR5HCSPi-06 also offers programmable features for wake-up keys and general purpose I/O pins.

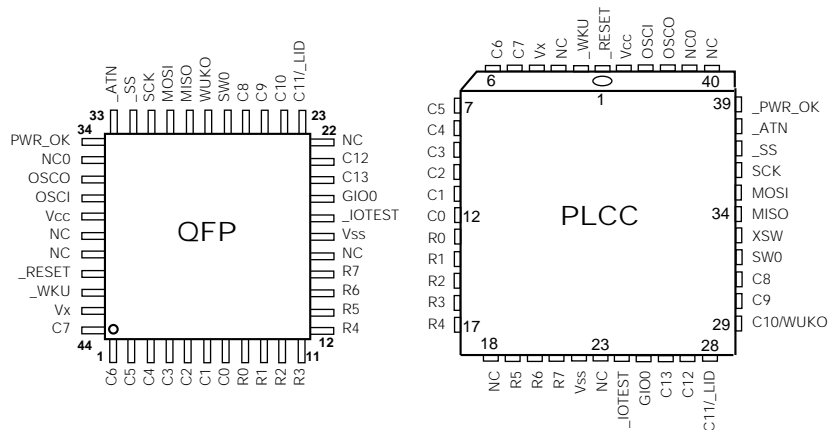
FEATURES

- SPI-compatible keyboard encoder and power management IC with other interfaces available
- Compatible with Windows CE® keyboard specification
- Zero-Power™ — typically consuming less than 2µA, between 3-5V
- Offers overall system power management capabilities
- Compatible with “system-on-silicon” CPUs for H/PCs
- Special keyboard and power management modes for H/PCs, including programmable “wake-up” keys
- Scans, debounces, and encodes an 8 x 14 matrix and controls discrete switches and LED indicators
- Available in a small 44-pin QFP package
- Custom versions available

APPLICATIONS

- StrongARM™ Handheld PCs
- Windows CE® Platforms
- Web Phones
- Personal Digital Assistants (PDAs)
- Wearable Computers
- Internet Appliance

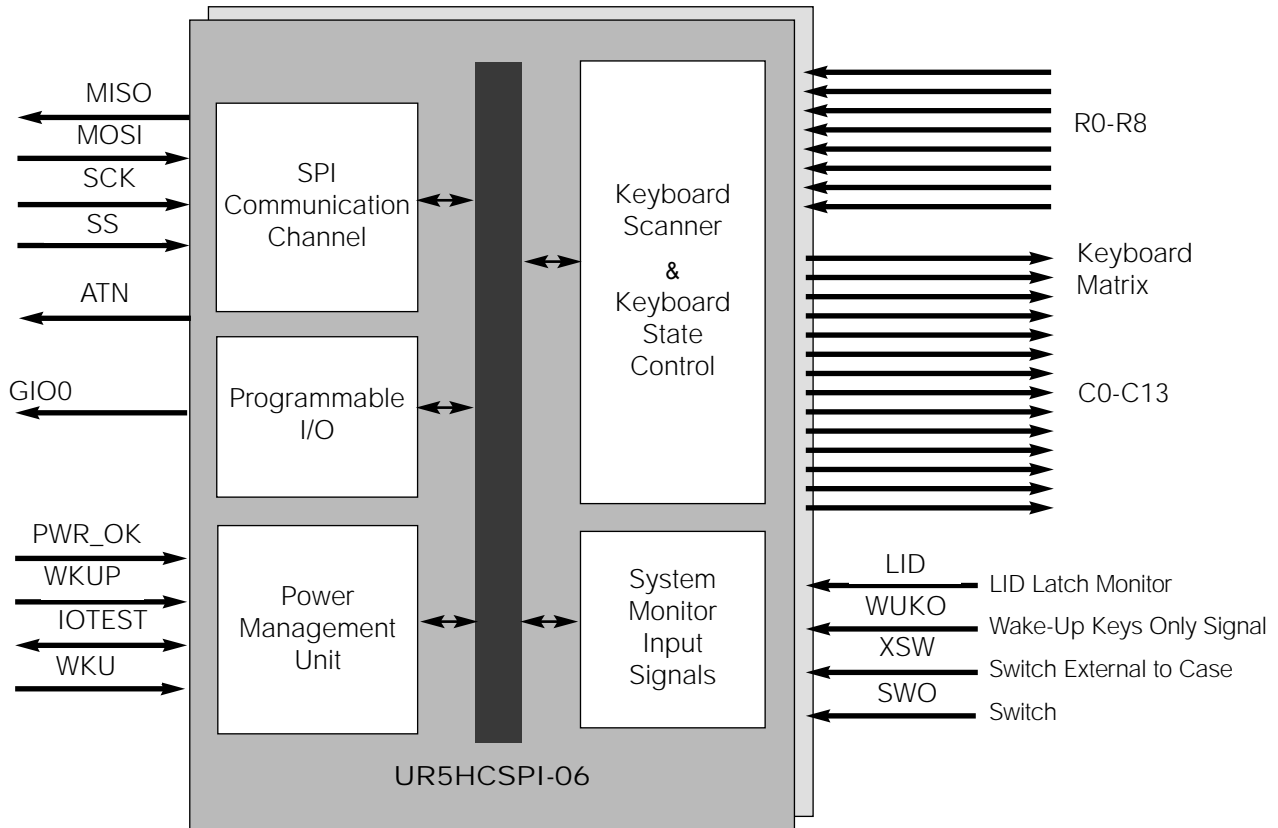
PIN ASSIGNMENTS



ORDERING CODE

Package Options	Pitch in mm's	TA=-20° C to +85° C
44-pin, Plastic PLCC	1.27 mm	UR5HCSPi-06-XX-FN
44-pin, Plastic QFP	0.8 mm	UR5HCSPi-06-XX-FB

Note 1: XX=Optional Customization, XXX= Denotes Revision number

BLOCK DIAGRAM


FUNCTIONAL DESCRIPTION

The UR5HCSPi-06 consists functionally of five major sections (see the Functional Diagram on page 2). These are the Keyboard Scanner and State control, the Programmable I/O, the SPI Communication Channel, the System Monitor and the Power Management unit. All sections communicate with each other and operate concurrently.

PIN DEFINITIONS

Mnemonic	PLCC	QFP	Type	Name and Function
VCC	44	38	I	Power Supply: 3-5V
VSS	22	17	I	Ground
VX	4	43	I	Tie to VCC
OSCI	43	37	I	Oscillator input
OSCO	42	36	O	Oscillator output
_RESET	1	41	I	Reset: apply 0V to provide orderly start-up
MISO	34	29	O	SPI Interface Signals
MOSI	35	30	I	
SCK	36	31	I	Slave Select: If not used tie to VSS
_SS	37	32	I	
_IOTEST	24	18	O	Wake-Up Control Signals
_WKU	2	42	I	Row Data Inputs
R0-R4	13-17	8-12	I	
R5-R7	19-21	13-15	I	Port provides internal pull-up resistors
C0-C5	12-7	7-2	O	Column Select Outputs:
C6-C7	6-5	1,44	O	Multi-function pins
C8-C9	31-30	26-25	O	
C10	29	24	I/O	C10 & "Wake-Up Keys Only" input
C11/_LID	28	23	I/O	C11 & Lid latch detect input
				Miscellaneous functions
C12	27	21	I/O	C12
C13	26	20	I/O	C13
GIO0	25	19	I/O	Programmable I/O
WUKO	33	28	I	External discrete switch
SWO	32	27	I	Discrete switch
				Power Management Pins
_ATN	38	33	O	CPU Attention Output
_PWR_OK	39	34	I	Power OK Input
NC	3,18	39-40		No Connects: these pins are unused
	23,40	16,22		
NC0	41	35		NC0 should be tied to VSS or GND

Note 1: An underscore before a pin mnemonic denotes an active low signal.

PIN DESCRIPTIONS

VCC and VSS

VCC and VSS are the power supply and ground pins. The UR5HCSPi-06 will operate from a 3-5 Volt power supply. To prevent noise problems, provide bypass capacitors and place them as close as possible to the IC with the power supply. VX, where available, should be tied to Vcc.

OSCI and OSCO

OSCI and OSCO provide the input and output connections for the on-chip oscillator. The oscillator can be driven by any of the following circuits:

- Crystal
- Ceramic Resonator
- External Clock Signal

The frequency of the on-chip oscillator is 2 MHz.

_RESET

A logic zero on the _RESET pin will force the UR5HCSPi-06 into a known start-up state. The reset signal can be supplied by any of the following circuits:

- RC
- Voltage monitor
- Master system reset

MOSI, MISO, SCK, _SS, _ATN

These five signals implement the SPI interface. The device acts as a slave on the SPI bus. The _SS (Slave Select) pin should be tied to ground if not used by the SPI master. The _ATN pin is asserted low each time the UR5HCSPi-06 has a packet ready for delivery. For a more detailed description, refer to the SPI Communication Channel section on page 9.

_IOTEST and _WKU

“Input Output Test” and “Wake Up” pins control the stop mode exit of the device. The designer can connect any number of active low signals to these two pins through a 17K resistor, in order to force the device to exit the stop mode. A sample circuit is shown on page 15 of this document.

All the signals are “wire-anded.” When any one of these signals is not active, it should be floating (i.e., these signals should be driven from “open-collector” or “open-drain” outputs). Other configurations are possible; contact Semtech.

R0-R 7

The R0-R7 pins are connected to the rows of the scanned matrix. Each pin provides an internal pull-up resistor, eliminating the need for external components.

C0-C9

C0 to C9 are bi-directional pins connected to the columns of the scanned matrix. When a column is selected, the pin outputs an active low signal. When the column is de-selected, the pin turns into high-impedance.

C10/WUKO

The C10/WUKO pin acts alternatively as column scan output and as an input. As an input, the pin detects the “Wake-Up Keys Only” signal, typically provided by the host CPU to indicate that the user has turned the unit off. When the device detects an active high state on this pin, it feeds this information into the “Keyboard State Control” unit, in order to disable the keyboard and enable the programmed wake-up keys.

C11/_LID

The C11/_LID pin acts in a similar manner to the C10/WUKO. This pin is typically connected to the LID latch through a 150K resistor, in order to detect physical closing of the device cover. When the pin detects an active low state in this input, it feeds this information into the “Keyboard State Control” unit, in order to disable keys inside the case and enable only switches located physically on the outer body of the H/PC unit.

PIN DESCRIPTIONS, (CON'T)

C12, C13 and GIO0

The SPICoder™ 06 offers pins C12, C13 and GIO0. C12 and C13 are used as additional column pins in order to accommodate larger-size keyboards, such as the Fujitsu FKB1406 palmtop keyboard. GIO0 is a programmable input/output switch; it can also be used as a wake-up signal. The programming of the GIO0 is explained on page 8 of this document.

XSW

The XSW pin is dedicated to an external switch. This pin is handled differently than the rest of the switch matrix and is intended to be connected to a switch physically located on the outside of the unit.

SW0

The SW0 pin is a dedicated input pin for a switch.

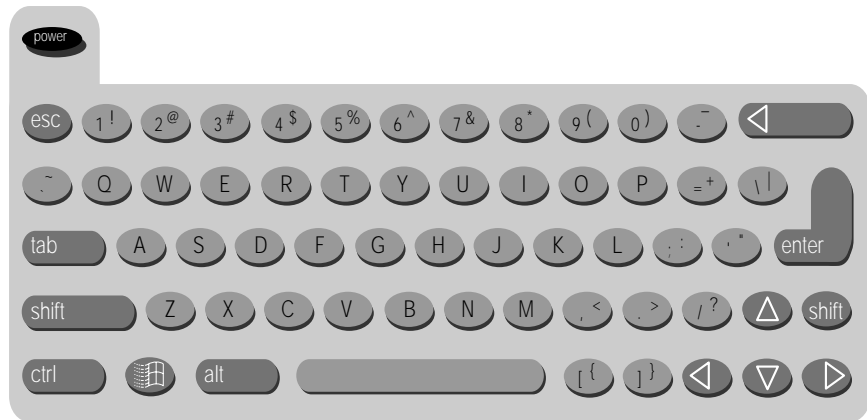
PWR_OK

The PWR_OK is an active low pin that monitors the battery status of the unit. When the UR5HCSP1-06 detects a transition from high to low on this pin, it will immediately enter the STOP mode, turn the LED off and remain in this state until the batteries of the unit are replaced and the signal is deasserted.

WINDOWS CE® KEYBOARD

The following illustration shows a typical implementation of a Windows CE® keyboard.

Windows CE® does not support the following keyboard keys typically found on desktop and laptop keyboards:



- INSERT
- SCROLL LOCK
- PAUSE
- NUM LOCK
- Function Keys (F1-F12)
- PRINT SCREEN

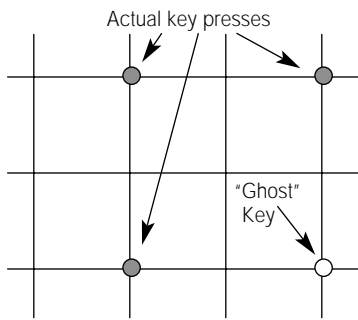
If the keyboard implements the Windows key, the following key combinations are supported in the Windows CE® environment:

Key Combination	Result
Windows	Open Start Menu
Windows+K	Open Keyboard Tool
Windows+I	Open Stylus Tool
Windows+C	Open Control Panel
Windows+E	Explore the H/PC
Windows+R	Display the Run Dialog Box
Windows+H	Open Windows CE® Help
Ctrl+Windows+A	Select all on desktop

"GHOST" KEYS

In any scanned contact switch matrix, whenever three keys defining a rectangle on the switch matrix are pressed at the same time, a fourth key positioned on the fourth corner of the rectangle is sensed as being pressed. This is known as the "ghost" or "phantom" key problem.

Figure 1: "Ghost" or "Phantom" Key Problem



Although the problem cannot be totally eliminated without using external hardware, there are methods to neutralize its negative effects for most practical applications. Keys that are intended to be used in combinations should be placed in the same row or column of the matrix, whenever possible. Shift Keys (Shift, Alt, Ctrl, Window) should not reside in the same row (or column) as any other keys. The UR5HCSPi-06 has built-in mechanisms to detect the presence of "ghost" keys.

KEYBOARD SCANNER

The encoder scans a keyboard organized as an 8 row by 14 column matrix for a maximum of 112 keys. Smaller size matrixes can also be accommodated by simply leaving unused pins open. The UR5HCSPi-06 provides internal pull-ups for the Row input pins. When active, the encoder selects one of the column lines (C0-C13) every 512 μ S and then reads the row data lines (R0-R7). A key closure is detected as a zero in the corresponding position of the matrix.

A complete scan cycle for the entire keyboard takes approximately 9.2 mS. Each key found pressed is debounced for a period of 20 mS. Once the key is verified, the corresponding key code(s) are loaded into the transmit buffer of the SPI communication channel.

N-Key Rollover

In this mode, the code(s) corresponding to each key press are transmitted to the host system as soon as that key is debounced, independent of the release of other keys.

When a key is released, the corresponding break code is transmitted to the host system. There is no limitation to the number of keys that can be held pressed at the same time. However, two or more key closures, occurring within a time interval of less than 5mS, will set an error flag and will not be processed. This feature is to protect against the effects of accidental key presses.

Data Command Buffer

The UR5HCSPi-06 implements a data buffer, which contains the key code/command bytes waiting to be transmitted to the host. If the data buffer is full, the whole buffer will be cleared and an "Initialize" command will be sent to the host. At the same time, the keyboard will be disabled until the "Initialize" or "Initialize Complete" command from the host is received.

Power Management Unit

In most keyboard subsystems, the power consumption is determined by the use of the LEDs. In these situations, USAR has implemented two modes of operation to minimize power drain. (For more information, see page 10 on the UR5HCSPi datasheet - doc5-spi-ds-100.pdf.) However, since the SPICoder™ 06 does not provide LED output/input, this is not a concern.

KEYBOARD STATES

These states of operation refer only to the keyboard functionality and, although they are related to power states, they are also independent of them.

"Send All Keys"

Entry Conditions: Power on reset, soft reset, PWR_OK = 1, $\{(LID=1) \text{ AND } (WUKO=0)\}$

Exit Conditions: PWR_OK = 0 -> "Send No Keys"(WUKO=1) AND (Key Press) -> "Send Wake-Up Keys Only"(LID = 0) AND (WUKO=0) AND (Key Press) -> "Send XSW Key Only"

Description: This is the UR5HCSPI-06's normal state of operation, accepting and transmitting every key press to the system. This state is entered after the power-on and is sustained while the unit is being used.

"Send Wake-Up Keys Only"

Entry Conditions: (WUKO=1) AND (Key or Switch press)

Exit Conditions: Soft Reset -> "Send All Keys" PWR_OK = 0 -> "Send No Keys"

Description: This state is entered when the user turns the unit off. A signal line driven by the host will notify the UR5HCSPI-06 about this state transition. While in this state, the UR5HCSPI-06 will transmit only keys programmed to be wake-up keys to the system. It is not necessary for the UR5HCSPI-06 to detect this transition in real time, since it does not affect any operation besides buffering keystrokes.

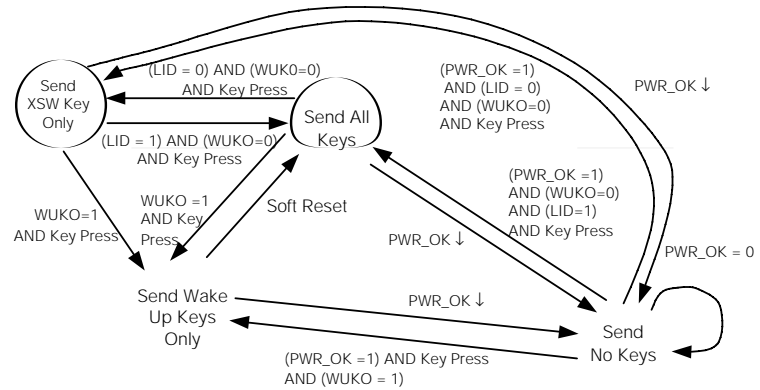


Figure 2: The UR5HCSPI-06 implements four modes of keyboard and switch operation.

"Send No Keys"

Entry Conditions: PWR_OK transition from high to low

Exit Conditions: (PWR_OK = 1) AND (Matrix key pressed OR Switch OR _WKUP)

Description: This state is entered when a PWR_OK signal is asserted (transition high to low), indicating a critically low level of battery voltage. The PWR_OK signal will cause an interrupt to the UR5HCSPI-06, which guarantees that the transition is performed in real time. While in this state, the UR5HCSPI-06 will perform as follows:

1. The UR5HCSPI-06 will enter the STOP mode for maximum energy conservation.
2. Stop mode time-out entry will be shortened to further conserve energy.

3. While in this state all interrupts are disabled. The UR5HCSPI-06 will exit this state on the next interrupt event that detects the PWR_OK line has been de-asserted.

"Send XSW Key Only"

Entry Condition: (LID=0) AND (WUKO=0) AND (Key Press)

Exit Condition: (LID=1) AND (WUKO=0) AND (Key Press) -> "Send All Keys" PWR_OK = 0 -> "Send No Keys" (WUKO = 1) AND (Key Press) -> "Send Wake Up Keys Only"

Description: This state is entered upon closing the lid of the device. While in this state, the encoder will transmit only the XSW key, which is located outside the unit. This feature is designed to accommodate buttons on the outside of the box, such as a microphone button, that need to be used while the lid is closed.

KEY CODES

Key codes range from 01H to 73H and are arranged as follows:

Make code = column_number * 8 + row_number + 1

Break code = Make code OR 80H

Discrete Switches transmit the following codes:

XSW = 71H

SW0 = 72H

GIO0 = 73H

Pin Configurations

When prototyping, caution should be taken to ensure that programming of the GIO0 pin does not conflict with the circuit implemented. A series protection resistor is recommended to be used for protection over improper programming of the pin.

After a power-on or soft reset, GIO0 defaults to the Input state.

The drawing to the right illustrates the suggested interface to the general purpose input/output pin.

GIO0 PIN

The UR5HCSPi-06 a general purpose pin that can be programmed as Input, Output, Debounced or Switch Input. The programmable I/O pin can be configured to the desired mode through a command from the system. After the I/O pin is configured, the host system can read or write data to it. If the pin is configured as a Debounced Switch, it will return scan codes.

Input Mode

While in the Input Mode, the GIO0 pin will detect input signals and report the input status to the system as required.

Output Mode

In the Output Mode, the UR5HCSPi-06 will control the output signal level according to the system command. When the pin is set at Output Mode, the default output is low.

Switch Input Mode

In Switch Input Mode, the UR5HCSPi-06 will generate an individual make key code when the switch closes (pin goes low), and a break key code when the switch returns to open (pin goes to high). The switches generate key codes outside of those generated by the key matrix, from 71H - 73H. When the switch closes, the SPICoder™ will not fall asleep.

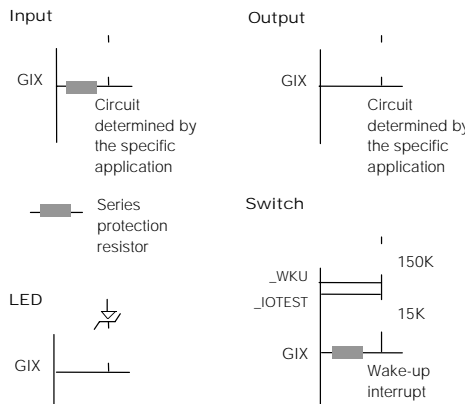


Figure 3: The suggested interface to the general purpose input/output pin

SPI COMMUNICATION CHANNEL

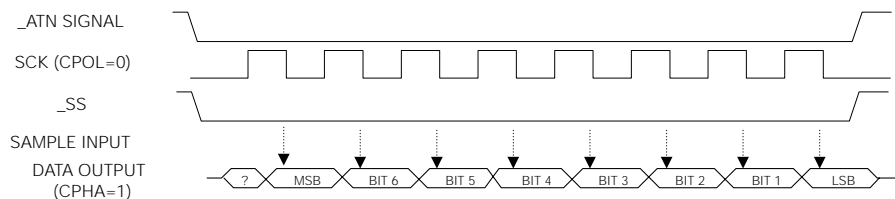
SPI data transfers can be performed at a maximum clock rate of 500 KHz. When the UR5HCSPi asserts the `_ATN` signal to the host Master, the data will have already been loaded into the data register waiting for the clocks from the master. The Slave Select (`SS`) line can be tied permanently to Ground if the UR5HCSPi is the only slave device in the SPI network. One `_ATN` signal is used per each byte transfer. If the host fails to provide clock signals for successive bytes in the data packet within 120 mS, the transmission will be aborted and a new session will be initiated by asserting a new `ATN` signal. In this case, the whole packet will be re-transmitted.

If the SPI transmission fails 20 times consecutively, the synchronization between the master and slave may be lost. In this case, the UR5HCSPi will enter the reset state.

The UR5HCSPi implements the SPI communication protocol according to the following diagram:

`CPOL = 0` ----- SCK line idles in low state

`CPHA = 1` ----- SS line is an output enable control



When the host sends commands to the keyboard, the UR5HCSPi-06 requires that the minimum and maximum intervals between two successive bytes be 200 μ S and 5 mS respectively.

Figure 5: SPI Communication Protocol

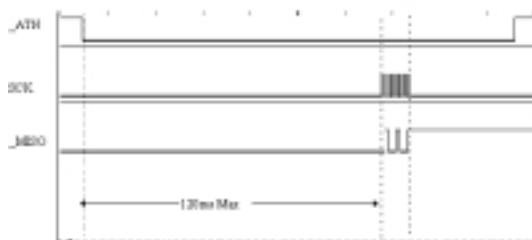


Figure 6: Transmitting Data Waveforms:



Figure 7: Receiving Data Waveforms

DATA/COMMAND BUFFER

The UR5HCSPi-06 implements a data buffer that contains the key code/command bytes waiting to be transmitted to the host. If the data buffer is full, the whole buffer will be cleared and an "Initialize" command will be sent to the host. At the same time, the keyboard will be disabled until the "Initialize" or "Initialize Complete" command from the host is received.

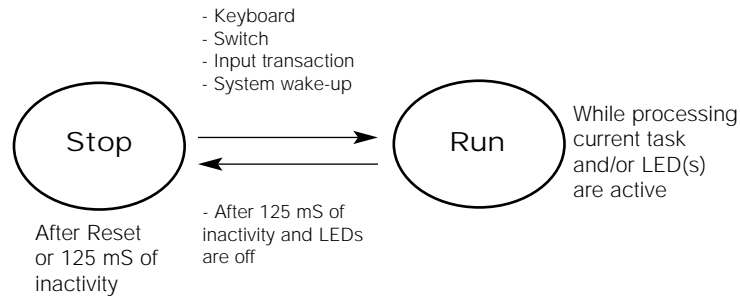
POWER MANAGEMENT UNIT

The UR5HCSPi-06 supports two modes of operation. The following table lists the typical and maximum supply current (no DC loads) for each mode at 3.3 Volts (+/- 10%).

Current	Typical	Max	Unit	Description
RUN	1.5	3.0	mA	Entered only while data/commands are in process and if the LEDs are blinking
STOP	2.0	20	µA	Entered after 125 mS of inactivity if LEDs islow

Power consumption of the keyboard sub-system will be determined primarily by the use of the LEDs. While the UR5HCSPi-06 is in the STOP mode, an active low Wake-Up Output from the Master must be connected to the edge-sensitive _WKU pin of the UR5HCSPi-06. This signal will be used to wake up the UR5HCSPi-06 in order to receive data from the Master host. The Master host will have to wait a minimum of 5 mS prior to providing clocks to the UR5HCSPi-06. The UR5HCSPi-06 will enter the STOP mode after a 125 mS period of keypad and/or host communications inactivity, or anytime the PWR_OK line is asserted low by the host. Note that while one or more keys are held pressed, the UR5HCSPi-06 will not enter the STOP mode until every key is released.

Figure 6: The Power States of the UR5HCSPi-06



LRC CALCULATION, (CON'T)

The following C language function is an example of an LRC calculation program. It accepts two arguments: a pointer to a buffer and a buffer length. Its return value is the LRC value for the specified buffer.

```
char Calculate LRC (char buffer,
size_t buffer)
{
char LRC;
size_t index;
/*
* Init the LRC using the first two
message bytes.
*/
LRC = buffer [0] ^ buffer [1];
/*
* Update the LRC using the
remainder of the buffer.
*/
for (index = 2; index < buffer; index
++)
LRC ^ = buffer[index];
/*
* If the MSB is set then clear the
MSB and change the next most
significant bit
*/
if (LRC & 0x80)
LRC ^ = 0xC0;
/* * Return the LRC value for the
buffer.*}
```

COMMANDS FROM THE UR5HCSP1-06 TO THE HOST, (CON'T)

Resend Request

<CONTROL>	80H
<RESEND>	A5H
<LRC>	25H

The UR5HCSP1-06 will send this Resend Request Command to the host when its command buffer is full, or if it detects either a parity error or an unknown command during a system command transmission.

Input/Output Mode Status Report

<CONTROL>	80H	
<MODIO>	A7H	
<IO NUMBER>	xxH	IO number, 0
<IO MODE>	xxH	IO mode: (0=input; 1=output; 2=switch; 3=LED)
<LRC>	xxH	

The UR5HCSP1-06 will send the I/O Mode Status Report to the host when it receives the I/O Mode Status Request Command from the host, in order to report the status of the GIO0 pin.

Input/Output Data Report

<CONTROL>	80H	
<MODIO>	A8H	
<IO NUMBER>	xxH	IO number, 0
<IO DATA>	xxH	IO data: (0=low, 1=high)
<LRC>	xxH	

The UR5HCSP1-06 will send the I/O Data Report to the host when it receives the I/O Data Request Command from the host.



COMMANDS FROM THE HOST TO THE UR5HCSPi-06

Commands from the Host - Summary

Command Name	Code	Description
Initialize	A0H	Causes the UR5HCSPi-06 to enter the power-on state
Initialization Complete	A1H	Issued as a response to the "Initialize Request"
Heartbeat Request	A2H	The UR5HCSPi-06 will respond with "Heartbeat Response"
Identification Request	F2H	The UR5HCSPi-06 will respond with "Identification Response"
Resend Request	A5H	Issued upon error during the reception of a packet
Input/Output Mode Modify	A7H	The UR5HCSPi-06 will modify or report the status of the GIO0 pin
Output Data to I/O pin	A8H	The UR5HCSPi-06 will output a signal to the GIO0 pin
Set Wake-Up Keys	A9H	Defines which keys are "wake-up" keys

Each command to UR5HCSPi-06 is composed of a sequence of codes. All commands start with <ESC> code (1BH) and end with the LRC code (bitwise exclusive OR of all bytes).

COMMANDS FROM THE HOST TO THE UR5HCSPi-06 ANALYTICALLY

Initialize

<ESC> 1BH
<INIT> A0H
<LRC> 7BH

When the UR5HCSPi-06 receives this command, it will clear all buffers and return to the power-on state.

Initialization Complete

<ESC> 1BH
<INIT COMPLETE> A1H
<LRC> 7AH

When the UR5HCSPi-06 receives this command, it will enable transmission of keyboard data. Keyboard data transmission is disabled if the TX output buffer is full (32 bytes). Note that if the transmit data buffer gets full the encoder will issue an "Initialize Request" to the host.

Heartbeat Request

<ESC> 1BH
<ONLINE> A2H
<LRC> 79H

When the UR5HCSPi-06 receives this command, it will reply with the Heartbeat Response Report.

Identification Request

<ESC> 1BH
<ID> F2H
<LRC> 29H

The UR5HCSPi-06 will reply to this command with the Identification Response Report.

COMMANDS FROM THE HOST TO THE UR5HCSPi-06, (CON'T)
Set Wake-Up Keys

```

<ESC>          1BH
<SETMATRIX>   A9H
<COL0>        xxH   (R7
R6 R5 R4 R3 R2 R1 R0 Bitmap: 0-
enabled, 1-disabled)
<COL1>        xxH
<COL2>        xxH
<COL3>        xxH
<COL4>        xxH
<COL5>        xxH
<COL6>        xxH
<COL7>        xxH
<COL8>        xxH
<COL9>        xxH
<COL10>       xxH
<COL11>       xxH
<COL12>*<    xxH
(*UR5HCSPi-06-06-XX only)
<COL13>*<    xxH
(*UR5HCSPi-06-06-XX only)
<SWITCHES>    xxH
(where SWITCHES bit assignments
are = x x x x x GIO0 SW0 XSW)
<LRC>         xxH

```

The "Set Wake-Up Keys" command is used to disable specific keys from waking up the host. Using this command, the host can set only a group of keys. For this IC, data in bytes <COL12> and <COL 13> is not relevant, but these two bytes must be present in the packet in order to preserve the packet structure.

I/O Mode Modify

```

<ESC>          1BH
<MODIO>       A7H
<IO NUMBER>   xxH   IO number: 0
<IO MODE>     xxH   IO mode: ( 0=input, 1=output,
2=switch, 3=LED, 4=current mode state
request)
<LRC>         xxH

```

When UR5HCSPi-06 receives this command, it will change the I/O pin's mode accordingly. If the <IO MODE> =4, the UR5HCSPi-06 will send the I/O Mode Status Report to the host.

Output Data to I/O Pin:

```

<ESC>          1BH
<MODIO>       A8H
<IO NUMBER>   xxH   IO number: 0
<IO DATA>    xxH   IO data: ( 0=low, 1=high, 2=current
I/O data request)
<LRC>         xxH

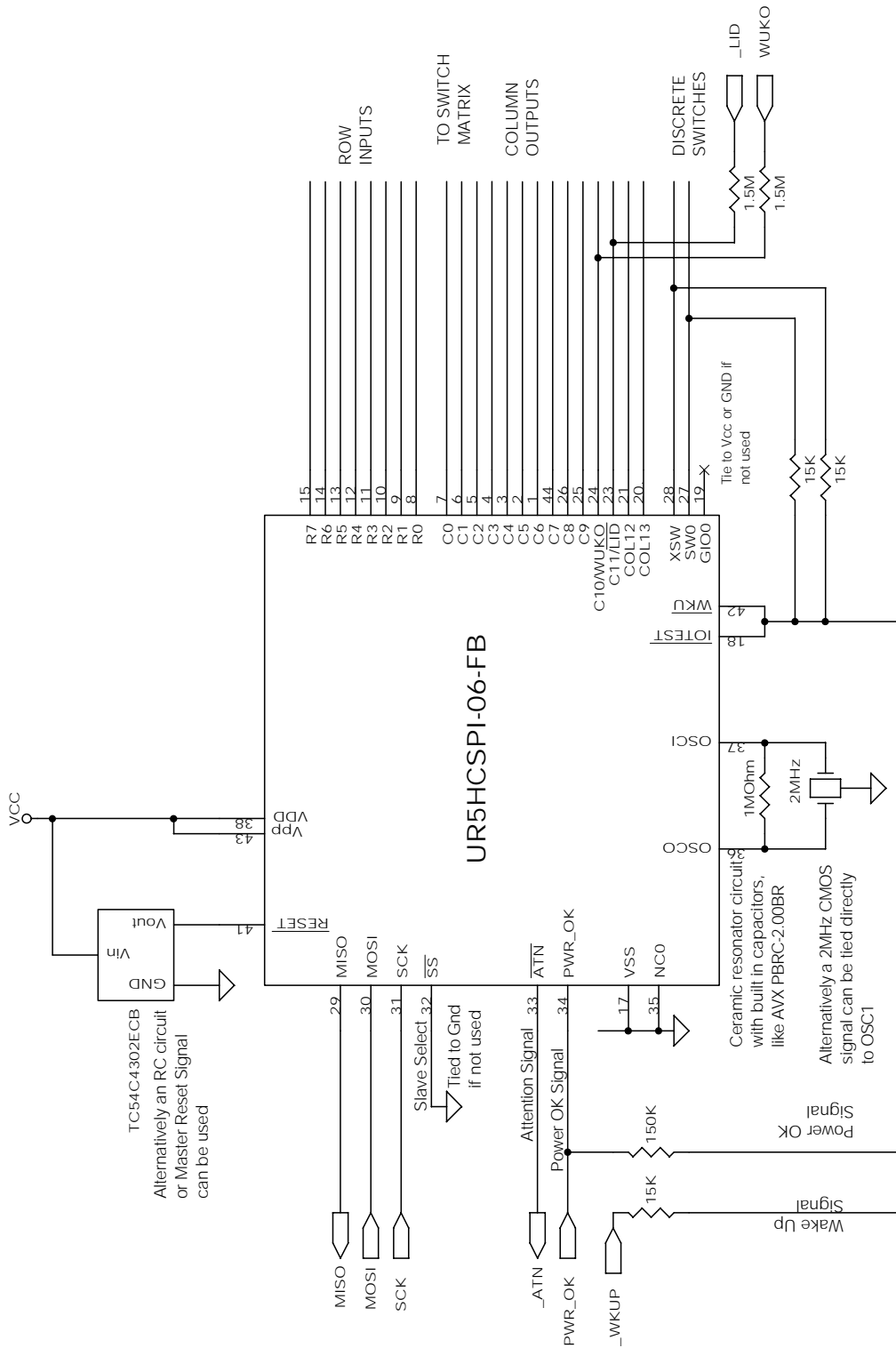
```

When UR5HCSPi-06 receives this command, it will change the value of the output pin accordingly. If the addressed pin is not configured as an output pin, the command will be ignored. If <IO DATA> =2, the UR5HCSPi-06 will respond by issuing the I/O Data Status Report to the host.

KEY MAP FOR THE FUJITSU FKB1406

		Columns (C0-C13)													
		0	1	2	3	4	5	6	7	8	9	10	11	12	13
Rows (R0-R6)	0	LAlt	`		LCtrl	FN	Esc	1 F1	2 F2	9 F9	0 F10	- NmLk	+ Bk		BkSp
	1		\	LSft			Del		T	Y	U Pad 4	I Pad 5	Enter	RShift	↓ PgDn
	2		TAB				Q	W	E	R	O Pad 6	P Ins	[Pause] ScrLk
	3		Z				CapLk			K Pad 2	L Pad 3	; PrtScr	' SysReq		↑ PgUp
	4		A				S	D	F	G	H	J Pad 1	/		← Home
	5		X				C	V	B	N Pad 0	M	,	.		Spc
	6						3 F3	4 F4	5 F5	6 F6	7 F7	8 F8		Prog	→ End

KEYBOARD LAYOUT FOR FUJITSU FKB1406

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IMPLEMENTATION NOTES FOR THE UR5HCSPi-06

The following notes pertain to the suggested schematic found on the previous page.

The Built-in Oscillator on the UR5HCSPi-06 requires the attachment of the 2.00 MHz Ceramic Resonators with built-in Load Capacitors.. You can use either an AVX, part number PBRC-2.00 BR; or a Murata part number CSTCC2.00MG ceramic resonator.

It may also be possible to operate with the 2.00 MHz Crystal, albeit with reduced performance. Due to their high Q, the Crystal oscillator circuits start-up slowly. Since the SPICoder™ constantly switches the clock on and off, it is important that the Ceramic Resonator is used (it starts up much quicker than the Crystal). Resonators are also less expensive than Crystals.

Also, if Crystal is attached, two Load Capacitors (33pF to 47pF) should be added, a Capacitor between each side of the Crystal and ground.

In both cases, using Ceramic Resonator with built-in Load Capacitors, or Crystal with external Load Capacitors, a feedback Resistor of 1 Meg should be connected between OSCIN and OSCOUT.

Troubleshoot the circuit by looking at the Output pin of the Oscillator. If the voltage is half-way between Supply and Ground (while the Oscillator should be running) --- the problem is with the Load Caps / Crystal. If the voltage is all the way at Supply or Ground (while the Oscillator should be running) --- there are shorts on the PCB.

Note: When the Oscillator is intentionally turned OFF, the voltage on the Output pin of the Oscillator is High (at the Supply rail).

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Ratings	Symbol	Value	Unit
Supply Voltage	Vdd	-0.3 to +7.0	V
Input Voltage	Vin	Vss -0.3 to Vdd +0.3	V
Current Drain per Pin (not including Vss or Vdd)	I	25	mA
Operating Temperature UR5HCSPI-06	Ta	T low to T high -40 to +85	°C
Storage Temperature Range	Tstg -	-65 to +150	°C

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance	Tja		°C per W
■ Plastic		60	
■ PLCC		70	

DC Electrical Characteristics (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I load<10µA)	Vol			0.1	V
	Voh	Vdd-0.1			
Output High Voltage (I load=0.8mA)	Voh	Vdd-0.8			V
Output Low Voltage (I load=1.6mA)	Vol:			0.4	V
Input High Voltage	Vih	0.7xVdd		Vdd	V
Input Low Voltage	Vil	Vss		0.2xVdd	V
User Mode Current	Ipp		5	10	mA
Data Retention Mode (0 to 70°C)	Vrm	2.0			V
Supply Current (Run)	Idd		1.53	3.0	mA
(Wait)			0.711	1.0	mA
(Stop)			2.0	20	µA
I/O Ports Hi-Z Leakage Current	Iil			+/-10	µA
Input Current	Iin			+/- 1	µA
I/O Port Capacitance	Cio		8	12	pF

Control Timing (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation	fosc			MHz
■ Crystal Option			2.0	
■ External Clock Option		dc	2.0	
Cycle Time	tcyc	1000		ns
Crystal Oscillator Startup Time	toxov		100	ms
Stop Recovery Startup Time	tilch		100	ms
RESET Pulse Width	trl	8		tcyc
Interrupt Pulse Width Low	tlih	250		ns
Interrupt Pulse Period	tilil	*		tcyc
OSC1 Pulse Width	toh, tol	200		ns

*The minimum period tilil should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 tcyc.



SPICODER™ BILL OF MATERIALS

UR5HCSPi-06-FB

Quantity	Manufacture	Part#	Description
3	Generic	15K	15K Resistor
1	Generic	150K	150K Resistor
1	Generic	1M	1M Resistor
2	Generic	1.5K	1.5 Resistors
1	TELCOM	TC54VC4302ECB713	IC Volt Detector CMOS 4.3V SOT23, for 5V Operation
		TC54VC2702ECB713	IC Volt Detector CMOS 2.7V SOT23, for 3.3V Operation
1	AVX	PBRC-2.00BR	2.00MHZ Ceramic Resonator with Built in Capacitors, SMT

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For sales information
and product literature,
contact:

HID & System Mgmt Division
Semtech Corporation
568 Broadway
New York, NY 10012
hidinfo@semtech.com
<http://www.semtech.com>
212 226 2042 Telephone
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Semtech Western Regional Sales
805-498-2111 Telephone
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Semtech Asia-Pacific Sales Office
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+886-2-2748-3390 Telefax

Semtech Japan Sales Office
+81-45-948-5925 Telephone
+81-45-948-5930 Telefax

Semtech Korea Sales Sales
+82-2-527-4377 Telephone
+82-2-527-4376 Telefax

Northern European Sales Office
+44 (0)2380-769008 Telephone
+44 (0)2380-768612 Telefax

Southern European Sales Office
+33 (0)1 69-28-22-00 Telephone
+33 (0)1 69-28-12-98 Telefax

Central European Sales Office
+49 (0)8161 140 123 Telephone
+49 (0)8161 140 124 Telefax

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