Dual 2-Phase, No R_{SENSE}™, DC/DC Controller with Output Tracking

FEATURES

- **Sense Resistor Optional**
- **Out-of-Phase Controllers Reduce Required Input Capacitance**
- **Programmable Output Voltage Tracking**
- Constant Frequency Current Mode Architecture
- Wide V_{IN} Range: 2.75V to 9.8V
- Wide V_{OUT} Range: 0.6V to V_{IN}
- 0.6V ±1.5% Reference
- Low Dropout Operation: 100% Duty Cycle
- True PLL for Frequency Locking or Adjustment (Frequency Range 250kHz to 850kHz)
- Selectable Burst Mode® or Pulse Skipping Operation at Light Loads
- Internal Soft-Start Circuitry
- Selectable Maximum Peak Current Sense Threshold
- Power Good Output Voltage Monitor
- Output Overvoltage Protection
- Micropower Shutdown: I_Q = 9µA
- Tiny 4mm × 4mm QFN and 24-Lead SSOP Packages

APPLICATIONS

- One or Two Lithium-Ion Powered Devices
- Notebook and Palmtop Computers, PDAs
- Portable Instruments
- Distributed DC Power Systems

DESCRIPTION

The LTC®3737 is a 2-phase dual step-down switching regulator controller that requires few external components. The constant frequency current mode architecture provides excellent AC and DC load and line regulation. MOSFET V_{DS} sensing eliminates the need for current sense resistors and improves efficiency. Power loss and noise due to the ESR of the input capacitance are minimized by operating the two controllers out of phase.

Burst Mode operation provides high efficiency operation at light loads. 100% duty cycle provides low dropout operation and extends battery operating time.

Switching frequency can be programmed up to 750kHz, allowing the use of small surface mount inductors and capacitors. For noise sensitive applications, the LTC3737 can be externally synchronized from 250kHz to 850kHz.

Other features include a power good output voltage monitor, a tracking input and internal soft-start.

The LTC3737 is available in the low profile thermally enhanced (4mm × 4mm) QFN package or a 24-lead SSOP narrow package.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
Burst Mode is a registered trademark of Linear Technology Corporation.
No R_{SENSE} is a trademark of Linear Technology Corporation.
U.S. patent numbers 5481178, 5731694, 5929620, 6144194,6580258, 5994885

TYPICAL APPLICATION

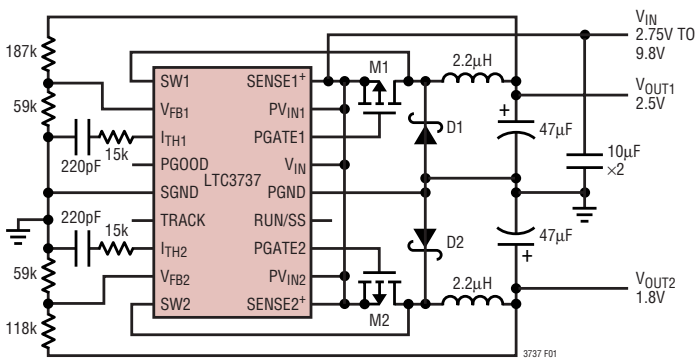
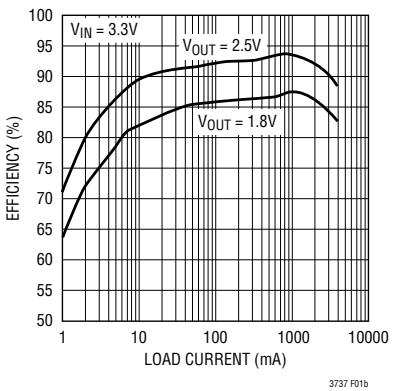


Figure 1. High Efficiency, 2-Phase, 550kHz Dual Step-Down Converter

Efficiency vs Load Current

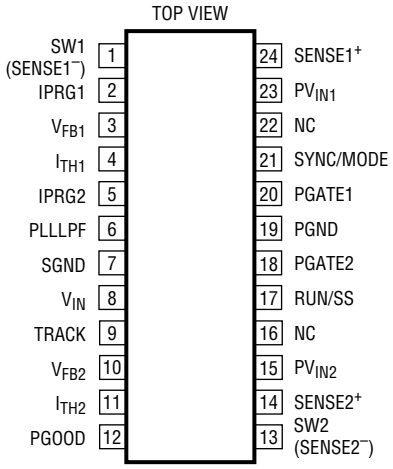


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}), PV_{IN1}, PV_{IN2}, SENSE1+, SENSE2+ ..... –0.3V to 10V
PGATE1, PGATE2, PLLLPF, RUN/SS, SYNC/MODE, TRACK, IPRG1, IPRG2 Voltages .... –0.3V to (V_{IN} + 0.3V)
V_{FB1}, V_{FB2}, I_{TH1}, I_{TH2} Voltages ..... –0.3V to 2.4V
SW1, SW2 Voltages ..... –2V to V_{IN} + 1V or 10V Max
PGOOD ..... –0.3V to 10V
PGATE1, PGATE2 Peak Output Current (<10µs) 1A

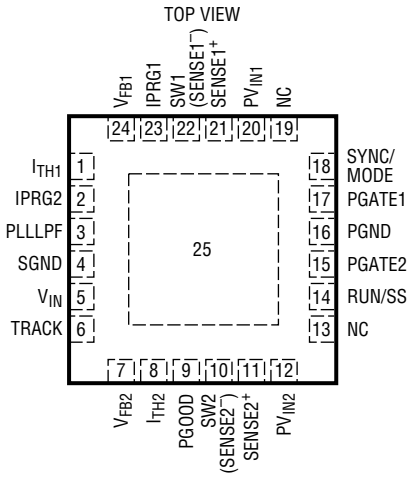
Operating Temperature Range (Note 2) ... –40°C to 85°C
Storage Ambient Temperature Range
QFN Package ..... –65°C to 125°C
SSOP Package ..... –65°C to 150°C
Junction Temperature (Note 3) ..... 125°C
Lead Temperature (Soldering, 10sec)
LTC3737EGN ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
24-LEAD (NARROW) PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC3737EGN



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD IS PGND (PIN 25) MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC3737EUF

UF PART MARKING
3737

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops						
Input DC Supply Current	(Note 4)					
Sleep Mode				220	325	µA
Shutdown	RUN/SS = 0V			9	20	µA
UVLO	V_{IN} < UVLO Threshold			3	10	µA
Undervoltage Lockout Threshold	V_{IN} Falling	●	1.95	2.25	2.55	V
	V_{IN} Rising	●	2.15	2.45	2.75	V
Shutdown Threshold at RUN/SS			0.45	0.65	0.85	V
Start-Up Current Source	RUN/SS = 0V		0.5	0.7	1	µA
Regulated Feedback Voltage	0°C to 85°C (Note 5)		0.591	0.6	0.609	V
	–40°C to 85°C	●	0.588	0.6	0.612	V
Output Voltage Line Regulation	2.75V < V_{IN} < 9.8V (Note 5)			0.05	0.2	mV/V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Load Regulation	I_{TH} = 0.9V (Note 5) I_{TH} = 1.7V			0.12 –0.12	0.5 –0.5	% %
$V_{FB1,2}$ Input Current	(Note 5)			10	50	nA
TRACK Input Current	TRACK = 0.6V			10	50	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.66	0.68	0.7	V
Overvoltage Protect Hysteresis				20		mV
Auxiliary Feedback Threshold	SYNC/MODE Ramping Negative		0.525	0.6	0.675	V
Gate Drive 1, 2 Rise Time	C_L = 3000pF			40		ns
Gate Drive 1, 2 Fall Time	C_L = 3000pF			40		ns
Maximum Current Sense Voltage ($SENSE^+$ – SW)($\Delta V_{SENSE(MAX)}$) IPRG = Floating (Note 6) IPRG = 0V (Note 6) IPRG = V_{IN} (Note 6)		● ● ●	110 70 185	125 85 204	140 100 223	mV mV mV
Soft-Start Time	Time for V_{FB1} to Ramp from 0.05V to 0.55V		0.667	0.833	1	ms
Oscillator and Phase-Locked Loop						
Oscilator Frequency	Unsynchronized (SYNC/MODE Not Clocked)					
	V_{PLLLPF} = Floating	●	480	550	600	kHz
	V_{PLLLPF} = 0V	●	260	300	340	kHz
	V_{PLLLPF} = V_{IN}	●	650	750	825	kHz
Phase-Locked Loop Lock Range	SYNC/MODE Clocked					
	Minimum Synchronizable Frequency	●		200	250	kHz
	Maximum Synchronizable Frequency	●	850	1150		kHz
Phase Detector Output Current						
Sinking	$f_{OSC} > f_{SYNC/MODE}$			–4		µA
Sourcing	$f_{OSC} < f_{SYNC/MODE}$			4		µA
PGOOD Output						
PGOOD Voltage Low	I_{PGOOD} Sinking 1mA			125		mV
PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage					
	V_{FB} < 0.6V, Ramping Positive		–13	–10.0	–7	%
	V_{FB} < 0.6V, Ramping Negative		–16	–13.3	–10	%
	V_{FB} > 0.6V, Ramping Negative		13	10.0	7	%
	V_{FB} > 0.6V, Ramping Positive		16	13.3	10	%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3737E is guaranteed to meet specified performance from 0°C to 70°C. Specifications over the –40°C to 85°C operating range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$$

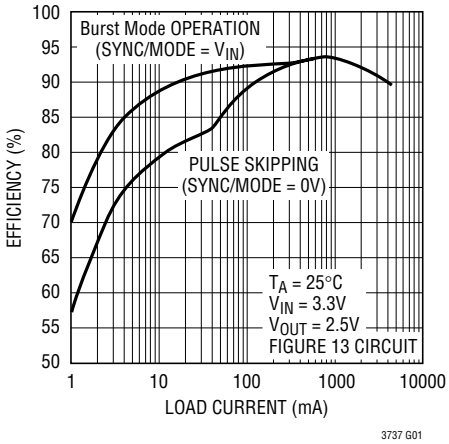
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: The LTC3737 is tested in a feedback loop that servos I_{TH} to a specified voltage and measures the resultant V_{FB} voltage.

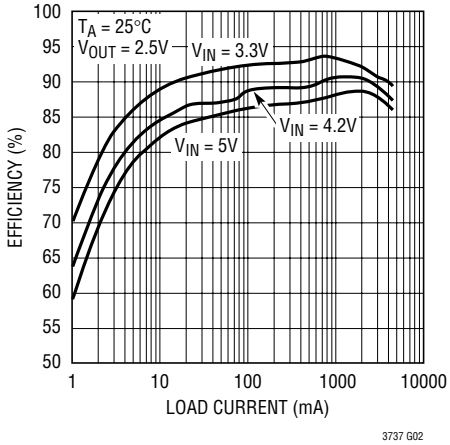
Note 6: Peak current sense voltage is reduced dependent on duty cycle to a percentage of value as shown in Figure 2.

TYPICAL PERFORMANCE CHARACTERISTICS

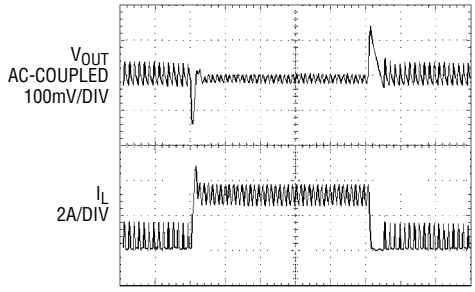
Efficiency vs Load Current



Efficiency vs Load Current

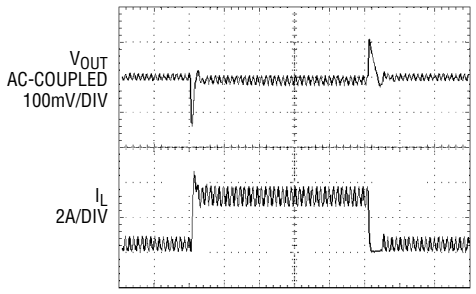


Load Step (Burst Mode Operation)



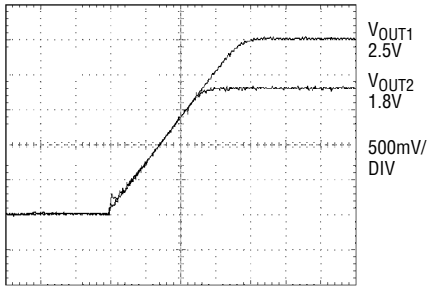
VIN = 3.3V 200µs/DIV
VOUT = 1.8V
ILOAD = 300mA TO 3A
SYNC/MODE = VIN
FIGURE 13 CIRCUIT

Load Step (Pulse Skipping Mode)



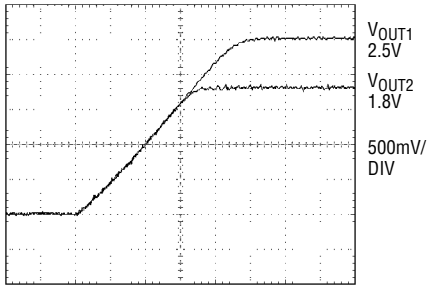
VIN = 3.3V 200µs/DIV
VOUT = 1.8V
ILOAD = 300mA TO 3A
SYNC/MODE = 0V
FIGURE 13 CIRCUIT

Tracking Start-Up with Internal Soft-Start (C_{SS} = 0nF)



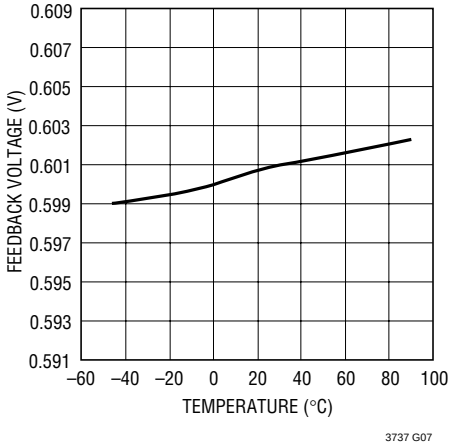
VIN = 4.2V 250µs/DIV
RLOAD1 = RLOAD2 = 1Ω
FIGURE 13 CIRCUIT

Tracking Start-Up with External Soft-Start (C_{SS} = 10nF)

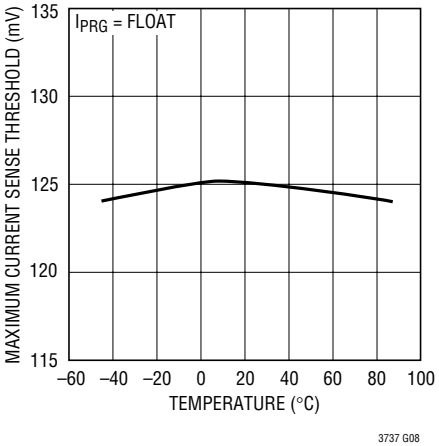


VIN = 4.2V 2.5ms/DIV
RLOAD1 = RLOAD2 = 1Ω
FIGURE 13 CIRCUIT

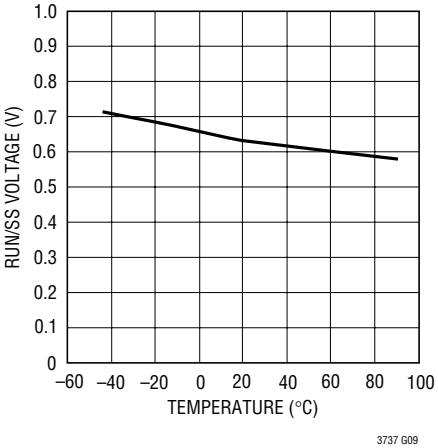
Regulated Feedback Voltage vs Temperature



Maximum Current Sense Threshold vs Temperature

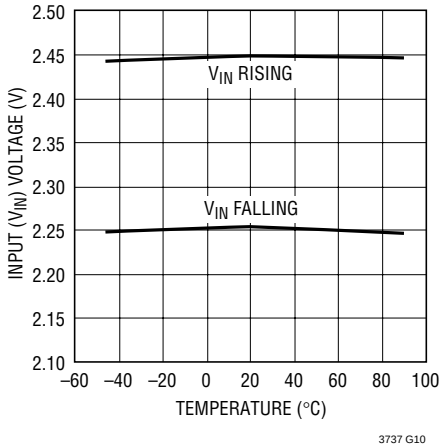


Shutdown (RUN) Threshold vs Temperature

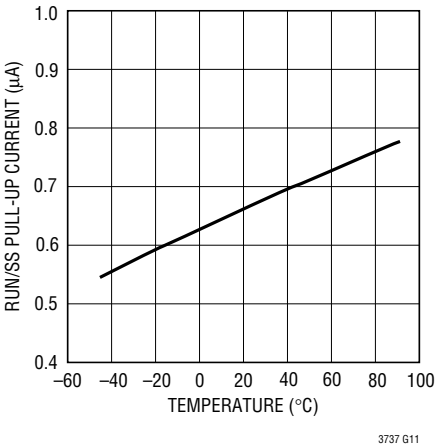


TYPICAL PERFORMANCE CHARACTERISTICS

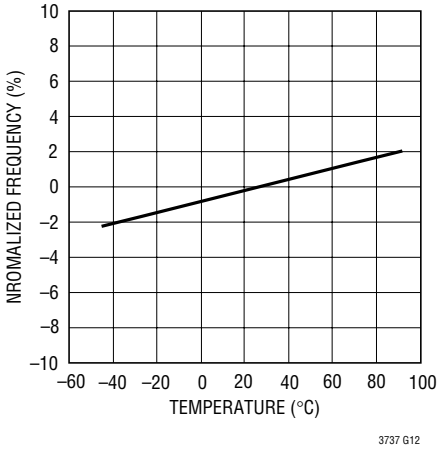
Undervoltage Lockout Threshold vs Temperature



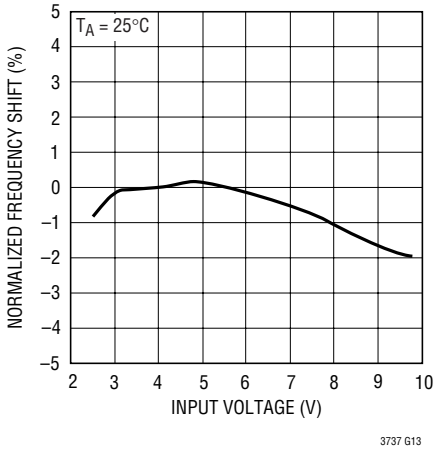
RUN/SS Pull-Up Current vs Temperature



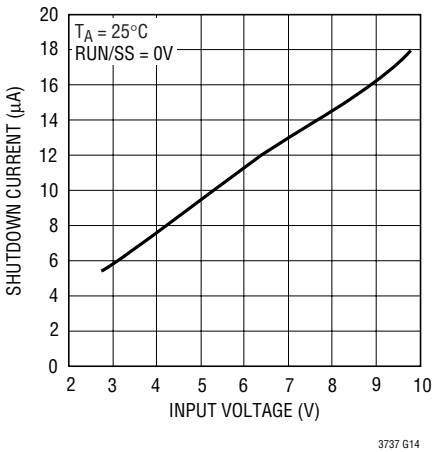
Oscillator Frequency vs Temperature



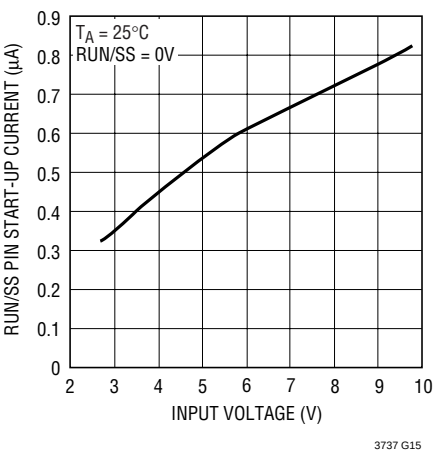
Oscillator Frequency vs Input Voltage



Shutdown Quiescent Current vs Input Voltage



RUN/SS Start-Up Current vs Input Voltage



PIN FUNCTIONS (QFN/SSOP)

I_{TH1}, I_{TH2} (Pins 1, 8/Pins 4, 11): Current Threshold and Error Amplifier Compensation Point. Nominal operating range on these pins is from 0.7V to 2V. The voltage on this pin determines the threshold of the main current comparator.

PLLLPF (Pin 3/Pin 6): Frequency Set/PLL Lowpass Filter. When synchronizing to an external clock, this pin serves as the lowpass filter point for the phase-locked loop. Normally, a series RC is connected between this pin and ground.

When not synchronizing to an external clock, this pin serves as the frequency select input. Tying this pin to GND selects 300kHz operation; tying this pin to V_{IN} selects 750kHz operation. Floating this pin selects 550kHz operation.

SGND (Pin 4/Pin 7): Signal Ground. This pin serves as the ground connection for most internal circuits.

V_{IN} (Pin 5/Pin 8): Chip Signal Power Supply. This pin powers the entire chip except for the gate drivers. Externally filtering this pin with a lowpass RC network (e.g., R = 10Ω, C = 1µF) is suggested to minimize noise pickup, especially in high load current applications.

TRACK (Pin 6/Pin 9): Tracking Input for Second Controller. This pin allows the start-up of V_{OUT2} to "track" that of V_{OUT1} according to a ratio established by a resistor divider on V_{OUT1} connected to the TRACK pin. For one-to-one tracking of V_{OUT1} and V_{OUT2} during start-up, a resistor divider with values equal to those connected to V_{FB2} from V_{OUT2} should be used to connect to TRACK from V_{OUT1}.

PGOOD (Pin 9/Pin 12): Power Good Output Voltage Monitor Open-Drain Logic Output. This pin is pulled to ground when the voltage on either feedback pin (V_{FB1}, V_{FB2}) is not within ±13.3% of its nominal set point.

NC (Pins 13, 19/Pins 16, 22): No Connect.

RUN/SS (Pin 14/Pin 17): Run Control Input and Optional External Soft-Start Input. Forcing this pin below 0.65V shuts down the chip (both channels). Driving this pin to V_{IN} or releasing this pin enables the chip to start-up with the internal soft-start. An external soft-start can be programmed by connecting a capacitor between this pin and ground.

PGND (Pin 16/Pin 19): Power Ground. This pin serves as the ground connection for the gate drivers.

PGATE1, PGATE2 (Pins 17, 15/Pins 20, 18): Gate Drives for External P-Channel MOSFETs. These pins have an output swing from PGND to $SENSE^+$.

SYNC/MODE (Pin 18/Pin 21): External Clock Synchronization and Burst Mode/Pulse Skipping Select. Applying a clock with frequency between 250kHz to 850kHz causes the internal oscillator to phase lock to the external clock, and disables Burst Mode operation but allows pulse skipping at low load currents. Forcing this pin high enables Burst Mode operation. Forcing this pin low enables pulse-skipping mode. In these cases, the frequency of the internal oscillator is set by the voltage on the PLLLPF pin. Do not let this pin float.

PV_{IN1}, PV_{IN2} (Pins 20, 12/Pins 23, 15): Powers of the Gate Drivers.

$SENSE1^+$, $SENSE2^+$ (Pins 21, 11/Pins 24, 14): Positive Inputs to Differential Current Comparators. Normally connected to the sources of the external P-channel MOSFETs.

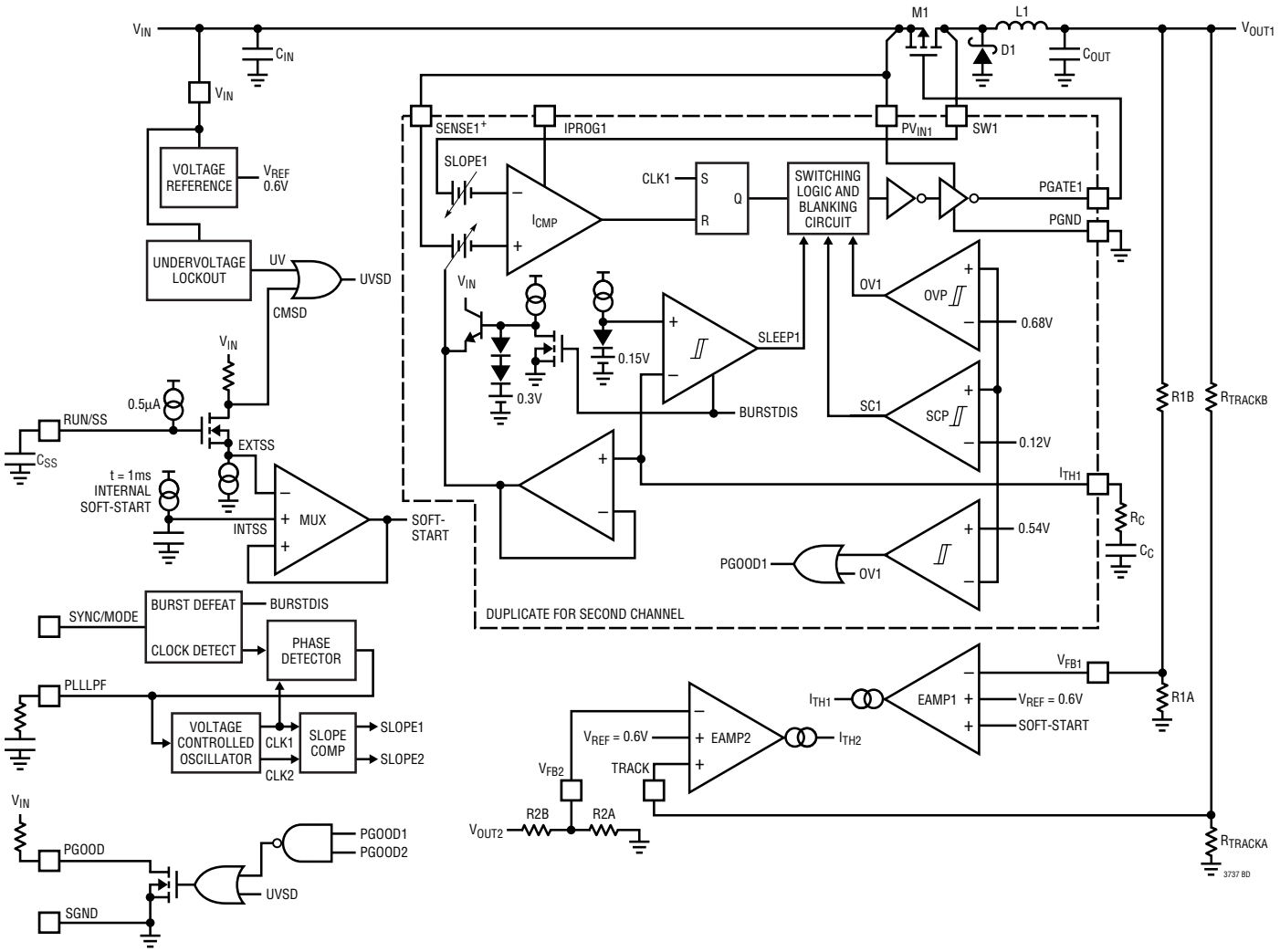
SW1 ($SENSE1^-$), SW2 ($SENSE2^-$) (Pins 22, 10/Pins 1, 13): Switch Node Connections to Inductors. Also the negative inputs to differential peak current comparators. Normally connected to the drains of the external P-Channel MOSFETs and the inductor when not using a sense resistor. When a sense resistor is used, it will be connected between SW and $SENSE^+$.

IPRG1, IPRG2 (Pins 23, 2/Pins 2, 5): Three-State Pins to Select Maximum Peak Sense Voltage Threshold. These pins select the maximum allowed voltage drop between the $SENSE^+$ and SW pins (i.e., the maximum allowed drop across the external P-channel MOSFET) for each channel. Tie high, low or float to select 204mV, 85mV or 125mV, respectively.

V_{FB1}, V_{FB2} (Pins 24, 7/Pins 3, 10): Each receives the remotely sensed feedback voltage for its controller from an external resistive divider across the output.

Exposed Pad (Pin 25/NA): Exposed Pad is PGND and must be soldered to PCB.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3737 uses a constant frequency, current mode architecture with the two controller channels operating 180 degrees out of phase. During normal operation, each external P-channel power MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the current comparator (I_{CMP}) resets the latch. The peak inductor current at which I_{CMP} resets the RS latch is determined by the voltage on the I_{TH} pin, which is the output of each error amplifier (EAMP). The V_{FB} pin receives the output voltage feedback signal from an external resistor divider. This feedback signal is compared to the internal 0.6V reference voltage by the EAMP. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn, causes the I_{TH} voltage to increase until the average inductor current matches the new load current.

Shutdown, Soft-Start and Tracking Start-Up (RUN/SS and TRACK Pins)

The LTC3737 is shut down by pulling the RUN/SS pin low. In shutdown, all controller functions are disabled and the chip draws only 9μA. The PGATE outputs are held high (off) in shutdown. Releasing RUN/SS allows an internal 0.7μA current source to charge up the RUN/SS pin. When the RUN/SS pin reaches 0.65V, the LTC3737's two controllers are enabled.

The start-up of V_{OUT1} is controlled by the LTC3737's internal soft-start. During soft-start, the error amplifier EAMP compares the feedback signal V_{FB1} to the internal soft-start ramp (instead of the 0.6V reference), which rises linearly from 0V to 0.6V in about 1ms. This allows the output voltage to rise smoothly from 0V to its final value, while maintaining control of the inductor current.

The 1ms soft-start time can be increased by connecting the optional external soft-start capacitor, C_{SS}, between the RUN/SS and SGND pins. As the RUN/SS pin continues to rise linearly from approximately 0.65V to 1.3V (being charged by the internal 0.7μA current source), the EAMP regulates V_{FB1} linearly from 0V to 0.6V.

The start-up of V_{OUT2} is controlled by the voltage on the TRACK pin. When the voltage on the TRACK pin is less than the 0.6V internal reference, the LTC3737 regulates the V_{FB2} voltage to the TRACK pin instead of the 0.6V reference. Typically, a resistor divider on V_{OUT1} is connected to the TRACK pin to allow the start-up of V_{OUT2} to "track" that of V_{OUT1}. For one-to-one tracking during start-up, the resistor divider would have the same values as the divider on V_{OUT2} that is connected to V_{FB2}.

If no tracking function is desired, then the TRACK pin can be tied to V_{IN}. Note, however, that in this situation, there would be no (internal or external) soft-start on V_{OUT2}.

Light Load Operation (Burst Mode Operation or Pulse Skipping Mode) (SYNC/MODE Pin)

The LTC3737 can be enabled to enter high efficiency Burst Mode operation at low load currents. To select Burst Mode operation, tie the SYNC/MODE pin to a DC voltage above 0.6V (e.g., V_{IN}). To disable Burst Mode operation and enable PWM pulse skipping mode, connect SYNC/MODE to a DC voltage below 0.6V (e.g., SGND). In this mode, the efficiency is lower at light loads. However, pulse skipping mode has the advantages of lower output ripple and less interference to audio circuitry.

When a controller is in Burst Mode operation, the peak current in the inductor is set to approximate one-fourth of the maximum sense voltage even when the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is greater than the load current, the EAMP will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.85V, the internal SLEEP signal goes high and the external MOSFET is turned off.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3737 draws. The load current is supplied by the output capacitor. As the output voltage decreases, the EAMP increases the I_{TH} voltage. When the I_{TH} voltage reaches 0.925V, the SLEEP signal goes low and the controller resumes normal operation by turning on the external P-channel MOSFET on the next cycle of the internal oscillator.

When the SYNC/MODE pin is clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop), the LTC3737 operates in PWM pulse skipping mode at light loads.

OPERATION (Refer to Functional Diagram)

When a controller is in pulse skipping operation, an internal offset at the current comparator input will assure that the current comparator remains tripped even at zero load current and the regulator will start to skip cycles, as it must, in order to maintain regulation.

Short-Circuit Protection

When one of the outputs is shorted to ground (V_{FB} < 0.12V), the switching frequency of that controller is reduced to 1/3 of the normal operating frequency. The other controller is unaffected and maintains normal operation.

The short-circuit threshold on V_{FB2} is based on the smaller of 0.12V and a fraction of the voltage on the TRACK pin. This also allows V_{OUT2} to start up and track V_{OUT1} more easily. Note that if V_{OUT1} is truly short circuited ($V_{OUT1} = V_{FB1} = 0V$), then the LTC3737 will try to regulate V_{OUT2} to 0V if a resistor divider on V_{OUT1} is connected to the TRACK pin.

Output Overvoltage Protection

As a further protection, the overvoltage comparator (OVP) guards against transient overshoots, as well as other more serious conditions, that may overvoltage the output. When the feedback voltage on the V_{FB} pin has risen 13.33% above the reference voltage of 0.6V, the external P-channel MOSFET is turned off until the overvoltage is cleared.

Frequency Selection and Phase-Locked Loop (PLLLPF and SYNC/MODE Pins)

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3737's controllers can be selected using the PLLLPF pin. If the SYNC/MODE pin is not being driven by an external clock source, the PLLLPF pin can be floated, tied to V_{IN} or tied to SGND to select 550kHz, 750kHz or 300kHz, respectively.

A phase-locked loop (PLL) is available on the LTC3737 to synchronize the internal oscillator to an external clock source that is connected to the SYNC/MODE pin. In this case, a series RC should be connected between the PLLLPF pin and SGND to serve as the PLL's loop filter. The LTC3737 phase detector adjusts the voltage on the PLLLPF pin to align the turn-on of controller 1's external P-channel MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external P-channel MOSFET is 180 degrees out of phase to the rising edge of the external clock source.

The typical capture range of the LTC3737's phase-locked loop is from approximately 200kHz to 1MHz, with a guarantee over all variations and temperature to be between 250kHz and 850kHz. In other words, the LTC3737's PLL is guaranteed to lock to an external clock source whose frequency is between 250kHz and 850kHz.

Dropout Operation

When the input supply voltage (V_{IN}) decreases towards the output voltage, the rate of change of the inductor current while the external P-channel MOSFET is on (ON cycle) decreases. This reduction means that the P-channel MOSFET will remain on for more than one oscillator cycle if the inductor current has not ramped up to the threshold set by the EAMP on the I_{TH} pin. Further reduction in the input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%; i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

Undervoltage Lockout

To prevent operation of the P-channel MOSFET below safe input voltage levels, an undervoltage lockout is incorporated in the LTC3737. When the input supply voltage (V_{IN}) drops below 2.25V, the external P-channel MOSFET and all internal circuitry are turned off except for the undervoltage block, which draws only a few microamperes.

OPERATION (Refer to Functional Diagram)

Peak Current Sense Voltage Selection and Slope Compensation (IPRG1 and IPRG2 Pins)

When a controller is operating below 20% duty cycle, the peak current sense voltage (between the SENSE+ and SW pins) allowed across the external P-channel MOSFET is determined by:

$$\Delta V_{SENSE(MAX)} = \frac{A(V_{ITH} - 0.7V)}{10}$$

where A is a constant determined by the state of the IPRG pins.

Floating the IPRG pin selects A = 1; tying IPRG to V_{IN} selects A = 5/3; tying IPRG to SGND selects A = 2/3. The maximum value of V_{ITH} is typically about 1.98V, so the maximum sense voltage allowed across the external P-channel MOSFET is 125mV, 85mV or 204mV for the three respective states of the IPRG pin. The peak sense voltages for the two controllers can be independently selected by the IPRG1 and IPRG2 pins.

However, once the controller's duty cycle exceeds 20%, slope compensation begins and effectively reduces the peak sense voltage by a scale factor given by the curve in Figure 2.

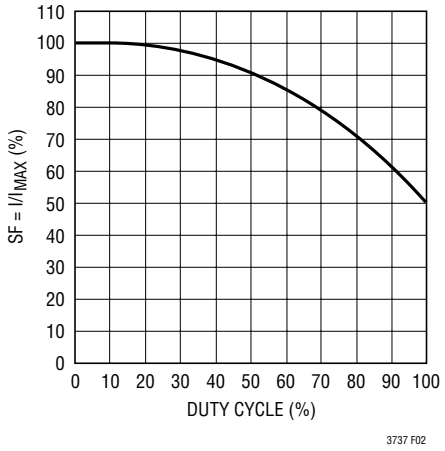


Figure 2. Maximum Peak Current vs Duty Cycle

The peak inductor current is determined by the peak sense voltage and the on-resistance of the external P-channel MOSFET:

$$I_{PK} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

Power Good (PGOOD) Pin

A window comparator monitors both feedback voltages and the open-drain PGOOD output pin is pulled low when either or both feedback voltages are not within ±10% of the 0.6V reference voltage. PGOOD is low when the LTC3737 is shutdown or in undervoltage lockout.

2-Phase Operation

Why the need for 2-phase operation? Until recently, constant frequency dual switching regulators operated both controllers in phase (i.e., single phase operation). This means that both topside MOSFETs (P-channel) are turned on at the same time, causing current pulses of up to twice the amplitude of those from a single regulator to be drawn from the input capacitor. These large amplitude pulses increase the total RMS current flowing in the input capacitor, requiring the use of larger and more expensive input capacitors, and increase both EMI and power losses in the input capacitor and input power supply.

With 2-phase operation, the two controllers of the LTC3737 are operated 180 degrees out of phase. This effectively interleaves the current pulses coming from the topside MOSFET switches, greatly reducing the time where they overlap and add together. The result is a significant reduction in the total RMS current, which in turn allows the use of smaller, less expensive input capacitors, reduces shielding requirements for EMI and improves real world operating efficiency.

Figure 3 shows qualitatively example waveforms for a single phase dual controller versus a 2-phase LTC3737 system. In this case, 2.5V and 1.8V outputs, each drawing

OPERATION (Refer to Functional Diagram)

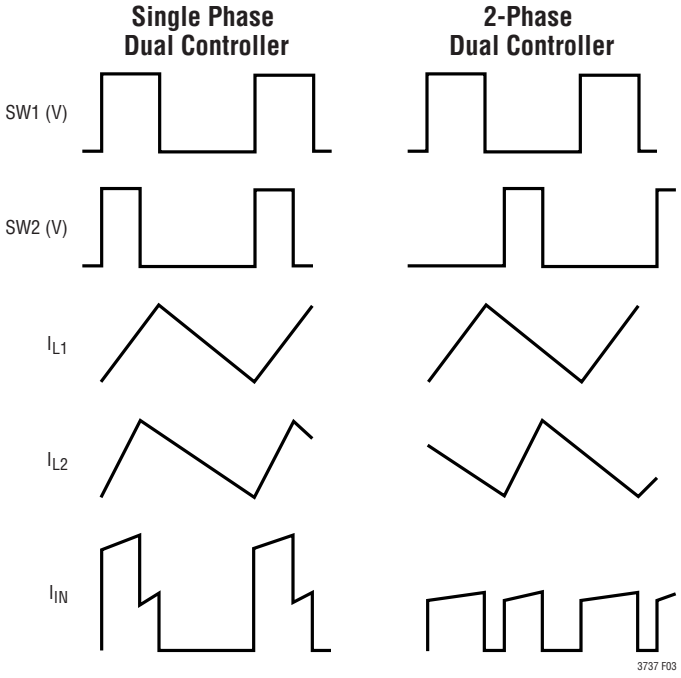


Figure 3. Example Waveforms for a Single Phase Dual Controller vs the 2-Phase LTC3737

a load current of 2A, are derived from a 7V (e.g., a 2-cell Li-Ion battery) input supply. In this example, 2-phase operation would reduce the RMS input capacitor current from $1.79A_{RMS}$ to $0.91A_{RMS}$. While this is an impressive reduction by itself, remember that power losses are proportional to I_{RMS}^2, meaning that actual power wasted is reduced by a factor of 3.86.

The reduced input ripple current also means that less power is lost in the input power path, which could include batteries, switches, trace/connector resistances, and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage. Significant cost and board footprint savings are also realized by being able to use smaller, less expensive, lower RMS current-rated, input capacitors.

Of course the improvement afforded by 2-phase operation is a function of the relative duty cycles of the two controllers, which in turn are dependent upon the input supply voltage. Figure 4 depicts how the RMS input current varies for single phase and 2-phase dual controllers with 2.5V and 1.8V outputs over a wide input voltage range.

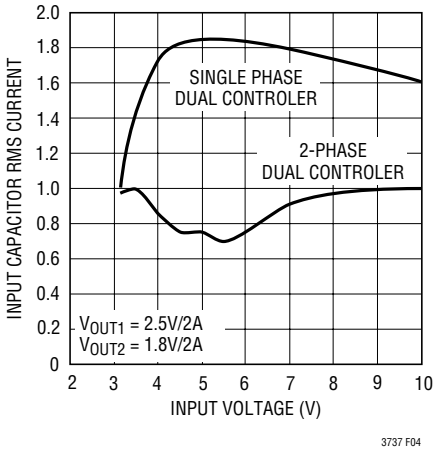


Figure 4. RMS Input Current Comparison

It can be readily seen that the advantages of 2-phase operation are not limited to a narrow operating range, but in fact extend over a wide region. A good rule of thumb for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

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The typical LTC3737 application circuit is shown in Figure 1. External component selection for each of the LTC3737's controllers is driven by the load requirement and begins with the selection of the inductor (L) and the power MOSFET M1. Next, the output diode D1 is selected. Finally C_{IN} and C_{OUT} are chosen.

Power MOSFET Selection

An external P-channel MOSFET must be selected for use with each channel of the LTC3737. The main selection criteria for the power MOSFET are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and the total gate charge Q_G.

The gate drive voltage is the input supply voltage. Since the LTC3737 is designed for operation down to low input voltages, a sublogic level MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC3737 is less than the absolute maximum MOSFET V_{GS} rating, which is typically 8V.

The P-channel MOSFET's on-resistance is chosen based on the required load current. The maximum average output load current, $I_{OUT(MAX)}$, is equal to the peak inductor current minus half the peak-to-peak ripple current, I_{RIPPLE}. The LTC3737's current comparator monitors the drain-to-source voltage, V_{DS}, of the P-channel MOSFET, which is sensed between the SENSE+ and SW pins. The peak inductor current is limited by the current threshold, set by the voltage on the I_{TH} pin, of the current comparator. The voltage on the I_{TH} pin is internally clamped, which limits the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ to approximately 125mV when IPRG is floating (85mV when IPRG is tied low; 204mV when IPRG is tied high).

The output current that the LTC3737 can provide is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation).

A reasonable starting point is setting ripple current I_{RIPPLE} to be 40% of $I_{OUT(MAX)}$. Rearranging the above equation yields:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}} \text{ for Duty Cycle} < 20\%$$

However, for operation above 20% duty cycle, slope compensation has to be taken into consideration to select the appropriate value of $R_{DS(ON)}$ to provide the required amount of load current:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

where SF is a scale factor whose value is obtained from the curve in Figure 2.

These must be further derated to take into account the significant variation in on-resistance with temperature. The following equation is a good guide for determining the required $R_{DS(ON)MAX}$ at 25°C (manufacturer's specification), allowing some margin for variations in the LTC3737 and external component values:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho T}$$

The ρ_T is a normalizing term accounting for the temperature variation in on-resistance, which is typically about 0.4%/°C, as shown in Figure 5. Junction to case temperature T_{JC} is

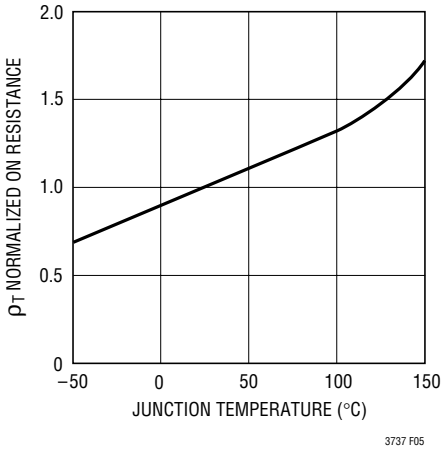


Figure 5. $R_{DS(ON)}$ vs Temperature

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about 10°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{80°C} \sim 1.3$ in the above equation is a reasonable choice.

The power dissipated in the MOSFET strongly depends on its respective duty cycles and load current. When the LTC3737 is operating in continuous mode, the duty cycles for the MOSFET are:

$$\text{Duty Cycle} = \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

The MOSFET power dissipations at maximum output current are:

$$P_P = \frac{V_{OUT} + V_D}{V_{IN} + V_D} \bullet \left(I_{OUT(MAX)}\right)^2 \bullet \rho_T \bullet R_{DS(ON)} + k \bullet V_{IN}^2 \bullet I_{OUT(MAX)} \bullet \rho_T \bullet R_{DS(ON)}$$

The MOSFET has I^2R losses and the P_P equation includes an additional term for transition losses, which are largest at high input voltages. The constant $k = 2A^{-1}$ can be used to estimate the amount of transition loss.

Using a Sense Resistor

A sense resistor R_{SENSE} can be connected between SENSE+ and SW to sense the output load current. In this case, the source of the P-channel MOSFET is connected to the SW pin and the drain is not connected to any pin of the LTC3737. Therefore, the current comparator monitors the voltage developed across R_{SENSE} instead of V_{DS} of the P-channel MOSFET. The output current that the LTC3737 can provide in this case is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}$$

Setting ripple current as 40% of $I_{OUT(MAX)}$ and using Figure 2 to choose SF, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{5}{6} \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

(See the $R_{DS(ON)}$ selection in Power MOSFET Selection).

Variation in the resistance of a sense resistor is much smaller than the variation in on-resistance of the external MOSFET. Therefore the load current is well controlled, and the system is more stable with a sense resistor. However the sense resistor causes extra I^2R losses in addition to the I^2R losses of the MOSFET. Therefore, using a sense resistor lowers the efficiency of LTC3737, especially for large load current.

Operating Frequency and Synchronization

The choice of operating frequency, f_{OSC}, is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The internal oscillator for each of the LTC3737's controllers runs at a nominal 550kHz frequency when the PLLLPF pin is left floating and the SYNC/MODE pin is a DC low or high. Pulling the PLLLPF to V_{IN} selects 750kHz operation; pulling the PLLLPF to GND selects 300kHz operation.

Alternatively, the LTC3737 will phase lock to a clock signal applied to the SYNC/MODE pin with a frequency between 250kHz and 850kHz (see Phase-Locked Loop and Frequency Synchronization).

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \left(V_{IN} - V_{OUT}\right)\left(\frac{\left(V_{OUT} + V_D\right) / \left(V_{IN} + V_D\right)}{f_{OSC} \bullet L}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee

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that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

Burst Mode Operation Considerations

The choice of $R_{DS(ON)}$ and inductor value also determines the load current at which the LTC3737 enters Burst Mode operation. When bursting, the controller clamps the peak inductor current to approximately:

$$I_{BURST(PEAK)} = \frac{1}{4} \bullet \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

The corresponding average current depends on the amount of ripple current. Lower inductor values (higher I_{RIPPLE}) will reduce the load current at which Burst Mode operation begins.

The ripple current is normally set so that the inductor current is continuous during the burst periods. Therefore,

$$I_{RIPPLE} \leq I_{BURST(PEAK)}$$

This implies a minimum inductance of:

$$L_{MIN} \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{BURST(PEAK)}} \bullet \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

A smaller value than L_{MIN} could be used in the circuit, although the inductor current will not be continuous during burst periods, which will result in slightly lower efficiency. In general, though, it is a good idea to keep I_{RIPPLE} comparable to $I_{BURST(PEAK)}$.

Inductor Core Selection

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. Core saturation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when several layers of wire can be used, while inductors wound on bobbins are generally easier to surface mount. However, designs for surface mount that do not increase the height significantly are available from Coiltronics, Coilcraft, Dale and Sumida.

Output Diode Selection

The catch diode carries load current during the switch off time of the power MOSFETs . The average diode current is therefore dependent on the P-channel MOSFET duty cycle. At high input voltages, the diode conducts most of the time. As V_{IN} approaches V_{OUT}, the diode conducts for only a small fraction of the time. The most stressful condition for the diode is when the output is short circuited. Under this condition, the diode must safely handle I_{PEAK} at close to 100% duty cycle. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode's ratings.

Under normal conditions, the average current conducted by the diode is:

$$I_D = \frac{V_{IN} - V_{OUT}}{V_{IN} + V_D} \bullet I_{OUT}$$

The allowable forward voltage drop in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{PEAK}}$$

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where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements.

A Schottky diode is a good choice for low forward drop and fast switching time. Remember to keep lead length short and observe proper grounding to avoid ringing and increased dissipation.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $V_{OUT} \bullet I_{OUT}$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle $(V_{OUT} + V_D)/(V_{IN} + V_D)$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX}}{V_{IN} + V_D}\left[(V_{OUT} + V_D)(V_{IN} - V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT} + V_D$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3737, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC3737 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The sources of the P-channel MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the sourced and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1μF to 1μF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3737, is also suggested. A 10Ω resistor placed between C_{IN} and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

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Setting Output Voltage

The LTC3737 output voltages are each set by an external feedback resistor divider carefully placed across the output, as shown in Figure 6. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

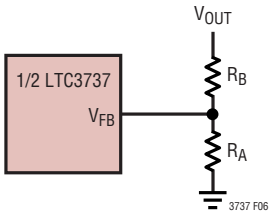


Figure 6. Setting Output Voltage

Run/Soft Start Function

The RUN/SS pin is a dual purpose pin that provides the optional external soft-start function and a means to shut down the LTC3737.

Pulling the RUN/SS pin below 0.65V puts the LTC3737 into a low quiescent current shutdown mode (I_Q = 9µA). If RUN/SS has been pulled all the way to ground, there will be a delay before the LTC3737 comes out of shutdown and is given by:

$$t_{DELAY} = 0.65V \bullet \frac{C_{SS}}{0.7\mu A} = 0.93s/\mu F \bullet C_{SS}$$

This pin can be driven directly from logic as shown in Figure 7. Diode D1 in Figure 7 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. This diode (and capacitor) can be deleted if the external soft-start is not needed.

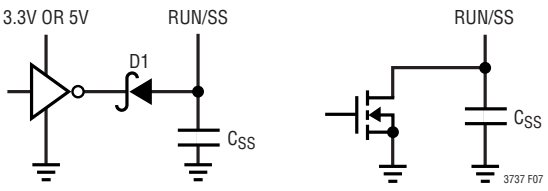


Figure 7. RUN/SS Pin Interfacing

During soft-start, the start-up of V_{OUT1} is controlled by slowly ramping the positive reference to the error amplifier from 0V to 0.6V, allowing V_{OUT1} to rise smoothly from 0V to its final value. The default internal soft-start time is 1ms. This can be increased by placing a capacitor between the RUN/SS pin and SGND. In this case, the soft start time will be approximately:

$$t_{SS1} = C_{SS} \bullet \frac{600mV}{0.7\mu A}$$

Tracking

The start-up of V_{OUT2} is controlled by the voltage on the TRACK pin. Normally this pin is used to allow the start-up of V_{OUT2} to track that of V_{OUT1} as shown qualitatively in Figures 8a and 8b. When the voltage on the TRACK pin is less than the internal 0.6V reference, the LTC3737 regulates the V_{FB2} voltage to the TRACK pin voltage instead of 0.6V. The start-up of V_{OUT2} may ratiometrically track that of V_{OUT1}, according to a ratio set by a resistor divider (Figure 8c):

$$\frac{V_{OUT1}}{V_{OUT2}} = \frac{R2A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R2B + R2A}$$

For coincident tracking (V_{OUT1} = V_{OUT2} during start-up),

$R2A = R_{TRACKA}$

$R2B = R_{TRACKB}$

The ramp time for V_{OUT2} to rise from 0V to its final value is:

$$t_{SS2} = t_{SS1} \bullet \frac{R_{TRACKA}}{R1A} \bullet \frac{R1A + R1B}{R_{TRACKA} + R_{TRACKB}}$$

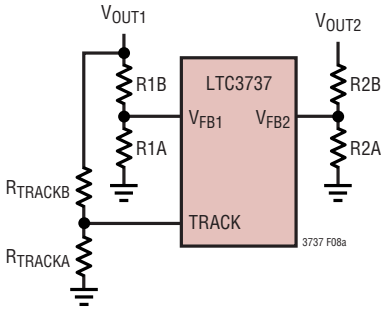
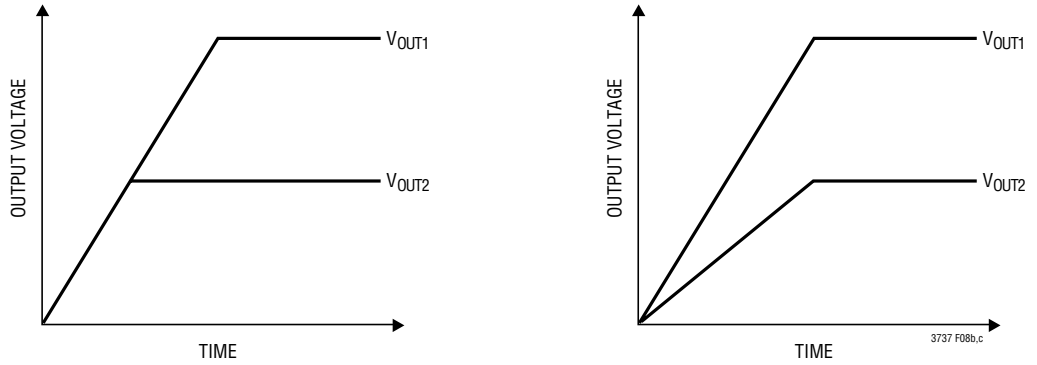


Figure 8a. Using the TRACK Pin

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(8b) Coincident Tracking **(8c) Ratiometric Tracking**

Figures 8b and 8c. Two Different Modes of Output Voltage Tracking

For coincident tracking,

$$t_{SS2} = t_{SS1} \bullet \frac{V_{OUT2F}}{V_{OUT1F}}$$

where V_{OUT1F} and V_{OUT2F} are the final, regulated values of V_{OUT1} and V_{OUT2}. V_{OUT1} should always be greater than V_{OUT2} when using the TRACK pin. If no tracking function is desired, then the TRACK pin may be tied to V_{IN}. However, in this situation there would be no (internal nor external) soft-start on V_{OUT2}.

Phase-Locked Loop and Frequency Synchronization

The LTC3737 has a phase-locked loop (PLL) comprised of an internal voltage controlled oscillator (VCO) and a phase detector. This allows the turn-on of the external P-channel MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the SYNC/MODE pin. The turn-on of controller 2's external P-channel MOSFET is thus 180 degrees out of phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLLPF pin. The relationship between the voltage on the PLLLPF pin and operating frequency, when there is a clock signal applied to SYNC/MODE, is shown in Figure 9 and specified in the electrical characteristics table. Note that the LTC3737 can only be synchronized to an external clock whose frequency is within range of the LTC3737's internal VCO, which is nominally 200kHz to 1MHz. This is guaranteed over temperature and variations to be between 250kHz and 850kHz. A simplified block diagram is shown in Figure 10.

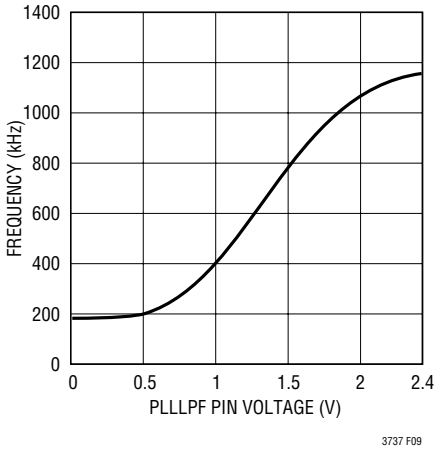


Figure 9. Relationship Between Oscillator Frequency and Voltage at the PLLLPF Pin

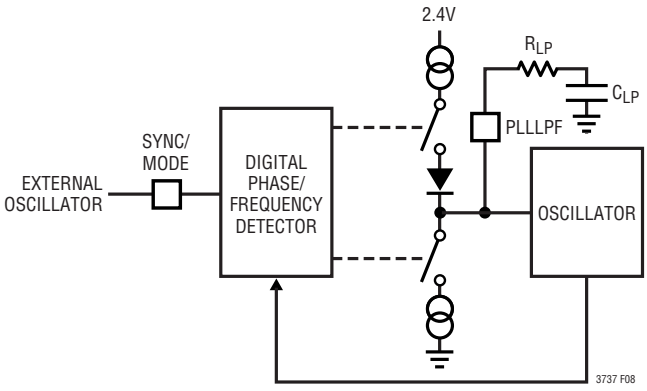


Figure 10. Phase-Locked Loop Block Diagram

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If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the PLLLPF pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLLLPF pin is adjusted until the phase and frequency of the external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF.

Typically, the external clock (on the SYNC/MODE pin) input high level is 1.6V, while the input low level is 1.2V. These levels are guaranteed to be TTL/CMOS compatible: 0.8V is guaranteed low, while 2.0V is guaranteed high.

Table 1 summarizes the different states in which the PLLLPF pin can be used.

Table 1

PLLLPF PIN	SYNC/MODE PIN	FREQUENCY
0V	DC Voltage	300kHz
Floating	DC Voltage	550kHz
V_{IN}	DC Voltage	750kHz
RC Loop Filter	Clock Signal	Phase-Locked to External Clock

Fault Condition: Short Circuit and Current Limit

To prevent excessive heating of the catch diode, foldback current limiting can be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diodes D_{FB1} and D_{FB2} between the output and the I_{TH} pin as shown in Figure 11. In a hard short (V_{OUT} = 0V), the current will be reduced to approximately 50% of the maximum output current.

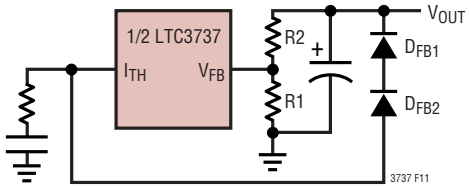


Figure 11. Foldback Current Limiting

Low Supply Operation

Although the LTC3737 can function down to below 2.4V, the maximum allowable output current is reduced as V_{IN} decreases below 3V. Figure 12 shows the amount of change as the supply is reduced down to 2.4V. Also shown is the effect on V_{REF}.

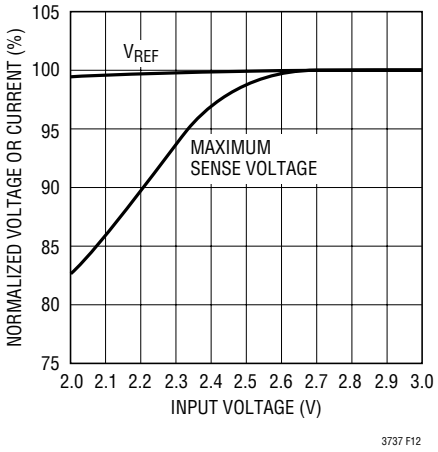


Figure 12. Line Regulation of V_{REF} and Maximum Sense Voltage

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LTC3737 is capable of turning the top P-channel MOSFET on and then off. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. The minimum on-time for the LTC3737 is typically about 250ns. Low duty cycle and high frequency applications may approach the minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT} + V_D}{f_{OSC} \bullet (V_{IN} + V_D)}$$

APPLICATIONS INFORMATION

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3737 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% - (L1 + L2 + L3 + …)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC3737 circuits: 1) LTC3737 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses, 4) voltage drop of the output diode and 5) transition losses.

1) The V_{IN} (pin) current is the DC supply current, given in the electrical characteristics, that excludes MOSFET driver currents. V_{IN} current results in a small loss that increases with V_{IN}.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from PV_{IN} to ground. The resulting dQ/dt is a current out of PV_{IN}, which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f \bullet Q_P$.

3) I^2R losses are calculated from the DC resistances of the MOSFET, inductor and sense resistor. In continuous mode, the average output current flows through L but is "chopped" between the P-channel MOSFET and the output diode. The MOSFET $R_{DS(ON)}$ multiplied by duty cycle can be summed with the resistance of L to obtain I^2R losses.

4) The output diode is a major source of power loss at high currents and is worse at high input voltages. The diode loss is calculated by multiplying the forward voltage times the load current times the diode duty cycle.

5) Transition losses apply to the external MOSFET and increase with higher operating frequencies and input voltages. Transition losses can be estimated from:

Transition Loss = $2(V_{IN})^2 \bullet I_{O(MAX)} \bullet C_{RSS}(f)$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then returns V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The I_{TH} series R_C-C_C filter (see Functional Diagram) sets the dominant pole-zero loop compensation. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability. The gain of the loop will be increased by increasing R_C, and the bandwidth of the loop will be increased by decreasing C_C. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

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A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25)(C_{LOAD}). Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} will be operating from a maximum of 4.2V down to a minimum of 2.7V (powered by a single lithium-ion battery). Load current requirement is a maximum of 2.5A, but most of the time it will be in a standby mode requiring only 2mA. Efficiency at both low and high load currents is important. Burst Mode operation at light loads is desired. Output voltage is 2.5V. The IPRG pin will be tied to V_{IN}, so the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ is approximately 204mV.

$$\text{Maximum Duty Cycle} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_D} = 93\%$$

From Figure 2, SF = 57%.

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho_T}$$
$$= 0.027\Omega$$

A 0.025Ω Si3473DV P-channel MOSFET is close to this value.

The PLLLPF pin will be left floating, so the LTC3737 will operate at its default frequency of 550kHz. For continuous Burst Mode operation, the required minimum inductor value is:

$$L_{MIN} = \frac{4.2V - 2.5V}{550kHz\left(\frac{0.051V}{0.025\Omega}\right)}\left(\frac{2.5V + 0.3V}{4.2V + 0.3V}\right) = 1.40\mu H$$

PC Board Layout Checklist

When laying out the printed circuit board, use the following checklist to ensure proper operation of the LTC3737.

- The power loop (input capacitor, MOSFET, inductor, output diode, output capacitor) of each channel should be as small as possible and isolated as much as possible from the other channel's power loop. It is better to have two separate, smaller valued input capacitors (e.g., two 10µF—one for each channel) than it is to have a single larger valued capacitor (e.g., one 22µF) that the channels share with a common connection.
- The signal and power grounds should be kept separate. The signal ground consists of the feedback resistor dividers, I_{TH} compensation networks and the SGND pin.

  The power grounds consist of the (–) terminal of the input and output capacitors, the anode of the Schottky diodes and the PGND pins. Each channel should have its own power ground for its power loop as described above. The power grounds for the two channels should connect together at a common point. It is most important to keep the ground paths with high switching currents away from each other.
- Put the feedback resistors close to the V_{FB} pins. The I_{TH} compensation components should also be very close to the LTC3737.
- The current sense traces ($SENSE^+$ and $SENSE^-$/SW) should be Kelvin connections right at the P-channel MOSFET source and drain.
- Keep the switch nodes (SW1, SW2) and the gate driver nodes (PGATE1, PGATE2) away from the small-signal components, especially the opposite channel's feedback resistors, I_{TH} compensation components and the current sense pins ($SENSE^+$ and $SENSE^-$/SW).

APPLICATIONS INFORMATION

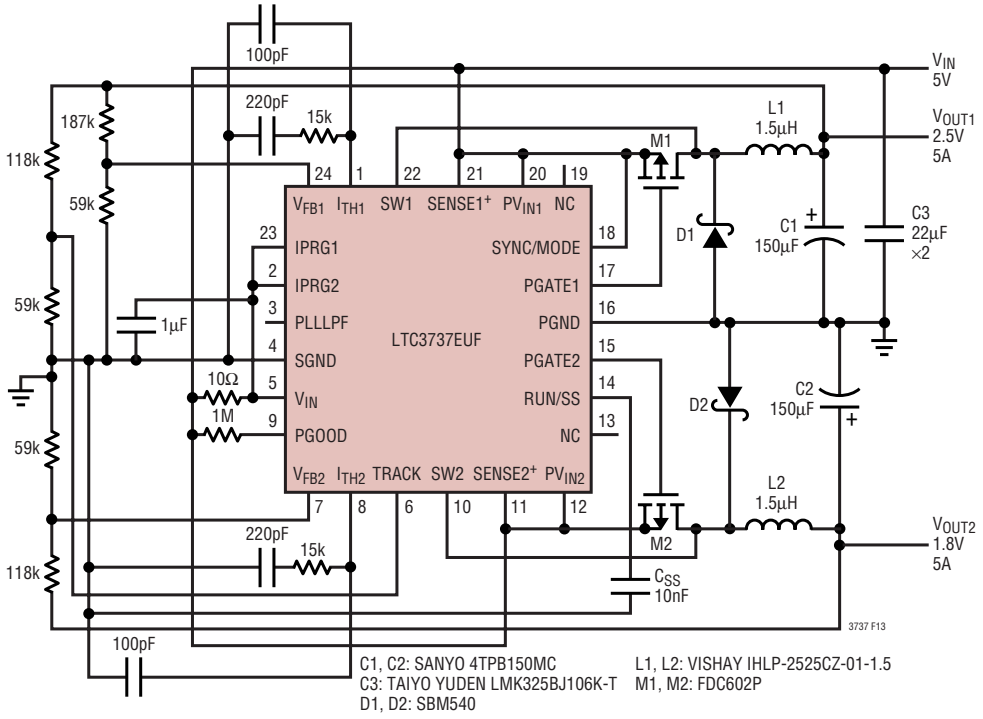
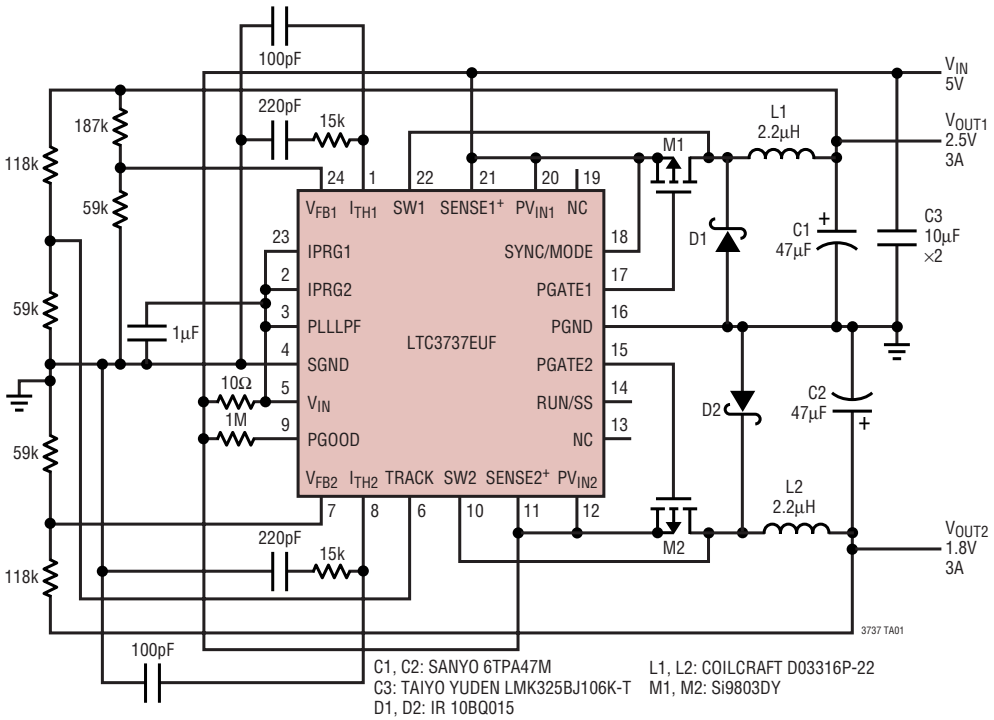


Figure 13. 2-Phase, 550kHz, Dual Output Step-Down DC/DC Converter

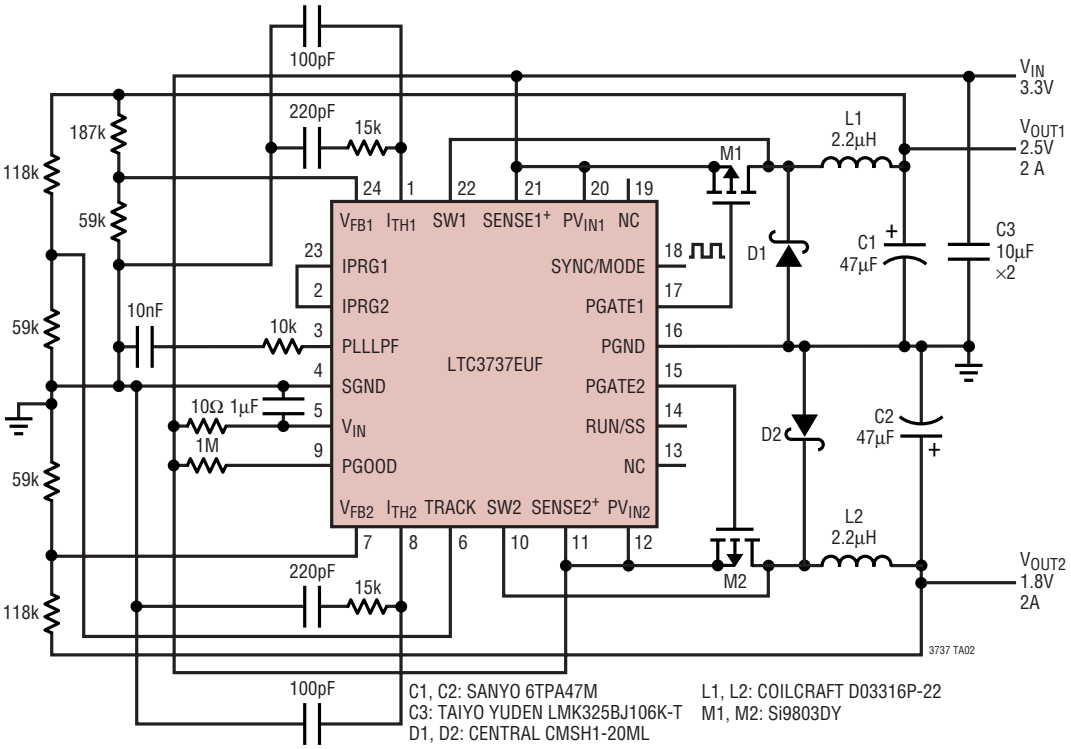
TYPICAL APPLICATIONS

2-Phase, 750kHz, Burst Mode Dual Output Step-Down DC/DC Converter

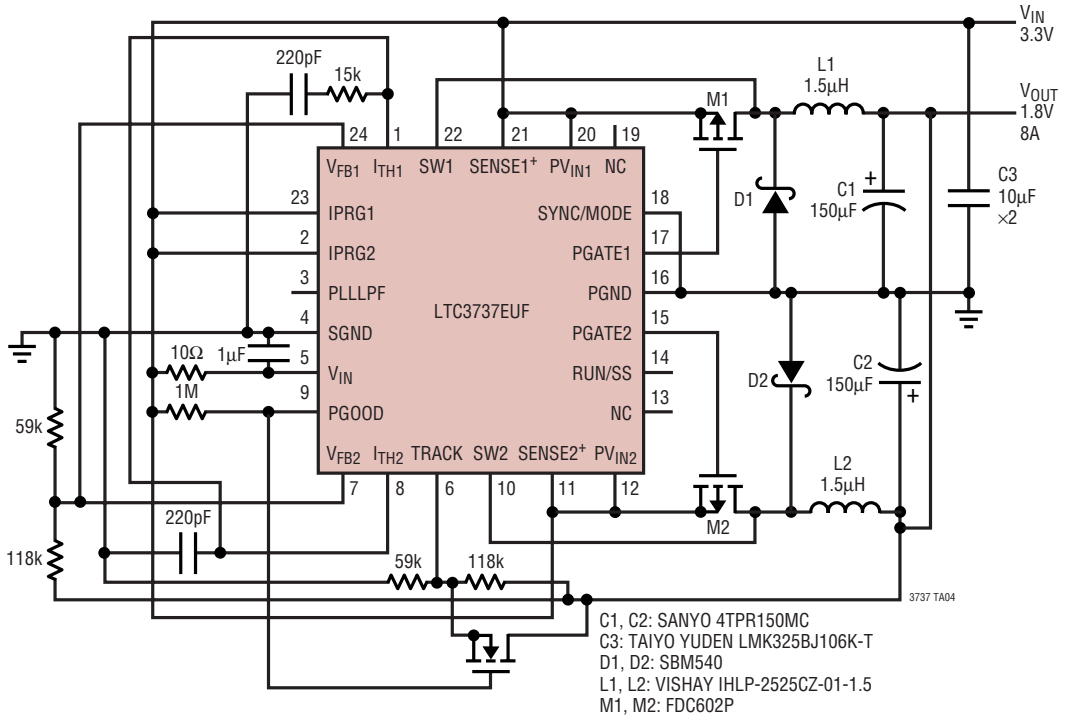


TYPICAL APPLICATIONS

2-Phase, Synchronizable Dual Output Step-Down DC/DC Converter

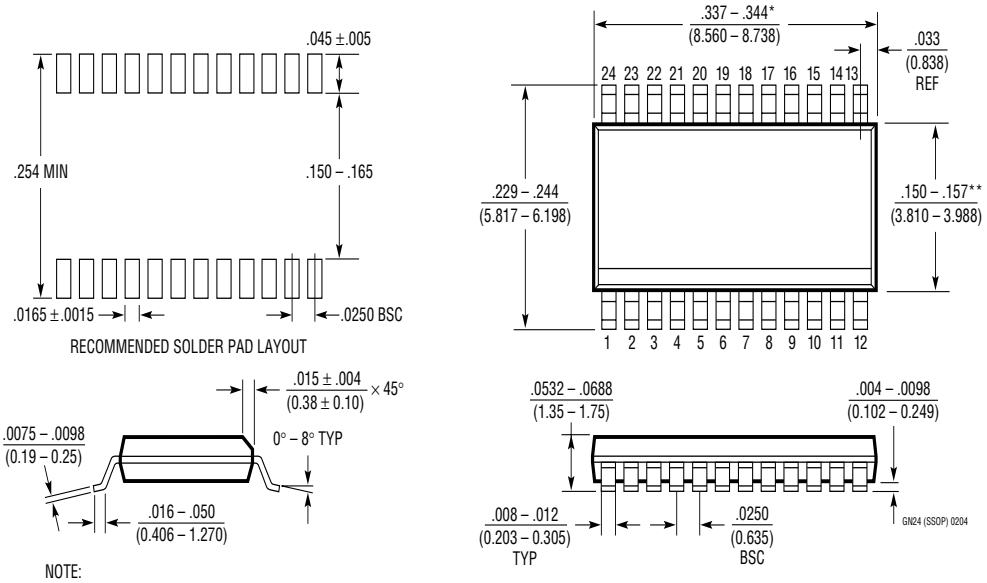


2-Phase, 550kHz, Single Output Step-Down DC/DC Converter ($3.3V_{IN}$ to $1.8V_{OUT}$ at 8A)



PACKAGE DESCRIPTION

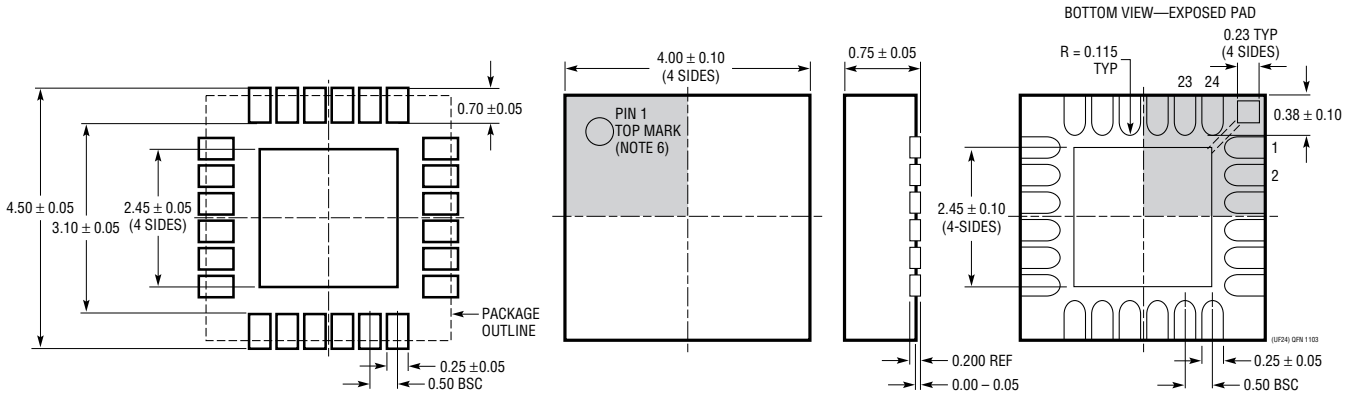
GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



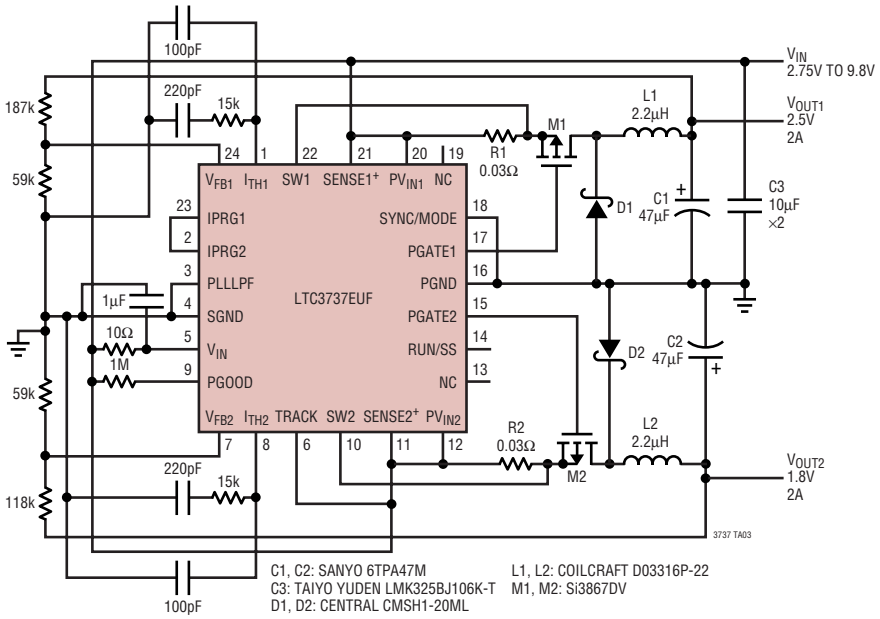
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

2-Phase, 300kHz, Resistor Sensing, Dual Output Step-Down DC/DC Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/LTC3728	Dual High Efficiency, 2-Phase Synchronous Step Down Controllers	Constant Frequency, Standby, 5V and 3.3V LDOs, V_{IN} to 36V, 28-Lead SSOP
LTC1629/LTC3729	20A TO 200A PolyPhase™ High Efficiency Controllers	Expandable Up to 12 Phases, No Heat Sinks, V_{IN} to 36V, 28-Lead SSOP
LTC1702A	No R_{SENSE}™ 2-Phase Dual Synchronous Controller	550kHz, No Sense Resistor, GN24, V_{IN} to 7V
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin Narrow SSOP, Fault Protection, $3.5V \le V_{IN} \le 36V$
LTC1772	Constant Frequency Current Mode Step-Down DC/DC Controller	$2.5V \le V_{IN} \le 9.8V$, I_{OUT} Up to 4A, SOT-23 Package, 550kHz
LTC1773	Synchronous Step-Down Controller	$2.65V \le V_{IN} \le 8.5V$, I_{OUT} Up to 4A, 10-Lead MSOP
LTC1778	No R_{SENSE} Synchronous Step-Down Controller	Current Mode Operation Without Sense Resistor, Fast Transient Response, $4V \le V_{IN} \le 36V$
LTC1872	Constant Frequency Current Mode Step-Up Controller	$2.5V \le V_{IN} \le 9.8V$, SOT-23 Package, 550kHz
LTC1929	Constant Frequency Current Mode 2-Phase Synchronous Controller	Up to 42A, No Heat Sink, $3.5V \le V_{IN} \le 36V$
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA, I_{SD} = <1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA, I_{SD} = <1µA, TSSOP-16E Package
LTC3700	Constant Frequency Step-Down Controller with LDO Regulator	$2.65 \le V_{IN} \le 9.8V$, 550kHz, 10-Lead SSOP
LTC3701	2-Phase, Low Input Voltage Dual Step-Down DC/DC Controller	$2.5V \le V_{IN} \le 9.8V$, 550kHz, PGOOD, PLL, 16-Lead SSOP
LTC3708	2-Phase, Dual Synchronous Controller with Output Tracking	Constant On-Time Dual Controller, V_{IN} Up to 36V, Very Low Duty Cycle Operation, 5mm × 5mm QFN Package
LTC3736	2-Phase, Dual Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, $0.6V \le V_{OUT} \le V_{IN}$, 4mm × 4mm QFN

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT/TP 0404 1K • PRINTED IN USA

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