300mA High PSRR Low Noise LDO

LM1101N5

General Description

The LM1101N5 performs ultra low drop voltage, high power supply rejection ratio (PSRR), fast response, low noise linear regulator, and designed to continuously deliver up to 300mA output current. The LM1101N5 has wide adjustable output voltage range and high output accuracy to 1.5%.
No by-pass capacitor is needed for this device and only 1μF ceramic capacitor is required for stability in any loading conditions. It reduces the amount of board space necessary for power applications.
The other features include soft start, current limit protection, Power-On-Reset function, and over temperature protection. The LM1101N5 is available in SOT-23-5 package.

Features

- Ultra Fast Response in Line/Load Transient
- Wide V_{IN} Range from 2.5V to 5.5V
- Adjustable Output Voltage from 0.8V to 4.5V
- Ultra Low Dropout Voltage: 200mV @300mA
- High Power Supply Rejection Ratio
  - 70dB at 1kHz
  - 60dB at 10kHz
- Ultra Low Output Noise Voltage 100μ$V_{(RMS)}$
- Low Shutdown Current < 1μA
- Only 1μF Ceramic Capacitor required for stability
- Over Temperature Protection
- Current Limit Protection
- RoHS Compliant and 100% Lead (Pb)-Free

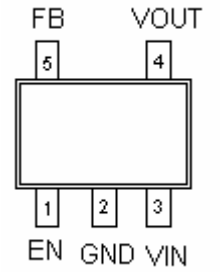
Applications

- Cellular Handsets
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Applications

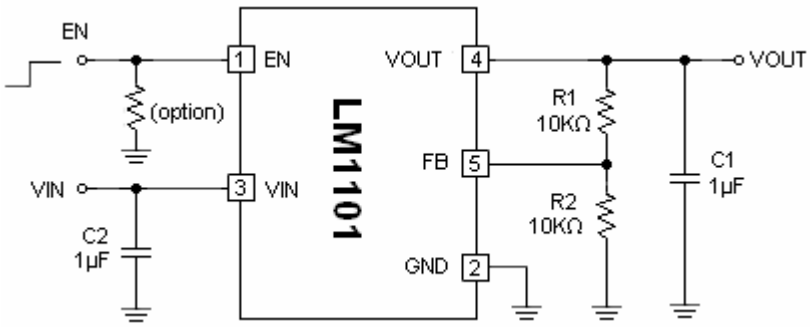
Ordering Information

Part Number	Package	Shipping
LM1101N5	SOT-23-5L (RoHS compliant package)	3000 pcs / Tape & Reel

Pin Configuration



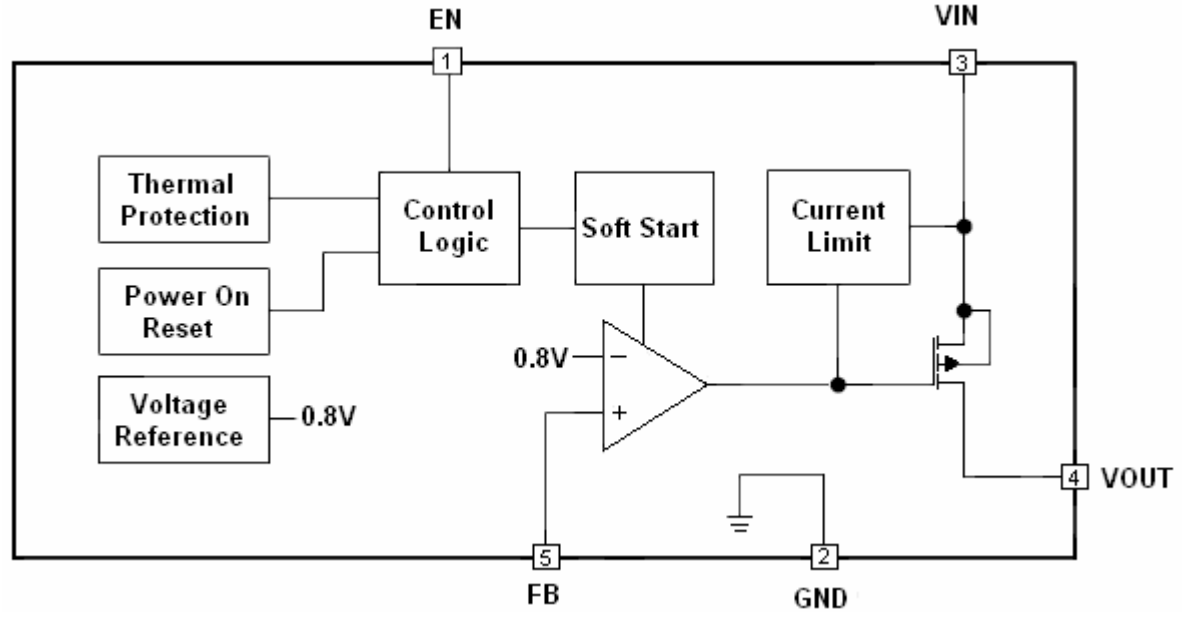
Typical Application Circuit



Pin Assignment

Pin Name	Pin No.	Pin Function
EN	1	**Chip Enable Input** (Active high).
GND	2	**Ground**.
VIN	3	**Input Voltage**. This is the source input to the power device that supplies current to the output pin.
VOUT	4	**Output Voltage**. VOUT is power output pin. An internal pull low resistance exists when the device is disabled. Minimum 1μF low ESR ceramic capacitor is required at this pin for stabilizing VOUT voltage.
FB	5	**Feedback Voltage**. FB is the non-inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage as $V_{OUT}= 0.8 * (1+R_1/R_2)(V)$. This pin has high impedance and should be kept from non-inverting input to noisy source to guarantee stable operation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- **V_{IN} ---------- -0.3V to +6.0V**
- **Other Pins---------- -0.3V to (V_{IN}+0.3V)**
- **Power Dissipation, P_D @ T_A = 25°C, SOT23-5 (Note 2) ---------- 0.4W**
- **Package Thermal Resistance, θ_{JA}, SOT23-5 (Note 2)---------- 250°C/W**
- **Package Thermal Resistance, θ_{JC}, SOT23-5 (Note 2)---------- 25°C/W**
- **Junction Temperature---------- 150°C**
- **Lead Temperature (Soldering, 10 sec.)---------- 260°C**
- **Storage Temperature ---------- -65°C to 150°C**
- **ESD susceptibility (Note3)**
  HBM (Human Body Mode)---------- 2KV
  MM (Machine Mode)---------- 200V

Recommended Operating Conditions (Note4)

Supply Input Voltage, V_{IN} ---------- +2.5V to +5.5V
Junction Temperature ---------- −40°C to 125°C
Ambient Temperature ---------- −40°C to 85°C

Electrical Characteristics @V_{IN}=5V, T_A=25℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Section						
Power Input Voltage	V_{IN}	V_{OUT}= V_{REF}	2.5	-	5.5	V
POR Threshold	V_{PORTH}		-	2.0	2.4	V
POR Hysteresis	V_{PORHYS}		-	0.1	-	V
Quiescent Current	I_Q	V_{IN}=V_{EN}=5V, I_{OUT}=0A	-	90	130	μA
Shutdown Current	I_{SD}	V_{IN}=5V,V_{EN}=0V	-	0.1	1	μA
Output Voltage						
Output Voltage Accuracy	V_{OUT}	V_{IN}=V_{EN}=5V, I_{OUT}=1mA	-1.5	-	1.5	%
Line Regulation	$V_{OUT(LINE)}$	2.5V<V_{IN}<5.0V, I_{OUT}=1mA, V_{OUT}=V_{REF}	-	-	0.2	%/V
Load Regulation	$V_{OUT(LOAD)}$	1mA<I_{OUT}<300mA,V_{IN}=V_{OUT}+0.5V	-	0.5	1	%/A
Output Voltage Noise		10Hz to 100kHz, C_{OUT}=1μF	-	100	-	$\mu V_{(RMS)}$
Power Supply Rejection Ratio	PSRR	I_{OUT}=10mA,1kHz	-	70	-	dB
		I_{OUT}=10mA,10kHz	-	60	-	
		I_{OUT}=10mA,100kHz	-	40	-	
Dropout Voltage	V_{DROP}	I_{OUT}=300mA, 2.5V < V_{OUT} < 3.3V	-	200	300	mV
Enable						
Enable High Level	V_{EN}		1.4	-	-	V
Disable Low Level	V_{SD}		-	-	0.4	V
Enable Input Current	I_{EN}	V_{EN}=5V or 0V	-1	0	1	μA
Output Voltage Ramp Up Time			-	600	-	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Over Current Protection						
OCP Threshold Level	I_{OCP}	V_{IN}=V_{EN}=5V, V_{OUT}=V_{REF}	360	600	-	mA
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}	V_{IN}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	-	160	-	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	V_{IN}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	-	30	-	°C

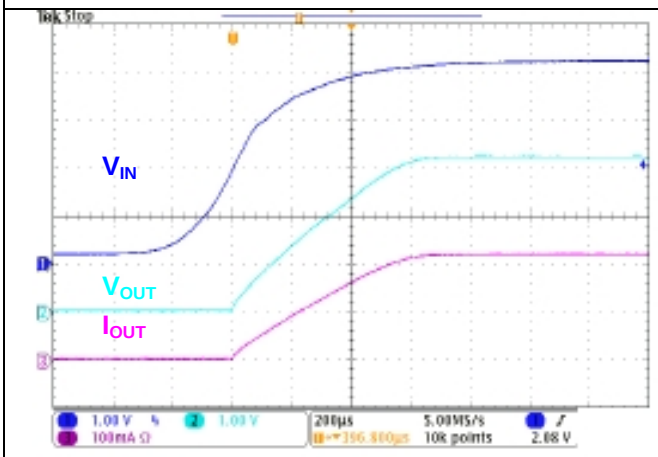
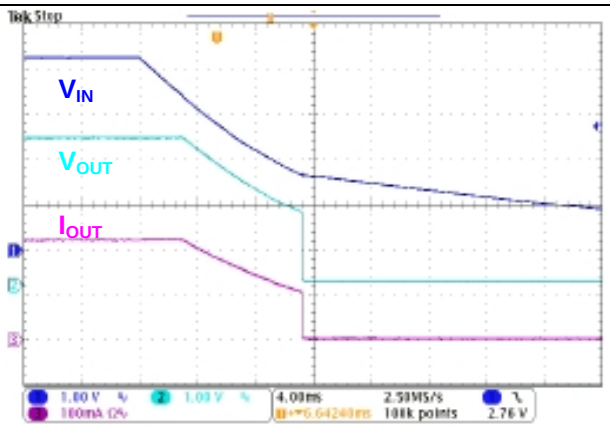
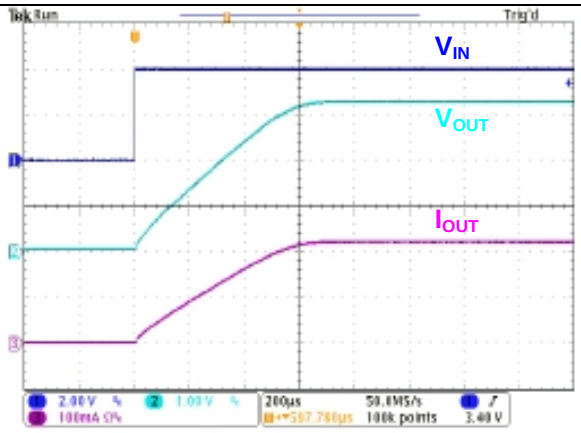
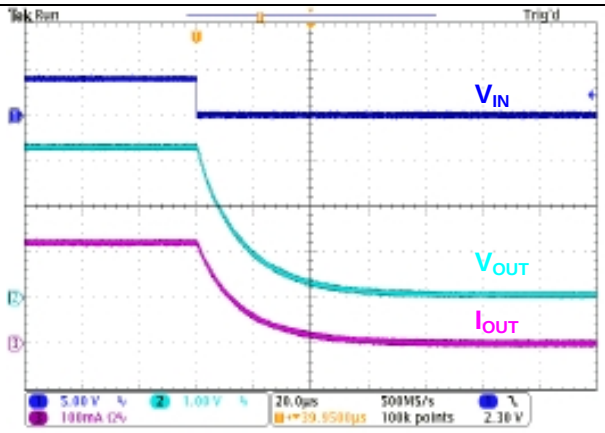
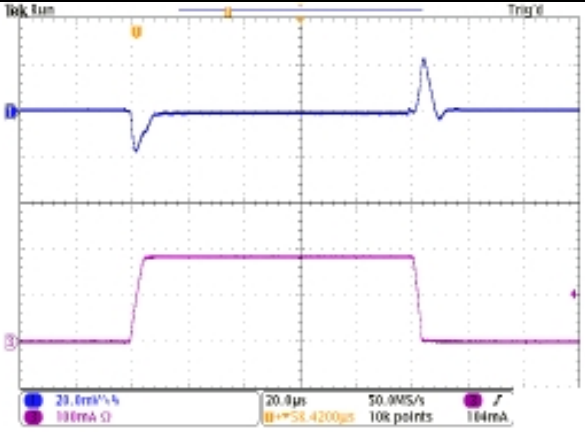
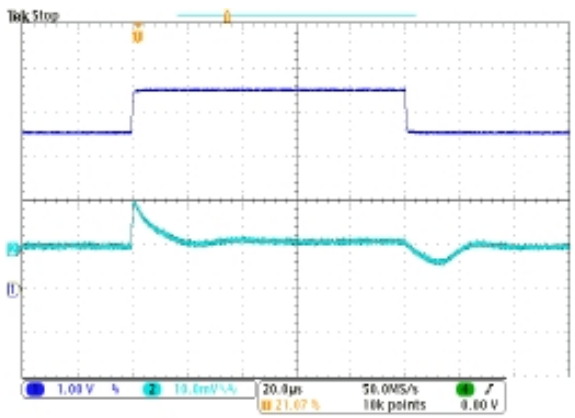
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A=25°C on a low effective thermal conductivity test board (single layout, 1S) of JEDEC 51-3 thermal measurement standard.

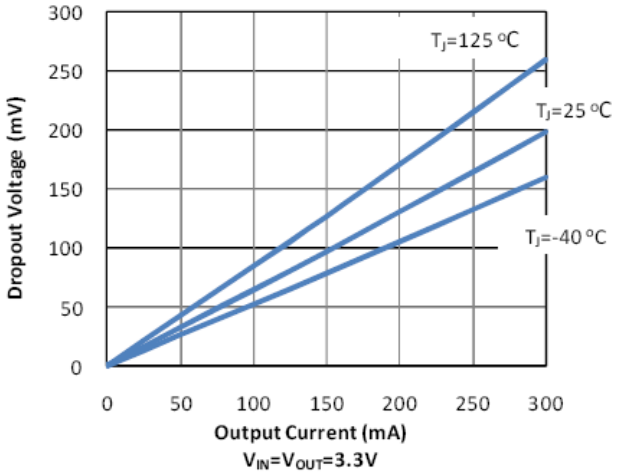
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

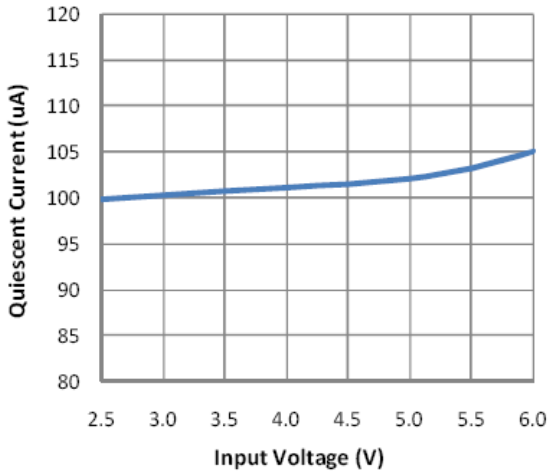
Typical Operating Characteristics

Power On from V_{IN}	Power Off from V_{IN}
	
V_{OUT}=3.3V，C_{IN}=C_{OUT}=1μF，R_{OUT}=15Ω	V_{OUT}=3.3V，C_{IN}=C_{OUT}=1μF，R_{OUT}=15Ω
Turn On from EN	**Turn Off from EN**
	
V_{OUT}=3.3V，C_{IN}=C_{OUT}=1μF，R_{OUT}=15Ω	V_{OUT}=3.3V，C_{IN}=C_{OUT}=1μF，R_{OUT}=15Ω
Load Transient Response	**Line Transient Response**
	
V_{OUT}=3.3V，C_{IN}=C_{OUT}=1μF	V_{OUT}=2.5V，C_{IN}=C_{OUT}=1μF，V_{IN}=3.5V to 4.5V

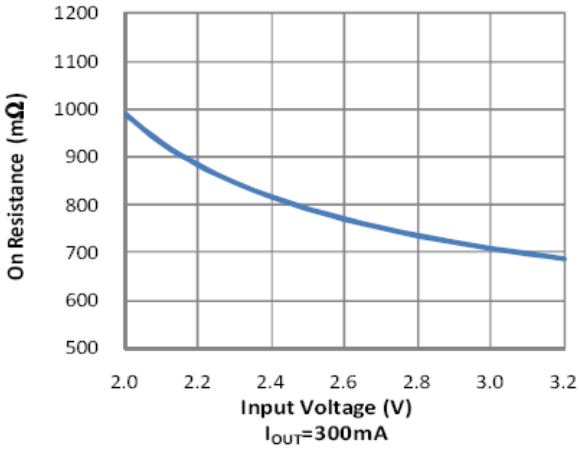
Dropout Voltage v.s. Output Current



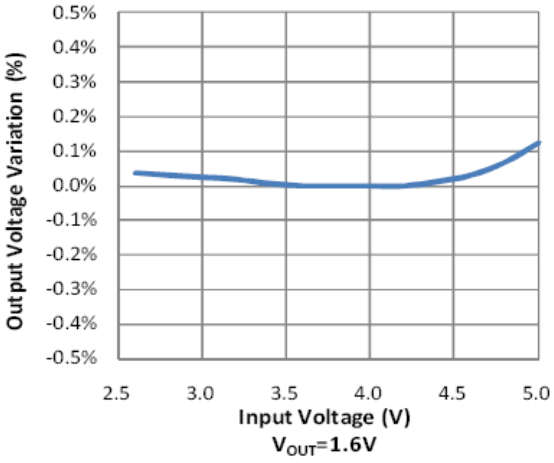
Quiescent Current v.s. Input Voltage



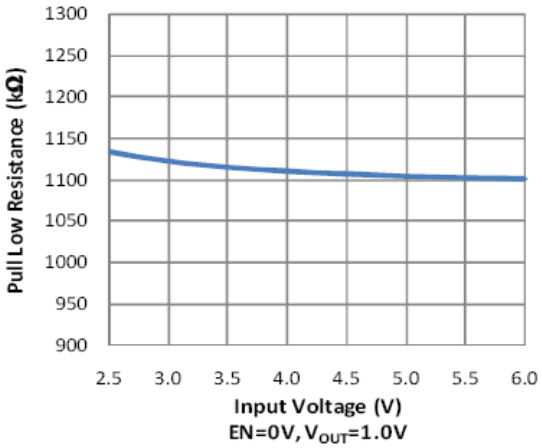
On Resistance v.s. Input Voltage



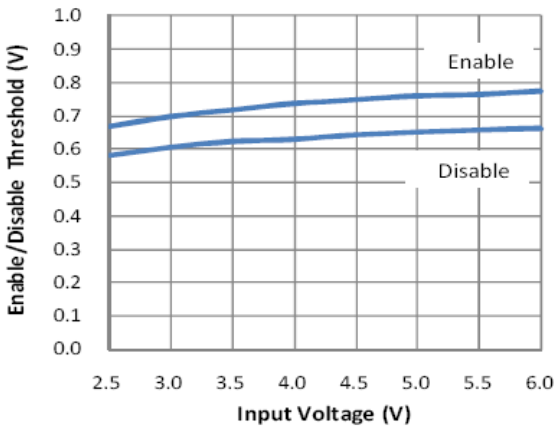
Output Voltage Line Regulation



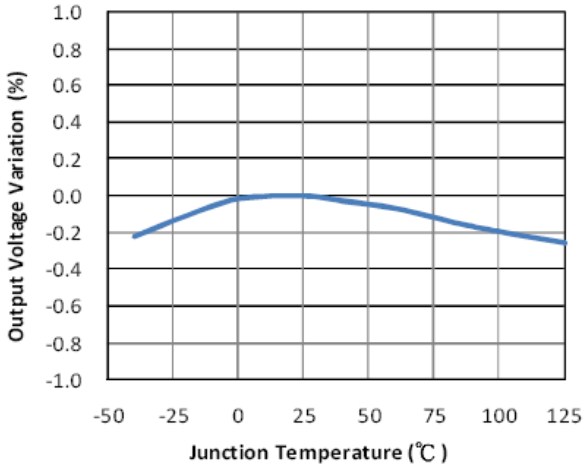
Pull Low Resistance v.s. Input Voltage



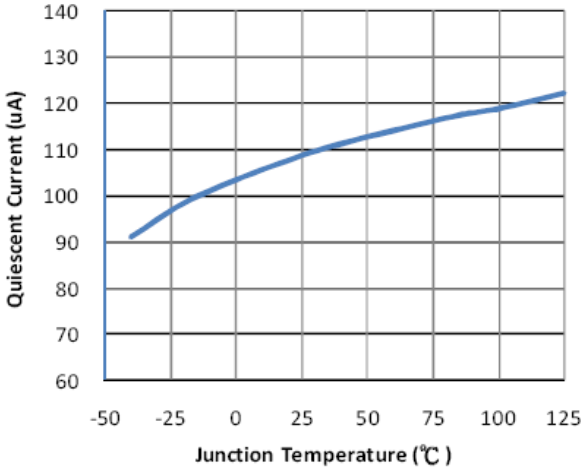
Enable/Disable v.s. Inptut Voltage



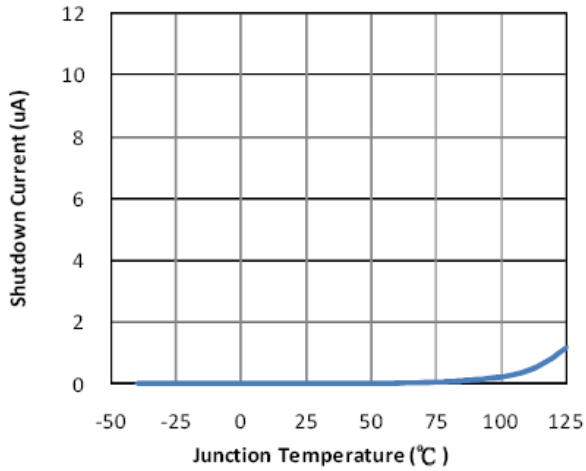
Output Voltage v.s. Temperature



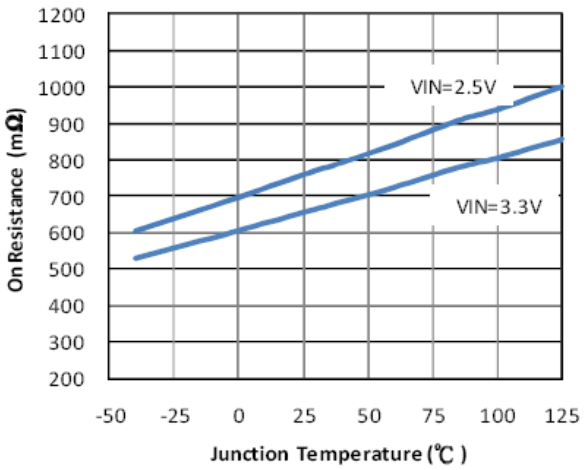
Quiescent Current v.s. Temperature



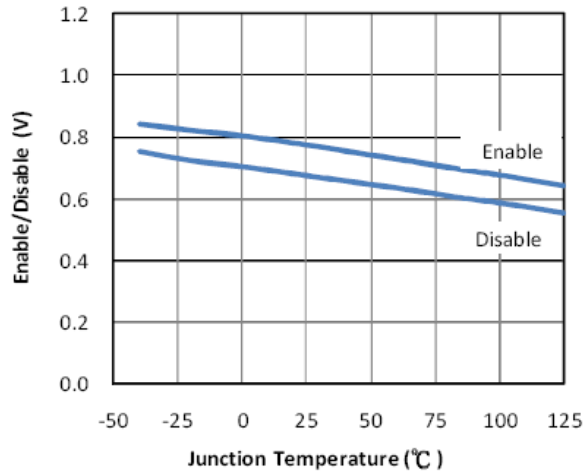
Shutdown Current v.s. Temperature



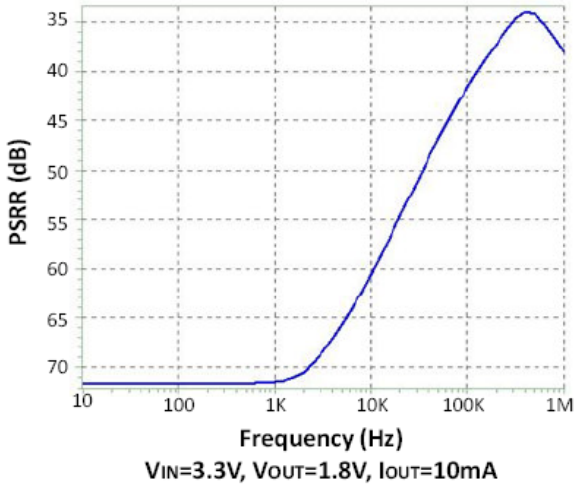
On Resistance v.s. Temperature



Enable/Disable v.s. Temperature



PSRR



VIN=3.3V, VOUT=1.8V, IOUT=10mA

Functional Description

Enable Function

LM1101 is enabled if the voltage of the EN pin is greater than 1.4V. If the voltage of the EN pin is less than 0.4V, the IC will be disabled.

POR – Power ON Reset

To let LM1101 start to operation, input voltage must be higher than its POR voltage even when EN voltage is pulled higher than enable high voltage. Typical POR voltage is 2.0V.

VOUT Voltage Adjustment

The V_{OUT} voltage of LM1101 can be adjusted by external voltage divider. Refer to typical application circuit, V_{OUT} voltage is calculated by the following equation:

$$V_{OUT} = (1+\frac{R_1}{R_2})\times 0.8V$$

Over Current Limit Function

LM1101 features over current limiting function which can limit its output current to 600mA.

Input and Output Capacitor Selection

For V_{IN} pin, 1μF or larger ceramic capacitor is required to provide bypass path in transient current demand. V_{OUT} pin is also recommended to have 1μF or larger ceramic capacitor to be stable and reduce the V_{OUT} voltage dip when fast loading transient is happened.

Power Dissipation

The max power depends on some conditions, including of thermal impedance, PCB layout, airflow, and so on. The max power dissipation can be calculated by the formula as below:

$$P_{D(max)}=(T_{J(max)}-T_A) / \theta_{JA}$$

$T_{J(max)}$ is the max junction temperature; θ_{JA} is the thermal impedance from junction to ambient. The thermal impedance θ_{JA} of SOT23-5 is package design and PCB design dependent.

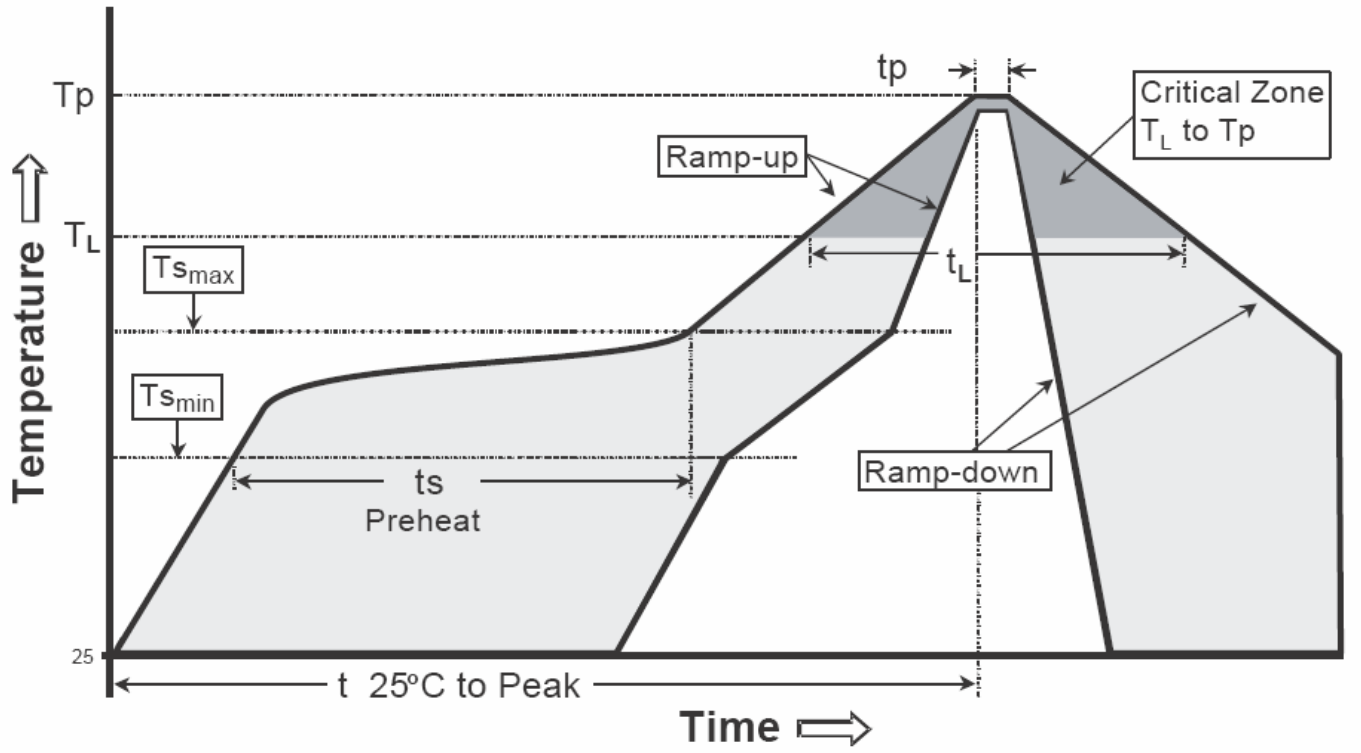
For recommended specification of LM1101, the max junction temperature is 125 degree C. The θ_{JA} of SOT23-5 is 250°C/W on the standard JEDEC 51-3 thermal test board. The max power dissipation (at 25°C ambient) can be calculated as below:

$P_{D\ (max\ at\ 25°C)}$=(125°C – 25°C) / (250°C/W) = 0.4W

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

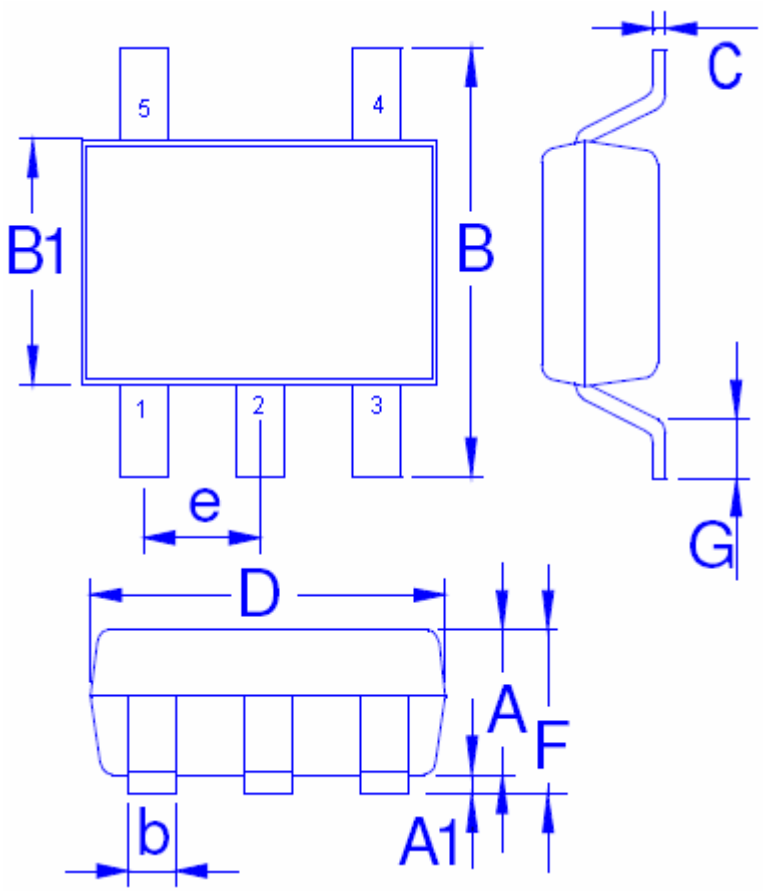
Recommended temperature profile for IR reflow

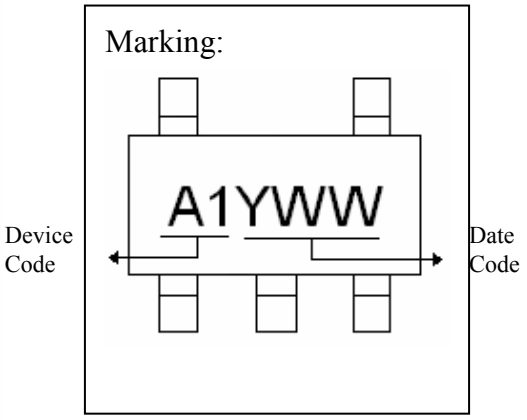


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-25 Dimension





Style:
Pin 1: Enable
Pin 2: Ground
Pin 3: V_{IN}
Pin 4: V_{OUT}
Pin 5: Feedback

5-Lead SOT-23-5L Plastic Surface Mounted Package
CYStek Package Code:N5

*:Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.30	0.0354	0.0512	c	0.08	0.22	0.0031	0.0087
A1	0.00	0.15	0.0000	0.0059	D	2.90*		0.1142*	
B	2.80*		0.1102*		E	0.95*		0.0374*	
B1	1.60*		0.0630*		F	-	1.45	-	0.0571
b	0.30	0.50	0.0118	0.0199	G	0.30	0.60	0.0118	0.0236

Notes : 1.Controlling dimension : millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead :Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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