TC1411/TC1411N

1A High-Speed MOSFET Drivers

Features

- Latch-Up Protected: Will Withstand 500 mA Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected: 4 kV
- High Peak Output Current: 1A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 16V
- High Capacitive Load Drive Capability:
  - 1000 pF in 25 nsec
- Short Delay Time: 30 nsec Typ.
- Matched Delay Times
- Low Supply Current
  - With Logic '1' Input: 500 µA
  - With Logic '0' Input: 100 µA
- Low Output Impedance: 8Ω
- Available in Space-Saving 8-pin MSOP Package
- Pinout Same as TC1410/TC1412/TC1413

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Relay Driver

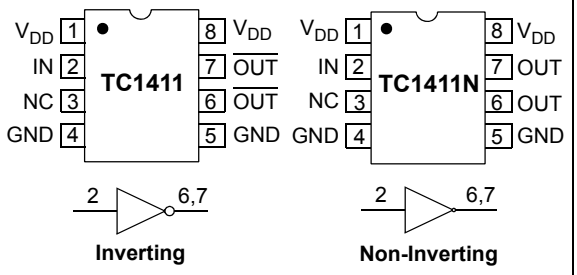
Description

The TC1411/TC1411N are 1A CMOS buffers/drivers. They will not latch-up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the TC1411/TC1411N can easily charge a 1000 pF gate capacitance in 25 nsec with matched rise and fall times, and provide low enough impedance in both the ON and the OFF states to ensure the MOSFET's intended state will not be affected, even by large transients. The leading and trailing edge propagation delay times are also matched to allow driving short-duration inputs with greater accuracy.

Package Types

8-Pin MSOP/PDIP/SOIC

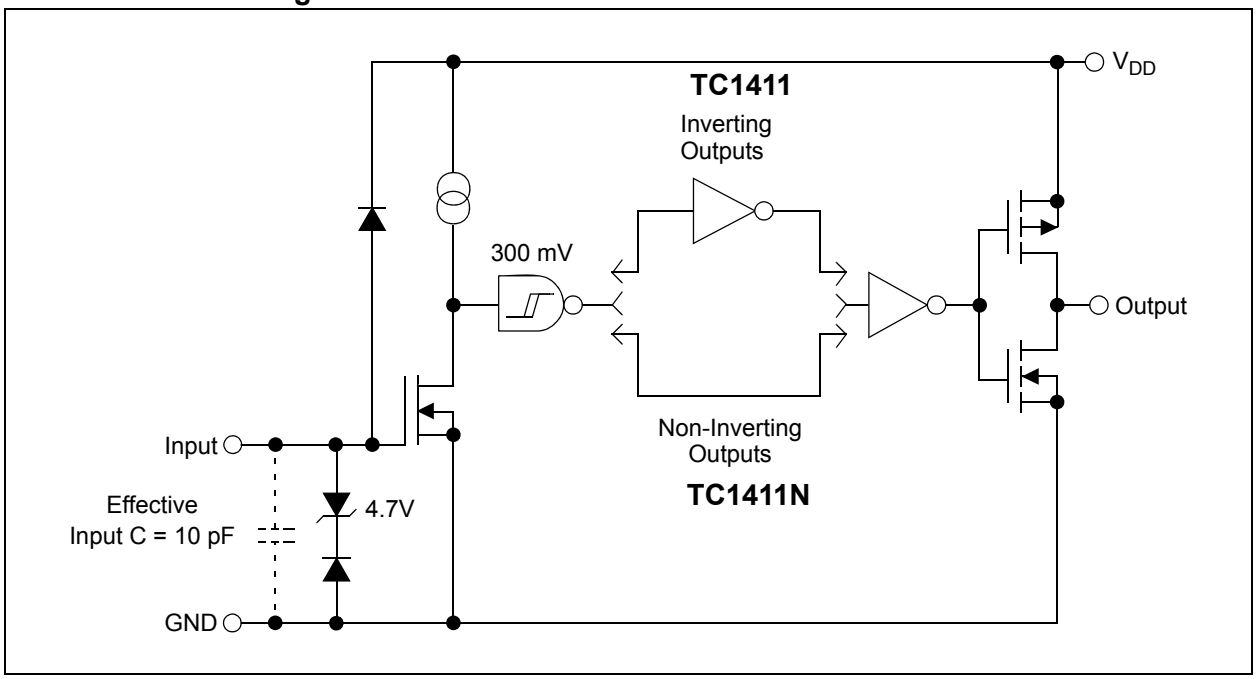


NC = No Internal Connection

Note: Duplicate pins must be connected together for proper operation.

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Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... +20V
Input Voltage ..... V_{DD} + 0.3V to GND – 5.0V
Power Dissipation ($T_A \leq 70°C$)
MSOP ..... 340 mW
PDIP ..... 730 mW
SOIC ..... 470 mW
Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature ..... +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 16V. Typical values are measured at T_A = +25°C, V_{DD} = 16V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.0	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1.0	—	1.0	µA	$0V \leq V_{IN} \leq V_{DD}$, T_A = +25°C
		-10	—	10		-40°C $\leq T_A \leq$ +85°C
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance	R_O	—	8	11	Ω	V_{DD} = 16V, I_O = 10 mA, T_A = +25°C
		—	10	14		0°C $\leq T_A \leq$ +70°C
		—	10	14		-40°C $\leq T_A \leq$ +85°C
Peak Output Current	I_{PK}	—	1.0	—	A	V_{DD} = 16V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	0.5	—	A	Duty cycle $\leq$ 2%, t $\leq$ 300 µs, V_{DD} = 16V
Switching Time (Note 1)						
Rise Time	t_R	—	25	35	ns	T_A = +25°C
		—	27	40		0°C $\leq T_A \leq$ +70°C
		—	29	40		-40°C $\leq T_A \leq$ +85°C, **Figure 4-1**
Fall Time	t_F	—	25	35	ns	T_A = +25°C
		—	27	40		0°C $\leq T_A \leq$ +70°C
		—	29	40		-40°C $\leq T_A \leq$ +85°C, **Figure 4-1**
Delay Time	t_{D1}	—	30	40	ns	T_A = +25°C,
		—	33	45		0°C $\leq T_A \leq$ +70°C
		—	35	45		-40°C $\leq T_A \leq$ +85°C, **Figure 4-1**
Delay Time	t_{D2}	—	30	40	ns	T_A = +25°C
		—	33	45		0°C $\leq T_A \leq$ +70°C
		—	35	45		-40°C $\leq T_A \leq$ +85°C, **Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	0.5	1.0	mA	V_{IN} = 3V, V_{DD} = 16V
		—	0.1	0.15		V_{IN} = 0V

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V $\leq V_{DD} \leq$ 16V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	ºC	
Specified Temperature Range (E)	T_A	-40	—	+85	ºC	
Specified Temperature Range (V)	T_A	-40	—	+125	ºC	
Maximum Junction Temperature	T_J	—	—	+150	ºC	
Storage Temperature Range	T_A	-65	—	+150	ºC	
Package Thermal Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	ºC/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	ºC/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	155	—	ºC/W	

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 16V.

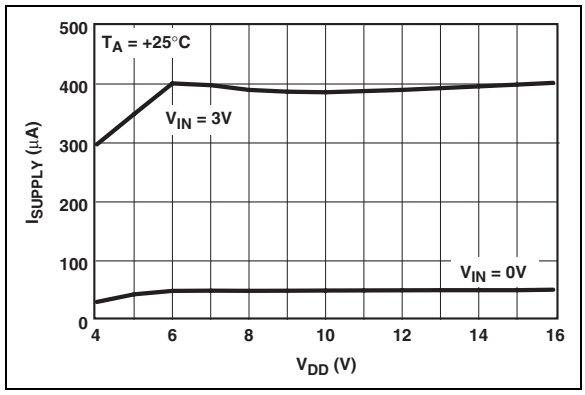


FIGURE 2-1: *Quiescent Supply Current vs. Supply Voltage.*

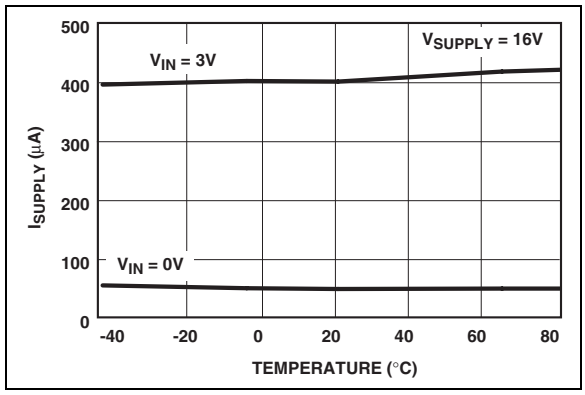


FIGURE 2-4: *Quiescent Supply Current vs. Temperature.*

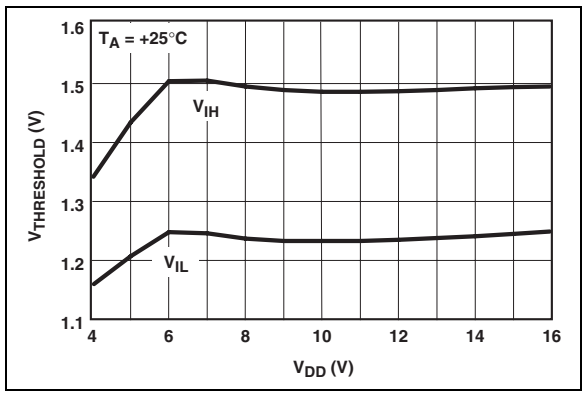


FIGURE 2-2: *Input Threshold vs. Supply Voltage.*

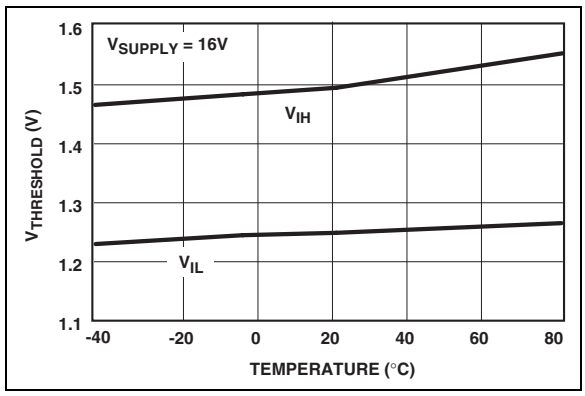


FIGURE 2-5: *Input Threshold vs. Temperature.*

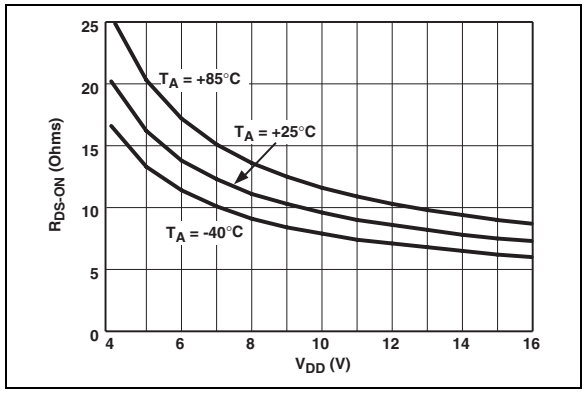


FIGURE 2-3: *High-State Output Resistance vs. Supply Voltage.*

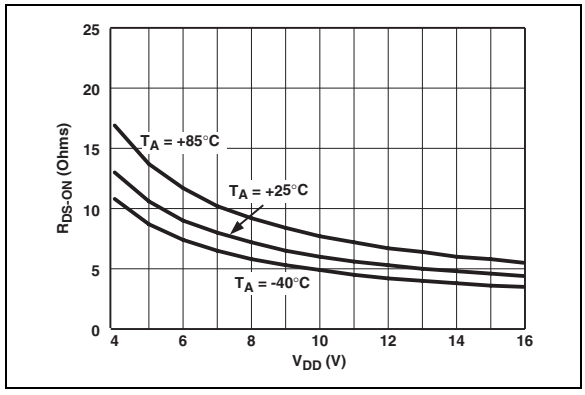


FIGURE 2-6: *Low-State Output Resistance vs. Supply Voltage.*

Note: Unless otherwise indicated, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 16V.

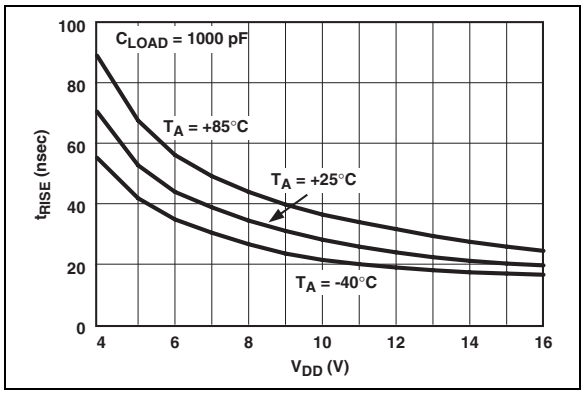


FIGURE 2-7: *Rise Time vs. Supply Voltage.*

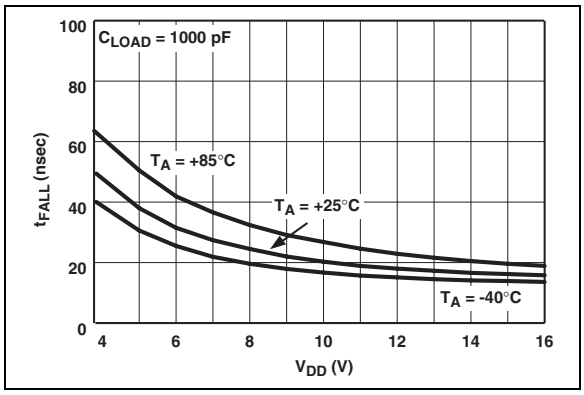


FIGURE 2-10: *Fall Time vs. Supply Voltage.*

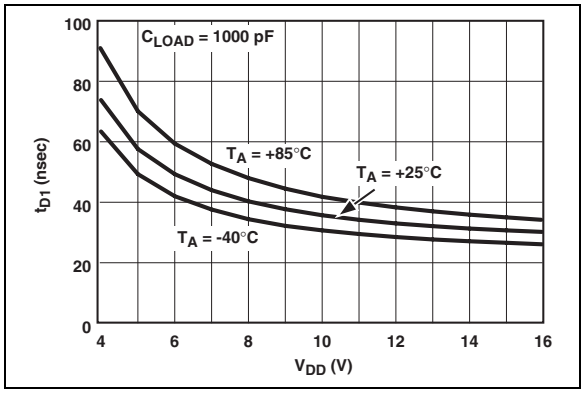


FIGURE 2-8: *Propagation Delay vs. Supply Voltage.*

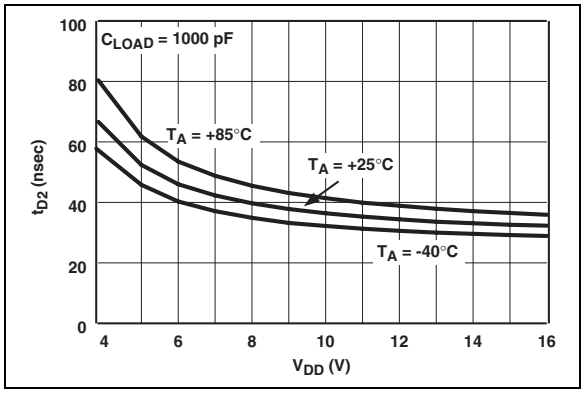


FIGURE 2-11: *Propagation Delay vs. Supply Voltage.*

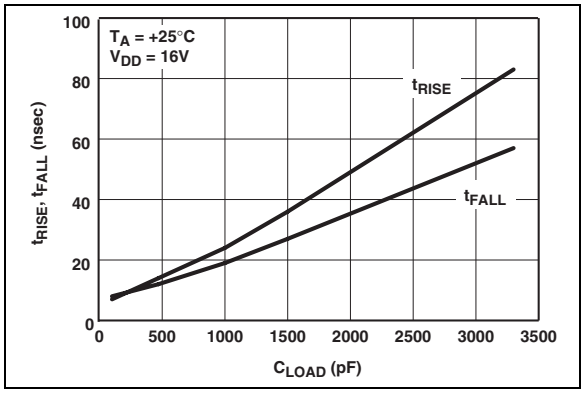


FIGURE 2-9: *Rise and Fall Times vs. Capacitive Load.*

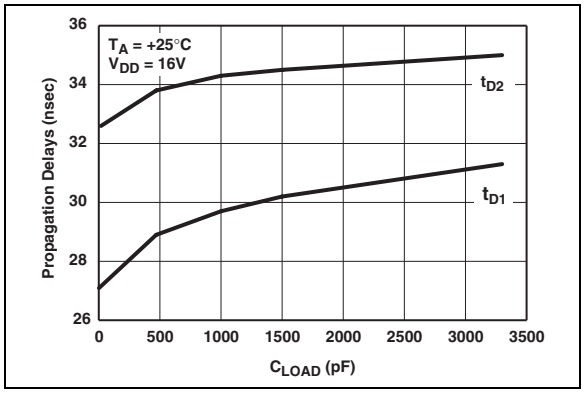


FIGURE 2-12: *Propagation Delays vs. Capacitive Load.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Symbol	Description
1	V_{DD}	Supply input, 4.5V to 16V
2	INPUT	Control input
3	NC	No connection
4	GND	Ground
5	GND	Ground
6	OUTPUT	CMOS push-pull output, common to pin 7
7	OUTPUT	CMOS push-pull output, common to pin 6
8	V_{DD}	Supply input, 4.5V to 16V

3.1 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 16V with respect to the ground pin. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A value of 1.0 µF is suggested.

3.2 Control Input (INPUT)

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input has 300 mV of hysteresis between the high and low thresholds that prevents output glitching even when the rise and fall time of the input signal is very slow.

3.3 CMOS Push-pull Output (OUTPUT)

The MOSFET driver output is a low impedance, CMOS push-pull style output, capable of driving a capacitive load with 1A peak currents.

3.4 Ground (GND)

The ground pins are the return path for the bias current and for the high peak currents which discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

3.5 No Connect (NC)

No internal connection.

4.0 APPLICATION INFORMATION

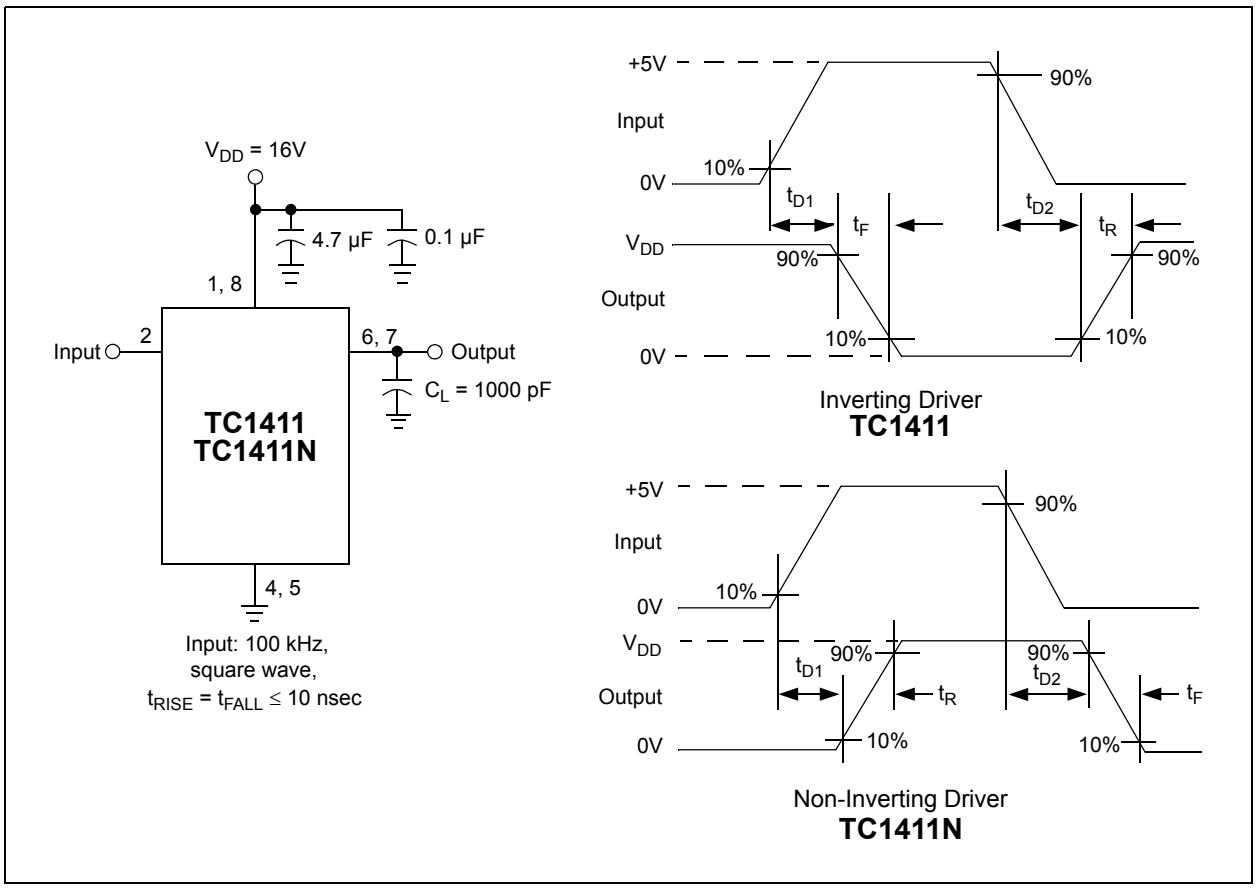


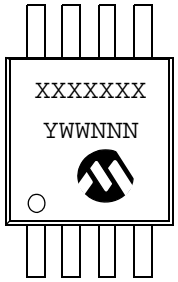
FIGURE 4-1: *Switching Time Test Circuit.*

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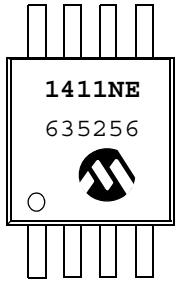
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

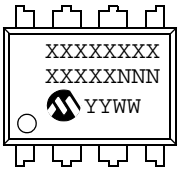
8-Lead MSOP



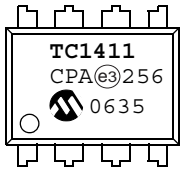
Example:



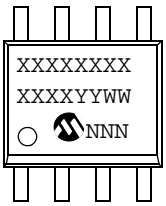
8-Lead PDIP (300 mil)



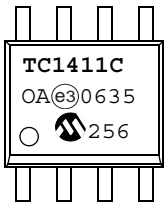
Example:



8-Lead SOIC (150 mil)



Example:

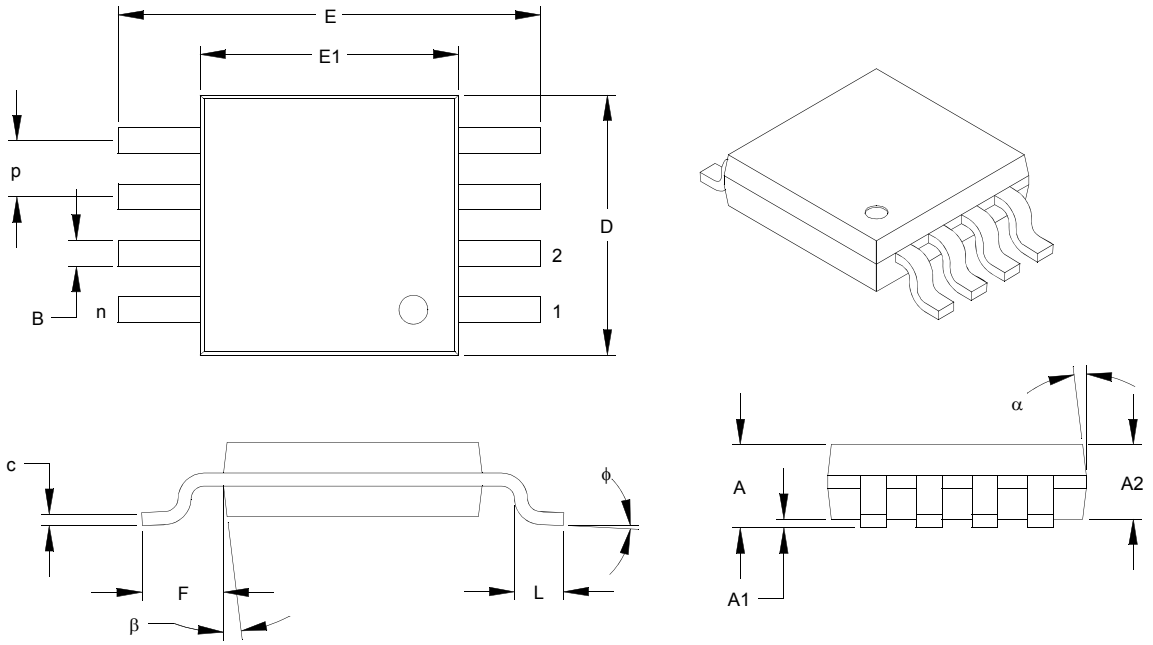


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (UA) (MSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 BSC			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

***** Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

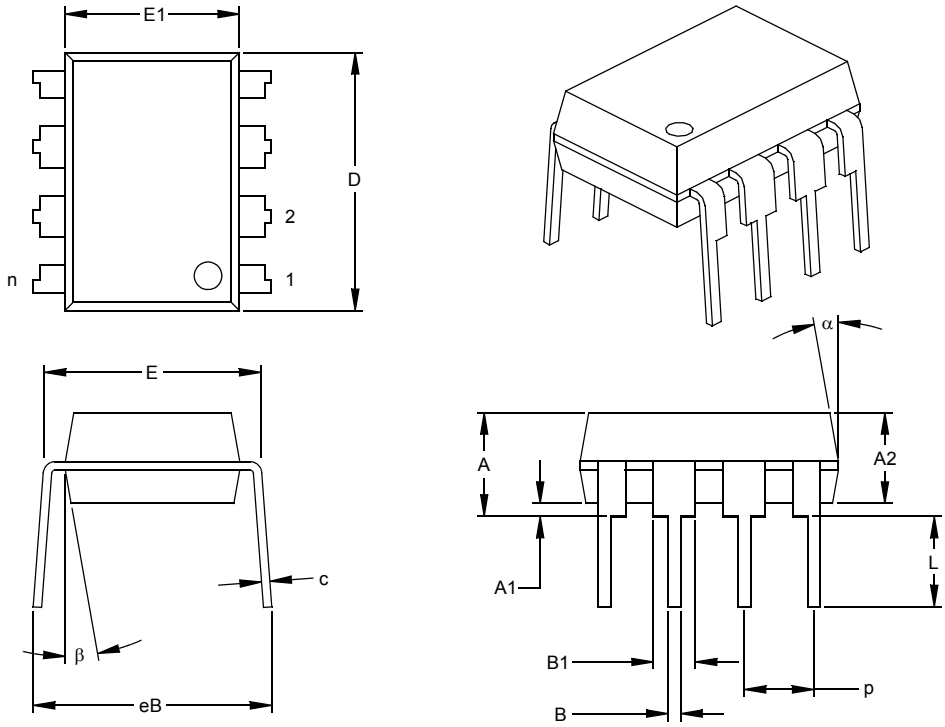
JEDEC Equivalent: MO-187 Revised 07-21-05

Drawing No. C04-111

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8-Lead Plastic Dual In-line (PA) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

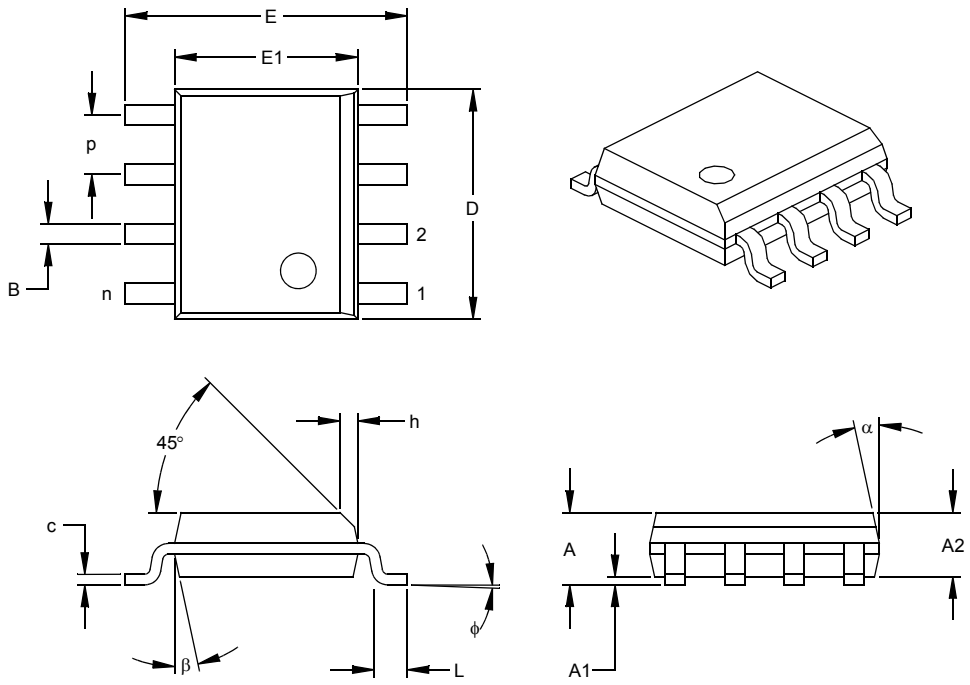


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

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APPENDIX A: REVISION HISTORY

Revision D (September 2006)

- Added -40°C to +125°C temperature range to Temperature Characteristics table and Product Information System page.
- Added disclaimer to package outline drawings.

Revision C (March 2003)

- Added 8-Lead MSOP Package.

Revision B (May 2002)

- Converted TELCOM data sheet for Embedded Control Handbook

Revision A (March 2001)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	TC1411:	1 A Single MOSFET Driver, Inverting
	TC1411N:	1 A Single MOSFET Driver, Non-Inverting
Temperature Range:	C =	0°C to +70°C
	E =	-40°C to +85°C
	V =	-40°C to +125°C
Package:	OA =	Plastic SOIC, (150 mil Body), 8-lead
	OA713 =	Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel)
	UA =	Plastic Micro Small Outline (MSOP), 8-lead *
	UA713 =	Plastic Micro Small Outline (MSOP), 8-lead * (Tape and Reel)
	PA =	Plastic DIP (300 mil Body), 8-lead

* MSOP package is only available in E-Temp.

Examples:

a)	TC1411COA:	1A Single MOSFET driver, 8LD SOIC pkg, 0°C to +70°C.
b)	TC1411CPA:	1A Single MOSFET driver, 8LD PDIP package, 0°C to +70°C.
c)	TC1411EUA713:	Tape and Reel, 1A Single MOSFET driver, 8LD MSOP package, -40°C to +85°C.
d)	TC1411VOA713:	Tape and Reel, 1A Single MOSFET driver, 8LD SOIC pkg, -40°C to +125°C.
a)	TC1411NCPA:	1A Single MOSFET driver, 8LD PDIP package, 0°C to +70°C.
b)	TC1411NEPA:	1A Single MOSFET driver, 8LD PDIP package, -40°C to +85°C.
c)	TC1411NEUA:	1A Single MOSFET driver, 8LD MSOP package, -40°C to +85°C.
d)	TC1411NVPA:	1A Single MOSFET driver, 8LD PDIP package, -40°C to +125°C

NOTES:

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08/29/06

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