MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Document order number: MC33972
Rev 3.0, 12/2004

Advance Information

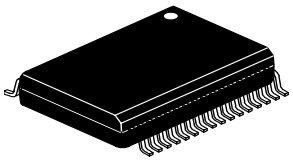
33972

Multiple Switch Detection Interface with Suppressed Wake-Up

MULTIPLE SWITCH DETECTION INTERFACE WITH SUPPRESSED WAKE-UP

The 33972 Multiple Switch Detection Interface with Suppressed Wake-Up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The analog input signal is buffered and provided on the AMUX output terminal for the MCU to read.

The 33972 device has two modes of operation, Normal and Sleep. Normal mode allows programming of the device and supplies switch contacts with pullup or pulldown current as it monitors switch change of state. The Sleep mode provides low quiescent current, which makes the 33972 ideal for automotive and industrial products requiring low sleep state currents.



DWB SUFFIX
EW (Pb-FREE) SUFFIX
CASE 1324-02
32-TERMINAL SOICW

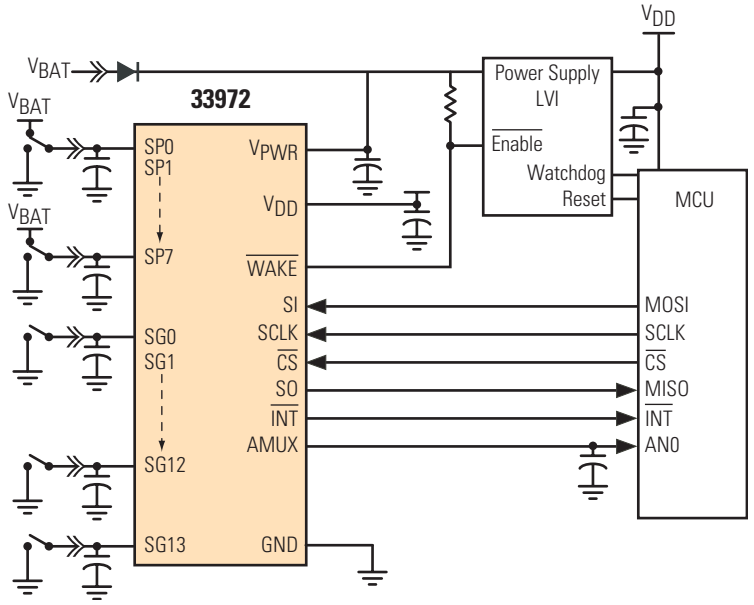
Features

- Designed to Operate 5.5 V ≤ V_{PWR} ≤ 26 V
- Switch Input Voltage Range -14 V to V_{PWR}, 40 V Max
- Interfaces Directly to Microprocessor Using 3.3 V/5.0 V SPI Protocol
- Selectable Wake-Up on Change of State
- Selectable Wetting Current (16 mA or 2.0 mA)
- 8 Programmable Inputs (Switches to Battery or Ground)
- 14 Switch-to-Ground Inputs
- V_{PWR} Standby Current 100 μA Typical, V_{DD} Standby Current 20 μA Typical
- Active Interrupt ($\overline{INT}$) on Change-of-Switch State
- Pb-Free Packaging Designated by Suffix Code EW

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33972DWB/R2	-40°C to 125°C	32 SOICW
MC33972EW/R2		

33972 Simplified Application Diagram



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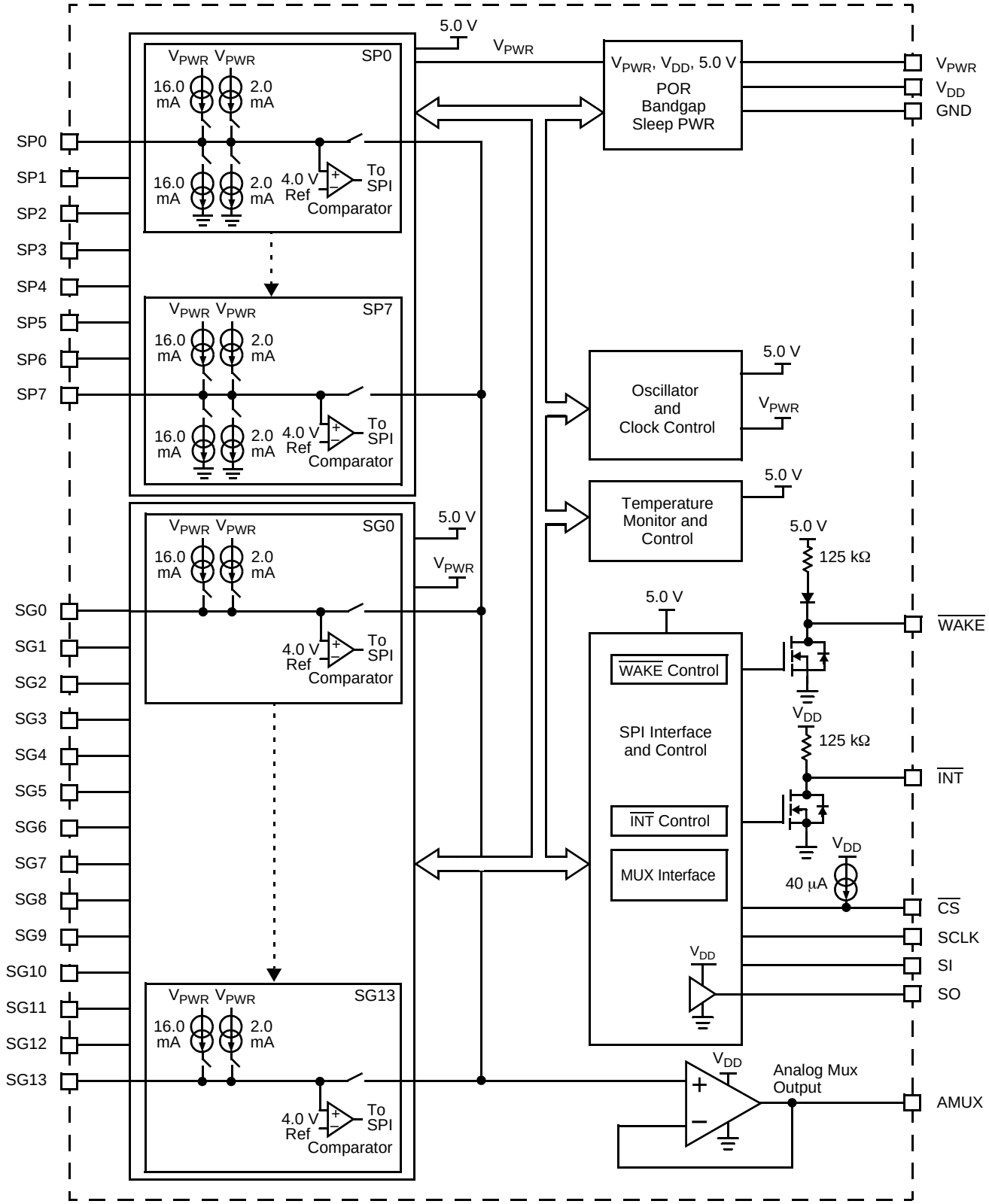

Figure 1. 33972 Simplified Internal Block Diagram

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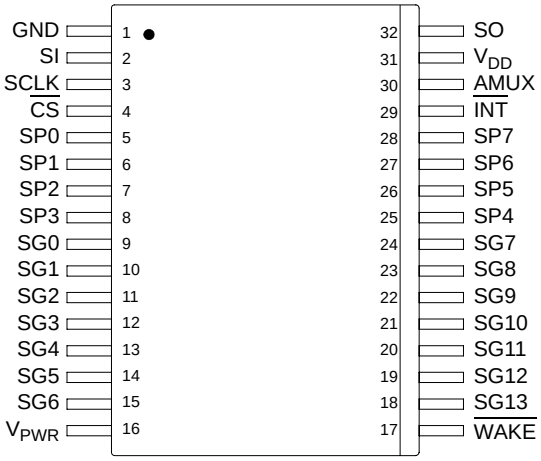

TERMINAL DEFINITIONS

A functional description of each terminal can be found in the System/Application Information section beginning on page 9.

Terminal	Terminal Name	Formal Name	Definition
1	GND	Ground	Ground for logic, analog, and switch to battery inputs.
2	SI	SPI Slave In	SPI control data input terminal from MCU to 33972.
3	SCLK	Serial Clock	SPI control clock input terminal.
4	$\overline{CS}$	Chip Select	SPI control chip select input terminal from MCU to 33972. Logic [0} allows data to be transferred in.
5–8 25–28	SP0–3 SP4–7	Programmable Switches 0–7	Programmable switch-to-battery or switch-to-ground input terminals.
9–15, 18–24	SG0–6, SG13–7	Switch-to-Ground Inputs 0–13	Switch-to-ground input terminals.
16	V_{PWR}	Battery Input	Battery supply input terminal. Terminal requires external reverse battery protection.
17	$\overline{WAKE}$	Wake-Up	Open drain wake-up output. Designed to control a power supply enable terminal.
29	$\overline{INT}$	Interrupt	Open-drain output to MCU. Used to indicate input switch change of state.
30	AMUX	Analog Multiplex Output	Analog multiplex output.
31	V_{DD}	Voltage Drain Supply	3.3/5.0 V supply. Sets SPI communication level for SO driver.
32	SO	SPI Slave Out	Provides digital data from 33972 to MCU.

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MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
V_{DD} Supply Voltage	–	-0.3 to 7.0	V_{DC}
$\overline{CS}$, SI, SO, SCLK, $\overline{INT}$, AMUX (Note 1)	–	-0.3 to 7.0	V_{DC}
$\overline{WAKE}$ (Note 1)	–	-0.3 to 40	V_{DC}
V_{PWR} Supply Voltage (Note 1)	–	-0.3 to 50	V_{DC}
Switch Input Voltage Range	–	-14 to 40	V_{DC}
Frequency of SPI Operation (V_{DD} = 5.0 V)	–	6.0	MHz
ESD Voltage (Note 2) Human Body Model (Note 3), (Note 4) Machine Model (Note 5)	 V_{ESD1} V_{ESD2}	 ±4000 ±200	V
THERMAL RATINGS			
Operating Temperature Ambient Junction Case	 T_A T_J T_C	 -40 to 125 -40 to 150 -40 to 125	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Power Dissipation (T_A = 25°C) (Note 6)	P_D	1.7	W
Thermal Resistance Junction to Ambient Junction to Lead	 $R_{\theta JA}$ $R_{\theta JL}$	 74 25	°C/W
Peak Package Reflow Temperature During Solder Mounting (Note 7) DWB Suffix EW Suffix	T_{SOLDER}	 240 245	°C

Notes

1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. ESD data available upon request.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
4. All terminals when tested individually.
5. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
6. Maximum power dissipation at T_J = 150°C junction temperature with no heat sink used.
7. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

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STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage					V
Supply Voltage Range Quasi-Functional (Note 8)	$V_{PWR(QF)}$	5.5	–	8.0	
Fully Operational	$V_{PWR(FO)}$	8.0	–	26	
Supply Voltage Range Quasi-Functional (Note 8)	$V_{PWR(QF)}$	26	–	40	
Supply Current All Switches Open, Normal Mode, Tri-State Disabled	$I_{PWR(ON)}$	–	2.0	4.0	mA
Sleep State Supply Current Scan Timer = 64 ms, Switches Open	$I_{PWR(SS)}$	40	70	100	μA
Logic Supply Voltage	V_{DD}	3.1	–	5.25	V
Logic Supply Current All Switches Open, Normal Mode	I_{DD}	–	0.25	0.5	mA
Sleep State Logic Supply Current Scan Timer = 64 ms, Switches Open	$I_{DD(SS)}$	–	10	20	μA
SWITCH INPUT					
Pulse Wetting Current Switch-to-Battery (Current Sink)	I_{PULSE}	12	15	18	mA
Pulse Wetting Current Switch-to-Ground (Current Source)	I_{PULSE}	12	16	18	mA
Sustain Current Switch-to-Battery Input (Current Sink)	$I_{SUSTAIN}$	1.8	2.0	2.2	mA
Sustain Current Switch-to-Ground Input (Current Source)	$I_{SUSTAIN}$	1.8	2.0	2.2	mA
Sustain Current Matching Between Channels on Switch-to-Ground Inputs $\frac{I_{SUS(MAX)} - I_{SUS(MIN)}}{I_{SUS(MIN)}}$ X 100	I_{MATCH}	–	2.0	4.0	%
Input Offset Current When Selected as Analog	I_{OFFSET}	-2.0	1.4	2.0	μA
Input Offset Voltage When Selected as Analog $V_{(SP\&SGinputs)}$ to AMUX Output	V_{OFFSET}	-10	2.5	10	mV
Analog Operational Amplifier Output Voltage Sink 250 μA	V_{OL}	–	10	30	mV
Analog Operational Amplifier Output Voltage Source 250 μA	V_{OH}	V_{DD} - 0.1	–	–	V
Switch Detection Threshold	V_{TH}	3.70	4.0	4.3	V
Switch Input Voltage Range	V_{IN}	-14	–	40	V
Temperature Monitor (Note 9), (Note 10)	T_{LIM}	155	–	185	°C
Temperature Monitor Hysteresis (Note 10)	$T_{LIM(HYS)}$	5.0	10	15	°C

Notes

8. Device operational. Table parameters may be out of specification.
9. Thermal shutdown of 16 mA pullup and pulldown current sources only. 2.0 mA current source/sink and all other functions remain active.
10. This parameter is guaranteed by design but is not production tested.

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STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions of 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic Voltage Thresholds (Note 11)	$V_{INLOGIC}$	0.8	–	2.2	V
SCLK, SI, Tri-State SO Input Current 0 V to V_{DD}	I_{SCLK}, I_{SI}, $I_{SO(TRI)}$	-10	–	10	μA
$\overline{CS}$ Input Current $\overline{CS}$ = V_{DD}	$I_{\overline{CS}}$	-10	–	10	μA
$\overline{CS}$ Pullup Current $\overline{CS}$ = 0 V	$I_{\overline{CS}}$	30	–	100	μA
SO High-State Output Voltage $I_{SO(HIGH)}$ = -200 μA	$V_{SO(HIGH)}$	V_{DD} - 0.8	–	V_{DD}	V
SO Low-State Output Voltage $I_{SO(HIGH)}$ = 1.6 mA	$V_{SO(LOW)}$	–	–	0.4	V
Input Capacitance on SCLK, SI, Tri-State SO (Note 12)	C_{IN}	–	–	20	pF
$\overline{INT}$ Internal Pullup Current	–	15	40	100	μA
$\overline{INT}$ Voltage $\overline{INT}$ = Open Circuit	$V_{\overline{INT}(HIGH)}$	V_{DD} - 0.5	–	V_{DD}	V
$\overline{INT}$ Voltage $I_{\overline{INT}}$ = 1.0 mA	$V_{\overline{INT}(LOW)}$	–	0.2	0.4	V
$\overline{WAKE}$ Internal Pullup Current	$I_{\overline{WAKE}(PU)}$	20	40	100	μA
$\overline{WAKE}$ Voltage $\overline{WAKE}$ = Open Circuit	$V_{\overline{WAKE}(HIGH)}$	4.0	4.3	5.3	V
$\overline{WAKE}$ Voltage $I_{\overline{WAKE}}$ = 1.0 mA	$V_{\overline{WAKE}(LOW)}$	–	0.2	0.4	V
$\overline{WAKE}$ Voltage Maximum Voltage Applied to $\overline{WAKE}$ Through External Pullup	$V_{\overline{WAKE}(MAX)}$	–	–	40	V

Notes

11. Upper and lower logic threshold voltage levels apply to SI, $\overline{CS}$, and SCLK.
12. This parameter is guaranteed by design but is not production tested.

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DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCH INPUT					
Pulse Wetting Current Time	$t_{PULSE(ON)}$	15	16	20	ms
Interrupt Delay Time Normal Mode	$t_{INT-DLY}$	– –	5.0 –	16 –	µs
Sleep Mode Switch Scan Time	t_{SCAN}	100	200	300	µs
Calibrated Scan Timer Accuracy Sleep Mode	$t_{SCAN\ TIMER}$	– –	– –	10 –	%
Calibrated Interrupt Timer Accuracy Sleep Mode	$t_{INT\ TIMER}$	– –	– –	10 –	%
DIGITAL INTERFACE TIMING (Note 13)					
Required Low-State Duration on V_{PWR} for Reset (Note 14) V_{PWR} ≤ 0.2 V	t_{RESET}	– –	– –	10 –	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK Required Setup Time	t_{LEAD}	100 –	– –	– –	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ Required Setup Time	t_{LAG}	50 –	– –	– –	ns
SI to Falling Edge of SCLK Required Setup Time	$t_{SI(SU)}$	16 –	– –	– –	ns
Falling Edge of SCLK to SI Required Hold Time	$t_{SI(HOLD)}$	20 –	– –	– –	ns
SI, $\overline{CS}$, SCLK Signal Rise Time (Note 15)	$t_{R(SI)}$	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time (Note 15)	$t_{F(SI)}$	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (Note 16)	$t_{SO(EN)}$	–	–	55	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (Note 17)	$t_{SO(DIS)}$	–	–	55	ns
Time from Rising Edge of SCLK to SO Data Valid (Note 18)	t_{VALID}	–	25	55	ns

Notes

13. These parameters are guaranteed by design. Production test equipment uses 4.16 MHz, 5.0 V SPI interface.
14. This parameter is guaranteed by design but not production tested.
15. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
16. Time required for valid output status data to be available on SO terminal.
17. Time required for output states data to be terminated at SO terminal.
18. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

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Timing Diagrams

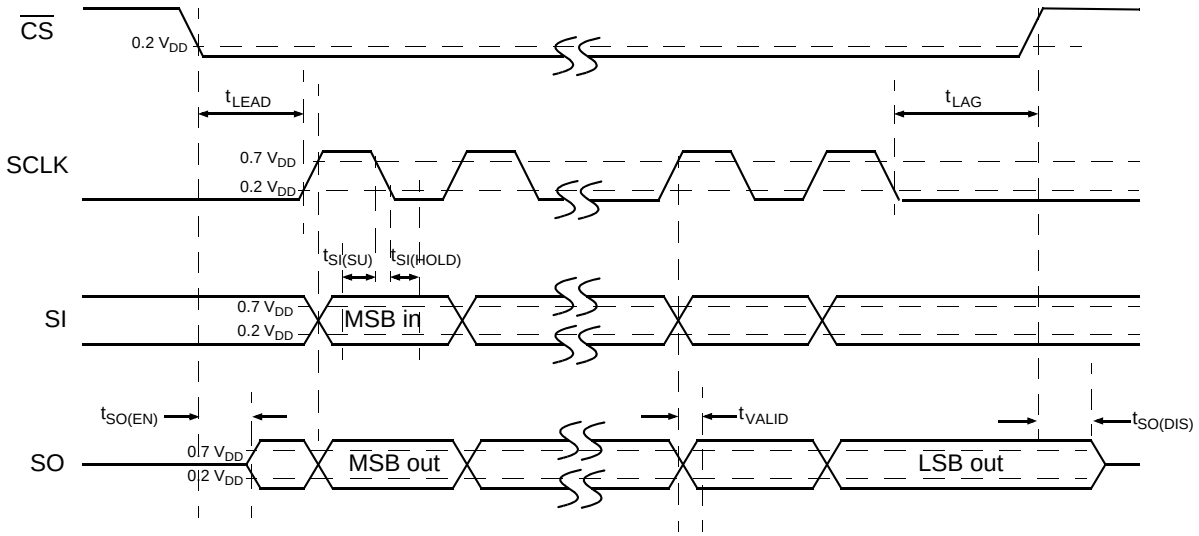

Figure 2. SPI Timing Characteristics

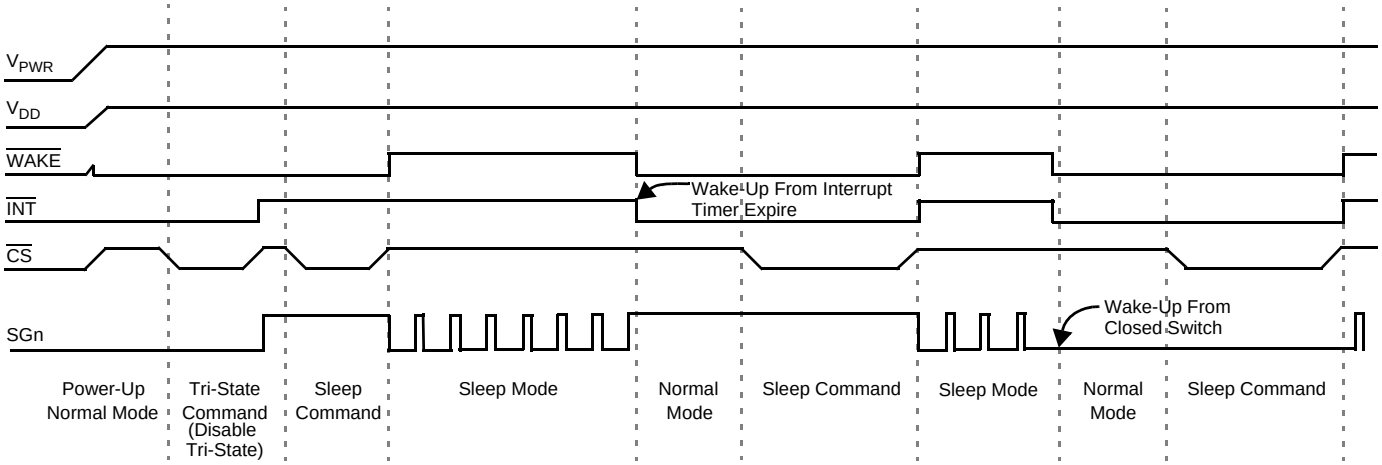

Figure 3. Sleep Mode to Normal Mode Operation

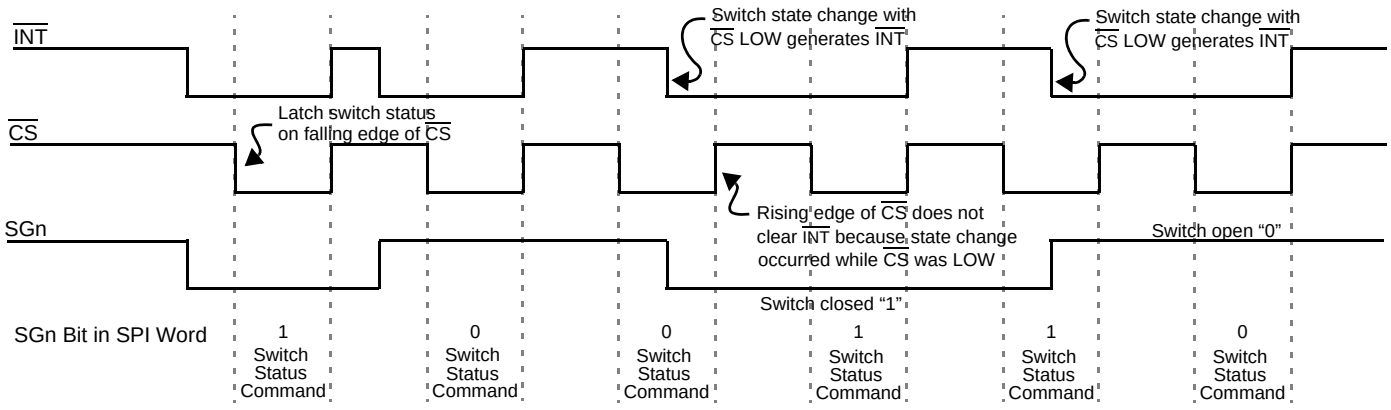

Figure 4. Normal Mode Interrupt Operation

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SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33972 device is an integrated circuit designed to provide systems with ultra-low quiescent sleep/wake-up modes and a robust interface between switch contacts and a microprocessor. The 33972 replaces many of the discrete components required when interfacing to microprocessor-based systems while providing switch ground offset protection, contact wetting current, and system wake-up.

The 33972 features 8-programmable switch-to-ground or switch-to-battery inputs and 14 switch-to-ground inputs. All switch inputs may be read as analog inputs through the analog multiplexer (AMUX). Other features include a programmable wake-up timer, programmable interrupt timer, programmable wake-up/interrupt bits, and programmable wetting current settings.

This device is designed primarily for automotive applications but may be used in a variety of other applications such as computer, telecommunications, and industrial controls.

FUNCTIONAL TERMINAL DESCRIPTION

$\overline{CS}$

The system MCU selects the 33972 to receive communication using the chip select ($\overline{CS}$) terminal. With the $\overline{CS}$ in a logic LOW state, command words may be sent to the 33972 via the serial input (SI) terminal, and switch status information can be received by the MCU via the serial output (SO) terminal. The falling edge of $\overline{CS}$ enables the SO output, latches the state of the $\overline{INT}$ terminal, and the state of the external switch inputs.

Rising edge of the $\overline{CS}$ initiates the following operation:

1. Disables the SO driver (high impedance)
2. $\overline{INT}$ terminal is reset to logic [1], except when additional switch changes occur during $\overline{CS}$ LOW. (See Figure 4 on page 8.)
3. Activates the received command word, allowing the 33972 to act upon new data from switch inputs.

To avoid any spurious data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic LOW state. Internal to the 33972 device is an active pullup to V_{DD} on $\overline{CS}$.

In Sleep mode the negative edge of $\overline{CS}$ (V_{DD} applied) will wake up the 33972 device. Data received from the device during $\overline{CS}$ wake-up may not be accurate.

SCLK

The system clock (SCLK) terminal clocks the internal shift register of the 33972. The SI data is latched into the input shift register on the falling edge of SCLK signal. The SO terminal shifts the switch status bits out on the rising edge of SCLK. The SO data is available for the MCU to read on the falling edge of SCLK. False clocking of the shift register must be avoided to ensure validity of data. It is essential the SCLK terminal be in a logic LOW state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended, though not necessary, that the SCLK terminal is commanded to a logic LOW state as long as the device is not accessed and $\overline{CS}$ is in a logic HIGH state. When the $\overline{CS}$ is in a logic HIGH state, any signal on the SCLK and SI terminals will be ignored and the SO terminal is tri-state.

SI

The SI terminal is used for serial instruction data input. SI information is latched into the input register on the falling edge of SCLK. A logic HIGH state present on SI will program a *one* in the command word on the rising edge of the $\overline{CS}$ signal. To program a complete word, 24 bits of information must be entered into the device.

SO

The SO terminal is the output from the shift register. The SO terminal remains tri-stated until the $\overline{CS}$ terminal transitions to a logic LOW state. All *open switches* are reported as *zero*, all *closed switches* are reported as *one*. The negative transition of $\overline{CS}$ enables the SO driver.

The first positive transition of SCLK will make the status data bit 24 available on the SO terminal. Each successive positive clock will make the next status data bit available for the MCU to read on the falling edge of SCLK. The SI/SO shifting of the data follows a first-in, first-out protocol, with both input and output words transferring the most significant bit (MSB) first.

$\overline{INT}$

The $\overline{INT}$ terminal is an interrupt output from the 33972 device. The $\overline{INT}$ terminal is an open-drain output with an internal pullup to V_{DD}. In Normal mode, a switch state change will trigger the $\overline{INT}$ terminal (when enabled). The $\overline{INT}$ terminal and INT bit in the SPI register are latched on the falling edge of $\overline{CS}$. This permits the MCU to determine the origin of the interrupt. When two 33972 devices are used, only the device initiating the interrupt will have the INT bit set. The $\overline{INT}$ terminal is cleared on the rising edge of $\overline{CS}$. The $\overline{INT}$ terminal will not clear with rising edge of $\overline{CS}$ if a switch contact change has occurred while $\overline{CS}$ was LOW.

In a multiple 33972 device system with $\overline{WAKE}$ HIGH and V_{DD} on (Sleep mode), the falling edge of $\overline{INT}$ will place all 33972s in Normal mode.

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$\overline{\text{WAKE}}$

The $\overline{\text{WAKE}}$ terminal is an open-drain output and a wake-up input. The terminal is designed to control a power supply Enable terminal. In the Normal mode, the $\overline{\text{WAKE}}$ terminal is LOW. In the Sleep mode, the $\overline{\text{WAKE}}$ terminal is HIGH. The $\overline{\text{WAKE}}$ terminal has a pullup to the internal +5.0 V supply.

In Sleep mode with the $\overline{\text{WAKE}}$ terminal HIGH, falling edge of $\overline{\text{WAKE}}$ will place the 33972 in Normal mode. In Sleep mode with V_{DD} applied, the $\overline{\text{INT}}$ terminal must be HIGH for negative edge of $\overline{\text{WAKE}}$ to wake up the device. If V_{DD} is not applied to the device in Sleep mode, $\overline{\text{INT}}$ does not affect $\overline{\text{WAKE}}$ operation.

V_{PWR}

The V_{PWR} terminal is battery input and Power-ON Reset to the 33972 IC. The V_{PWR} terminal requires external reverse battery and transient protection. Maximum input voltage on V_{PWR} is 50 V. All wetting, sustain, and internal logic current is provided from the V_{PWR} terminal.

V_{DD}

The V_{DD} input terminal is used to determine logic levels on the microprocessor interface (SPI) terminals. Current from V_{DD} is used to drive SO output and the pullup current for $\overline{\text{CS}}$ and $\overline{\text{INT}}$ terminals. V_{DD} must be applied for wake-up from negative edge of $\overline{\text{CS}}$ or $\overline{\text{INT}}$.

GND

The GND terminal provides ground for the IC as well as ground for inputs programmed as switch-to-battery inputs.

SP0:SP7

The 33972 device has 8 switch inputs capable of being programmed to read switch-to-ground or switch-to-battery contacts. The input is compared with a 4.0 V reference. When programmed to be switch-to-battery, voltages greater than 4.0 V are considered closed. Voltages less than 4.0 V are considered open. The opposite holds true when inputs are programmed as switch-to-ground. Programming features are defined in Table 1 through Table 6 in the Device Operation section of this datasheet beginning on page 12. Voltages greater than the V_{PWR} supply voltage will source current through the SP inputs to the V_{PWR} terminal. Transient battery voltages greater than 40 V must be clamped by an external device.

SG0:SG13

The SGn terminals are switch-to-ground inputs only. The input is compared with a 4.0 V reference. Voltages greater than 4.0 V are considered open. Voltages less than 4.0 V are considered closed. Programming features are defined in Table 1 through Table 6 in the Device Operation section of this datasheet beginning on page 12. Voltages greater than the V_{PWR} supply voltage will source current through the SG inputs to the V_{PWR} terminal. Transient battery voltages greater than 40 V must be clamped by an external device.

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MCU INTERFACE DESCRIPTION

The 33972 device directly interfaces to a 3.3 V or 5.0 V microcontroller unit (MCU). SPI serial clock frequencies up to 6.0 MHz may be used for programming and reading switch input status (production tested at 4.16 MHz). Figure 5 illustrates the configuration between an MCU and one 33972.

Serial peripheral interface (SPI) data is sent to the 33972 device through the SI input terminal. As data is being clocked into the SI terminal, status information is being clocked out of the device by the SO output terminal. The response to a SPI command will always return the switch status, interrupt flag, and thermal flag. Input switch states are latched into the SO register on the falling edge of the chip select ($\overline{CS}$) terminal. Twenty-four bits are required to complete a transfer of information between the 33972 and the MCU.

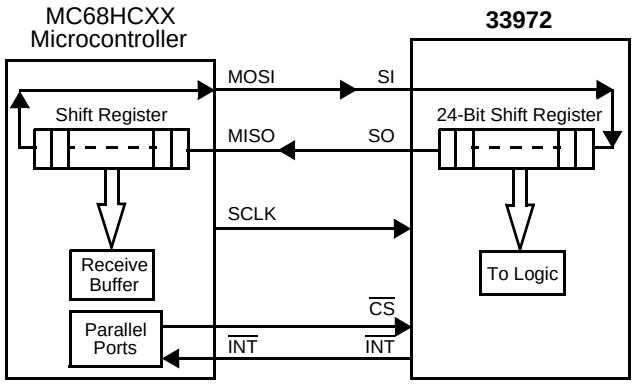

Figure 5. SPI Interface with Microprocessor

Two or more 33972 devices may be used in a module system. Multiple ICs may be SPI-configured in parallel or serial. Figures 6 and 7 show the configurations. When using the serial configuration, 48-clock cycles are required to transfer data in/out of the ICs.

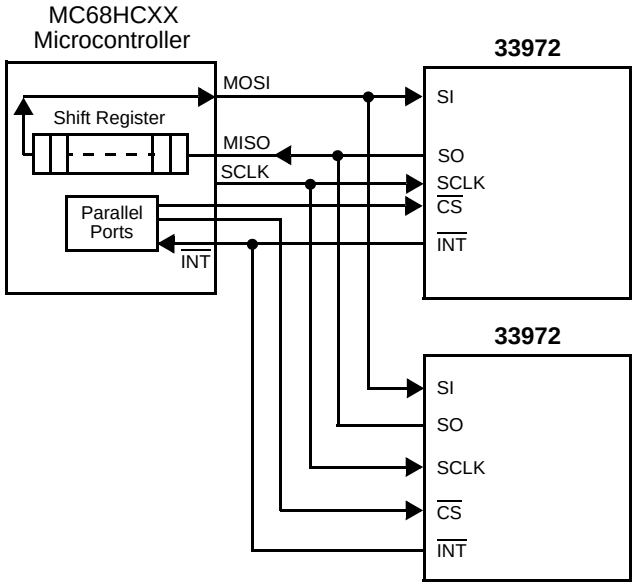

Figure 6. SPI Parallel Interface with Microprocessor

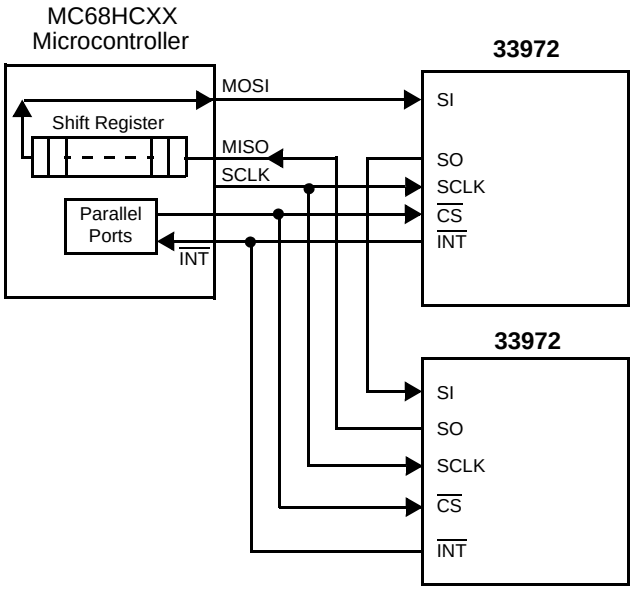

Figure 7. SPI Serial Interface with Microprocessor

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DEVICE OPERATION

Power Supply

The 33972 is designed to operate from 5.5 V to 40 V on the V_{PWR} terminal. Characteristics are provided from 8.0 V to 16 V for the device. Switch contact currents and the internal logic supply are generated from the V_{PWR} terminal. The V_{DD} supply terminal is used to set the SPI communication voltage levels, current source for the SO driver, and pullup current on $\overline{INT}$ and $\overline{CS}$.

V_{DD} supply may be removed from the device to reduce quiescent current. If V_{DD} is removed while the device is in Normal mode, the device will remain in Normal mode. If V_{DD} is removed in Sleep mode, the device will remain in Sleep mode until wake-up input is received ($\overline{WAKE}$ HIGH to LOW, switch input or interrupt timer expires).

Removing V_{DD} from the device disables SPI communication and will not allow the device to wake up from $\overline{INT}$ and $\overline{CS}$ terminals.

Power-ON Reset (POR)

Applying V_{PWR} to the device will cause a Power-ON Reset and place the device in Normal mode.

Default settings from Power-ON Reset via V_{PWR} or Reset Command are as follows:

- Programmable Switch – Set to Switch to Battery
- All Inputs Set as Wake-Up
- Wetting Current On (16 mA)
- Wetting Current Timer On (20 ms)
- All Inputs Tri-State
- Analog Select 00000 (No Input Channel Selected)

Modes of Operation

The 33972 has two operating modes, Normal mode and Sleep mode. A discussion on Normal mode begins below. A discussion on Sleep mode begins on page 18.

Normal Mode

Normal mode may be entered by the following events:

- Application of V_{PWR} to the IC
- Change-of-Switch State (when enabled)
- Falling Edge of $\overline{WAKE}$
- Falling Edge of $\overline{INT}$ (with V_{DD} = 5.0 V and $\overline{WAKE}$ at Logic [1])
- Falling Edge of $\overline{CS}$ (with V_{DD} = 5.0 V)
- Interrupt Timer Expires

Only in Normal mode with V_{DD} applied can the registers of the 33972 be programmed through the SPI.

The registers that may be programmed in Normal mode are listed below. Further explanation of each register is provided in subsequent paragraphs.

- Programmable Switch Register (*Settings Command*)
- Wake-Up/Interrupt Register (*Wake-Up/Interrupt Command*)
- Wetting Current Register (*Metallic Command*)
- Wetting Current Timer Register (*Wetting Current Timer Enable Command*)
- Tri-State Register (*Tri-State Command*)
- Analog Select Register (*Analog Command*)
- Calibration of Timers (*Calibration Command*)
- Reset (*Reset Command*)

Figure 4, page 8, is a graphical description of the device operation in Normal mode. Switch states are latched into the input register on the falling edge of $\overline{CS}$. The $\overline{INT}$ to the MCU is cleared on the rising edge of $\overline{CS}$. However, $\overline{INT}$ will not clear on rising edge of $\overline{CS}$ if a switch has closed during SPI communication ($\overline{CS}$ LOW). This prevents switch states from being missed by the MCU.

Programmable Switch Register

Inputs SP0 to SP7 may be programmable for switch-to-battery or switch-to-ground. These inputs types are defined using the *settings command* (Table 1). To set an SPn input for switch-to-battery, a logic [1] for the appropriate bit must be set. To set an SPn input for switch-to-ground, a logic [0] for the appropriate bit must be set. The MCU may change or update the Programmable Switch Register via software at any time in Normal mode. Regardless of the setting, when the SPn input switch is closed a logic [1] will be placed in the Serial Output Response Register (Table 12, page 17).

Table 1. Settings Command

Settings Command								Not used								Battery/Ground Select							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0

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Wake-Up/Interrupt Register

The Wake-Up/Interrupt Register defines the inputs that are allowed to wake the 33972 from Sleep mode or set the $\overline{INT}$ terminal LOW in Normal mode. Programming the wake-up/interrupt bit to logic [0] will disable the specific input from generating an interrupt and will disable the specific input from waking the IC in Sleep mode (Table 2). Programming the wake-up/interrupt bit to logic [1] will enable the specific input to generate an interrupt with switch change of state and will enable the specific input as wake-up. The MCU may change or update the Wake-Up/Interrupt Register via software at any time in Normal mode.

Table 2. Wake-Up/Interrupt Command

Wake-Up/Interrupt Command								Command Bits														
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	0	1	1	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

Wetting Current Register

The 33972 has two levels of switch contact current, 16 mA and 2.0 mA (see Figure 8). The *metallic command* is used to set the switch contact current level (Table 3). Programming the metallic bit to logic [0] will set the switch wetting current to 2.0 mA. Programming the metallic bit to logic [1] will set the switch contact wetting current to 16 mA. The MCU may change or update the Wetting Current Register via software at any time in Normal mode.

Wetting current is designed to provide higher levels of current during switch closure. The higher level of current is designed to keep switch contacts from building up oxides that form on the switch contact surface.

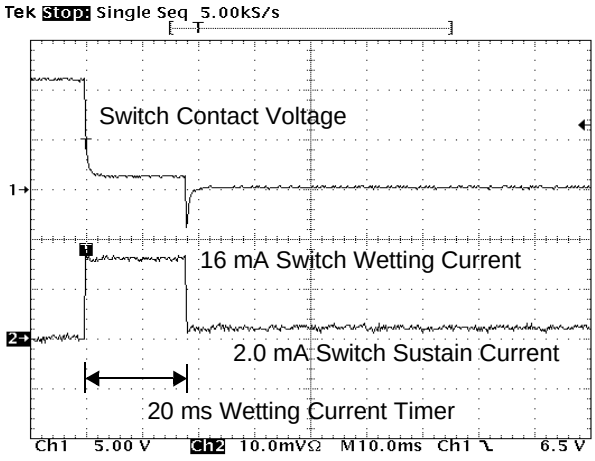

Figure 8. Contact Wetting and Sustain Current

Table 3. Metallic Command

Metallic Command								Command Bits														
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	1	0	1	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

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Wetting Current Timer Register

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparator threshold (4.0 V). When the 20 ms timer expires, the contact current is reduced from 16 mA to 2.0 mA. The wetting current timer may be disabled for a specific input. When the timer is disabled, 16 mA of current will continue to flow through the closed switch contact. With multiple wetting current timers disabled, power dissipation for the IC must be considered.

The MCU may change or update the Wetting Current Timer Register via software at any time in Normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the wetting current timer bit to logic [0] will disable the wetting current timer. Programming the wetting current timer bit to logic [1] will enable the wetting current timer (Table 4).

Table 4. Wetting Current Timer Enable Command

Wetting Current Timer Commands								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	0	0	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

Tri-State Register

The *tri-state command* is use to set the SPn or SGn input node as high impedance (Table 5). By setting the Tri-State Register bit to logic [1], the input will be high impedance regardless of the metallic command setting. The comparator on each input remains active. This command allows the use of each input as a comparator with a 4.0 V threshold. The MCU may change or update the Tri-State Register via software at any time in Normal mode.

Table 5. Tri-State Command

Tri-State Commands								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	1	0	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

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Analog Select Register

The analog voltage on switch inputs may be read by the MCU using the *analog command* (Table 6). Internal to the IC is a 22-to-1 analog multiplexer. The voltage present on the selected input terminal is buffered and made available on the AMUX output terminal. The AMUX output terminal is clamped to a maximum of V_{DD} volts regardless of the higher voltages present on the input terminal. After an input has been selected as the analog, the corresponding bit in the next SO data stream will be logic [0]. When selecting a channel to be read as analog, the user must also set the desired current (16 mA, 2.0 mA, or high impedance). Setting bit 6 and bit 5 to 0,0 selects the input as high impedance. Setting bit 6 and bit 5 to 0,1 selects 2.0 mA, and 1,0 selects 16 mA. Setting bit 6 and bit 5 to 1,1 in the Analog Select Register is not allowed and will place the input as an analog input with high impedance.

Analog currents set by the *analog command* are pullup currents for all SGn and SPn inputs (Table 6). The *analog command* does not allow pulldown currents on the SPn inputs. Setting the current to 16 mA or 2.0 mA may be useful for reading sensor inputs. Further information is provided in the Applications section of this datasheet beginning on page 20. The MCU may change or update the Analog Select Register via software at any time in Normal mode.

Table 6. Analog Command

Analog Command								Not used									Current Select		Analog Channel Select				
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	16 mA	2.0 mA	0	0	0	0	0

Table 7. Analog Channel

Bits 43210	Analog Channel Select
00000	No Input Selected
00001	SG0
00010	SG1
00011	SG2
00100	SG3
00101	SG4
00110	SG5
00111	SG6
01000	SG7
01001	SG8
01010	SG9
01011	SG10
01100	SG11
01101	SG12
01110	SG13
01111	SP0
10000	SP1
10001	SP2
10010	SP3
10011	SP4
10100	SP5
10101	SP6
10110	SP7

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Calibration of Timers

In cases where an accurate time base is required, the user may calibrate the internal timers using the *calibration command* (Table 8). After the 33972 device receives the calibration command, the device expects 512 μs logic [0] calibration pulse on the $\overline{CS}$ terminal. The pulse is used to calibrate the internal clock. No other SPI terminals should transition during this 512 μs calibration pulse. Because the oscillator frequency changes with temperature, calibration is required for an accurate time base. Calibrating the timers has no affect on the quiescent current measurement. The calibration command simply makes the time base more accurate. The *calibration command* may be used to update the device on a periodic basis.

Table 8. Calibration Command

Calibration Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Reset

The reset command resets all registers to Power-ON Reset (POR) state. Refer to Table 10, page 17, for POR states or the paragraph entitled Power-ON Reset (POR) on page 12 of this datasheet.

Table 9. Reset Command

Reset Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

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SPI Command Summary

Table 10 below provides a comprehensive list of SPI commands recognized by the 33972 and the reset state of each register. Table 11 and Table 12 contain the Serial Output (SO) data for input voltages greater or less than the threshold level. Open switches are always indicated with a logic [0], closed switches are indicated with logic [1].

Table 10. SPI Command Summary

	MSB Command Bits								Setting Bits																LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Switch Status Command	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Settings Command Bat=1, Gnd=0 (Default state = 1)	0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Wake-Up/Interrupt Bit Wake-Up=1 Non-Wake-Up=0 (Default state = 1)	0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	0	0	1	1	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Metallic Command Metallic = 1 Non-metallic = 0 (Default state = 1)	0	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	0	1	0	1	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Analog Command	0	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	16mA 0	2.0mA 0	0	0	0	0	0
Wetting Current Timer Enable Command Timer ON = 1 Timer OFF = 0 (Default state = 1)	0	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	1	0	0	0	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Tri-State Command Input Tri-State=1 Input Active = 0 (Default state = 1)	0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	1	0	1	0	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Calibration Command (Default state – uncalibrated)	0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Sleep Command (Refer to Sleep Mode on page 18.)	0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	int timer	int timer	int timer	scan timer	scan timer	scan timer
Reset Command	0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SO Response Will Always Send	them flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0

Table 11. Serial Output (SO) Bit Data

Type of Input	Input Programmed	Voltage on Input Terminal	SO SPI Bit
SP	Switch to Ground	SPn < 4.0 V	1
	Switch to Ground	SPn > 4.0 V	0
	Switch to Battery	SPn < 4.0 V	0
	Switch to Battery	SPn > 4.0 V	1
SG	N/A	SGn < 4.0 V	1
	N/A	SGn > 4.0 V	0

Table 12. Serial Output (SO) Response Register

SO Response Will Always Send	them flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0

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Example of Normal Mode Operation

The operation of the device in Normal Mode is defined by the states of the programmable internal control registers. A typical application may have the following settings:

- Programmable Switch – Set to Switch-to-Ground
- All Inputs Set as Wake-Up
- Wetting Current On (16 mA)
- Wetting Current Timer On (20 ms)
- All inputs Tri-State-Disabled (comparator is active)
- Analog select 00000 (no input channel selected)

With the device programmed as above, an interrupt will be generated with each switch contact change of state (open-to-close or close-to-open) and 16 mA of contact wetting current will be source for 20 ms. The $\overline{INT}$ terminal will remain LOW until switch status is acknowledged by the microprocessor. It is critical to understand $\overline{INT}$ will not be cleared on the rising edge of $\overline{CS}$ if a switch closure occurs while $\overline{CS}$ is LOW. The maximum duration a switch state change can exist without acknowledgement depends on the software response time to the interrupt. Figure 4, page 8, shows the interaction between changing input states and the $\overline{INT}$ and $\overline{CS}$ terminals.

If desired the user may disable interrupts (*wake up/interrupt command*) from the 33972 device and read the switch states on a periodic basis. Switch activation and deactivation faster than the MCU read rate will not be acknowledged.

The 33972 device will exit the Normal mode and enter the Sleep mode only with a valid sleep command.

Sleep Mode

Sleep mode is used to reduce system quiescent currents. Sleep mode may be entered only by sending the *sleep command.* All register settings programmed in Normal mode will be maintained in Sleep mode.

The 33972 will exit Sleep mode and enter Normal mode when any of the following events occur:

- Input Switch Change of State (when enabled)
- Interrupt Timer Expire
- Falling Edge of $\overline{WAKE}$
- Falling Edge of $\overline{INT}$ (with V_{DD} = 5.0 V and $\overline{WAKE}$ at Logic [1])
- Falling Edge of $\overline{CS}$ (with V_{DD} = 5.0 V)
- Power-ON Reset (POR)

The V_{DD} supply may be removed from the device during Sleep mode. However removing V_{DD} from the device in Sleep mode will disable a wake-up from falling edge of $\overline{INT}$ and $\overline{CS}$.

Note In cases where $\overline{CS}$ is used to wake the device, the first SO data message is not valid.

The sleep command contains settings for two programmable timers for Sleep mode, the interrupt timer and the scan timer, as shown in Table 13 The interrupt timer is used as a periodic wake-up timer. When the timer expires, an interrupt is generated and the device enters Normal mode.

Note The interrupt timer in the 33972 device may be disabled by programming the interrupt bits to logic [1 1 1].

Table 14 shows the programmable settings of the Interrupt timer.

Table 13. Sleep Command

Sleep Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	int timer	int timer	int timer	scan timer	scan timer	scan timer

Table 14. Interrupt Timer

Bits 543	Interrupt Period
000	32 ms
001	64 ms
010	128 ms
011	256 ms
100	512 ms
101	1.024 s
110	2.048 s
111	No interrupt wake-up

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The scan timer sets the polling period between input switch reads in Sleep mode. The period is set in the *sleep command* and may be set to 000 (no period) to 111 (64 ms). In Sleep mode when the scan timer expires, inputs will behave as programmed prior to sleep command. The 33972 will wake up for approximately 125 μs and read the switch inputs. At the end of the 125 μs, the input switch states are compared with the switch state prior to sleep command. When switch state changes are detected, an interrupt (when enabled; refer to *wake-up/interrupt command* description on page 13) is generated and the device enters Normal mode. Without switch state changes, the 33972 will reset the scan timer, inputs become tri-state, and the Sleep mode continues until the scan timer expires again.

Table 15 shows the programmable settings of the Scan timer.

Table 15. Scan Timer

Bits 210	Scan Period
000	No Scan
001	1.0 ms
010	2.0 ms
011	4.0 ms
100	8.0 ms
101	16 ms
110	32 ms
111	64 ms

Note The interrupt and scan timers are disabled in the Normal mode.

Figure 3, page 8, is a graphical description of how the 33972 device exits Sleep mode and enters Normal mode. Notice that the device will exit Sleep mode when the interrupt timer expires or when a switch change of state occurs. The falling edge of $\overline{\text{INT}}$ triggers the MCU to wake from Sleep state. Figure 9 illustrates the current consumed during Sleep mode. During the 125 μs, the device is fully active and switch states are read. The quiescent current is calculated by integrating the normal running current over scan period plus approximately 60 μA.

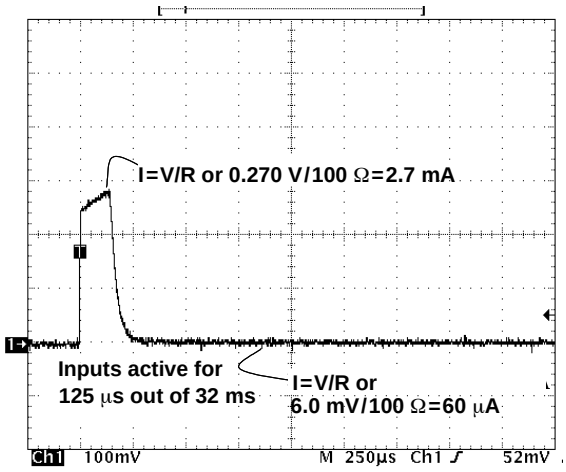

Figure 9. Sleep Current Waveform

Temperature Monitor

With multiple switch inputs closed and the device programmed with the wetting current timers disabled, considerable power will be dissipated by the IC. For this reason temperature monitoring has been implemented. The temperature monitor is active in the Normal mode only. When the IC temperature is above the thermal limit, the temperature monitor will do all of the following:

- Generate an interrupt.
- Force all 16 mA pullup and pulldown current sources to revert to 2.0 mA current sources.
- Maintain the 2.0 mA current source and all other functionality.
- Set the thermal flag bit in the SPI output register.

The thermal flag bit in the SPI word will be cleared on rising edge of $\overline{\text{CS}}$ provided the die temperature has cooled below the thermal limit. When die temperature has cooled below thermal limit, the device will resume previously programmed settings.

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APPLICATIONS

Introduction

The 33972's primary function is the detection of open or closed switch contacts. However, there are many features that allow the device to be used in a variety of applications. The following is a list of applications to consider for the IC:

- Sensor Power Supply
- Switch Monitor for Metallic or Elastomeric Switches
- Analog Sensor Inputs (Ratiometric)
- Power MOSFET/LED Driver and Monitor
- Multiple 33972 Devices in a Module System

The following paragraphs describe the applications in detail.

Sensor Power Supply

Each input may be used to supply current to sensors external to a module. Many sensors such as Hall effect, pressure sensors, and temperature sensors require a supply voltage to power the sensor and provide an open collector or analog output. Figure 10 shows how the 33972 may be used to supply power and interface to these types of sensors. In an application where the input makes continuous transitions, consider using the *wake-up/interrupt command* to disable the interrupt for the particular input.

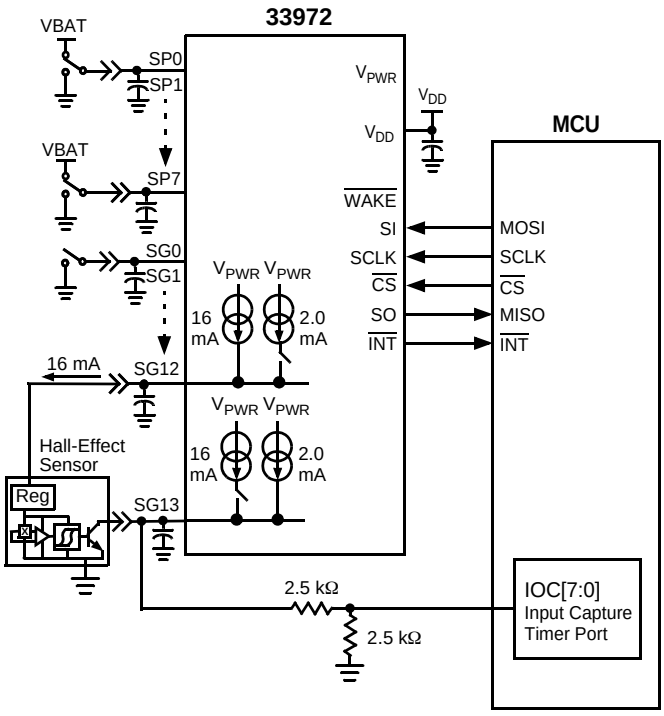

Figure 10. Sensor Power Supply

Metallic/Elastomeric Switch

Metallic switch contacts often develop higher contact resistance over time owing to contact corrosion. The corrosion is induced by humidity, salt, and other elements that exist in the environment. For this reason the 33972 provides two settings for contacts. When programmed for metallic switches, the device provides higher wetting current to keep switch contacts free of oxides. The higher current occurs for the first 20 ms of switch closure. Where longer duration of wetting current is desired, the user may send the *wetting current timer command* and disable the timer. Wetting current will be continuous to the closed switch. After the time period set by the MCU, the *wetting current timer command* may be sent again to enable the timer. The user must consider power dissipation on the device when disabling the timer. (Refer to the paragraph entitled Temperature Monitor, page 19.)

To increase the amount of wetting current for a switch contact, the user has two options. Higher wetting current to a switch may be achieved by paralleling SGn or SPn inputs. This will increase wetting current by 16 mA for each input added to the switch contact. The second option is to simply add an external resistor pullup to the V_{PWR} supply for switch-to-ground inputs or a resistor to ground for a switch-to-battery input. Adding an external resistor has no effect on the operation of the device.

Elastomeric switch contacts are made of carbon and have a high contact resistance. Resistance of 1.0 kΩ is common. In applications with elastomeric switches, the pullup and pulldown currents must be reduced to prevent excessive power dissipation at the contact. Programming for a lower current settings is provided in the Device Operation Section beginning on page 12 under Table 3, Metallic Command.

Analog Sensor Inputs (Ratiometric)

The 33972 features a 22-to-1 analog multiplexer. Setting the binary code for a specific input in the *analog command* allows the microcontroller to perform analog to digital conversion on any of the 22 inputs. On rising edge of $\overline{CS}$ the multiplexer connects a requested input to the AMUX terminal. The AMUX terminal is clamped to max of V_{DD} volts regardless of the higher voltages present on the input terminal. After an input has been selected as the analog, the corresponding bit in the next SO data stream will be logic [0].

The input terminal, when selected as analog, may be configured as analog with high impedance, analog with 2.0 mA pullup, or analog with 16 mA pullup. Figure 11, page 21, shows how the 33972 may be used to provide a ratiometric reading of variable resistive input.

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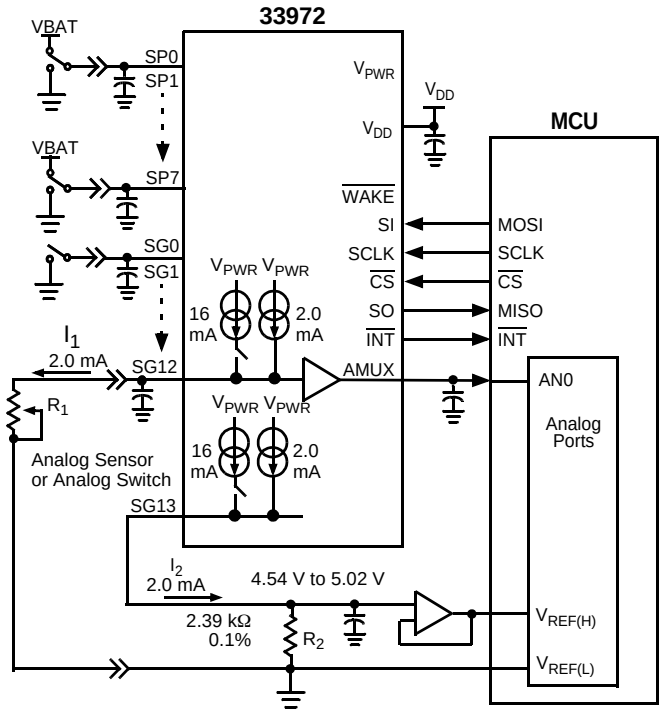

Figure 11. Analog Ratiometric Conversion

To read a potentiometer sensor, the wiper should be grounded and brought back to the module ground, as illustrated in Figure 11. With the wiper changing the impedance of the sensor, the analog voltage on the input will represent the position of the sensor.

Using the Analog feature to provide 2.0 mA of pullup current to an analog sensor may induce error due to the accuracy of the current source. For this reason, a ratiometric conversion must be considered. Using two current sources (one for the sensor and one to set the reference voltage to the A/D converter) will yield a maximum error (owing to the 33972) of 4%.

Higher accuracy may be achieved through module level calibration. In this example, we use the resistor values from Figure 11 and assume the current sources are 4% from each other. The user may use the module end-of-line tester to calculate the error in the A/D conversion. By placing a 2.0 kΩ, 0.1% resistor in the end-of-line test equipment and assuming a perfect 2.0 mA current source from the 33972, a calculated A/D conversion may be obtained. Using the equation yields the following:

$$ADC = \frac{I1 \times R1}{I2 \times R2} \times 225$$

$$ADC = \frac{2.0\ mA \times 2.0\ k\Omega}{2.0\ mA \times 2.39\ k\Omega} \times 225$$

$$ADC = 213\ counts$$

The ADC value of 213 counts is the value with 0% error (neglecting the resistor tolerance and AMUX input offset voltage). Now we can calculate the count value induced by the mismatch in current sources. From a sample device the maximum current source was measured at 2.05 mA and minimum current source was measured at 1.99 mA. This yields 3% error in A/D conversion. The A/D measurement will be as follows:

$$ADC = \frac{1.99\ mA \times 2.0\ k\Omega}{2.05\ mA \times 2.39\ k\Omega} \times 225$$

$$ADC = 207\ counts$$

This A/D conversion is 3% low in value. The error correction factor of 1.03 may be used to correct the value:

$$ADC = 207\ counts \times 1.03$$

$$ADC = 213\ counts$$

An error correction factor may then be stored in E^2 memory and used in the A/D calculation for the specific input. Each input used as analog measurement will have a dedicated calibrated error correction factor.

Power MOSFET/LED Driver and Monitor

Because of the flexible programming of the 33972 device, it may be used to drive small loads like LEDs or MOSFET gates. It was specifically designed to power up in the Normal mode with the inputs tri-state. This was done to ensure the LEDs or MOSFETs connected to the 33972 power up in the off-state. The Switch Programmable (SP0–SP7) inputs have a source-and-sink capability, providing effective MOSFET gate control. To complete the circuit, a pulldown resistor should be used to keep the gate from floating during the Sleep modes. Figure 12, page 22, shows an application where the SG0 input is used to monitor the drain-to-source voltage of the external MOSFET. The 1.5 kΩ resistor is used to set the drain-to-source trip voltage. With the 2.0 mA current source enabled, an interrupt will be generated when the drain-to-source voltage is approximately 1.0 V.

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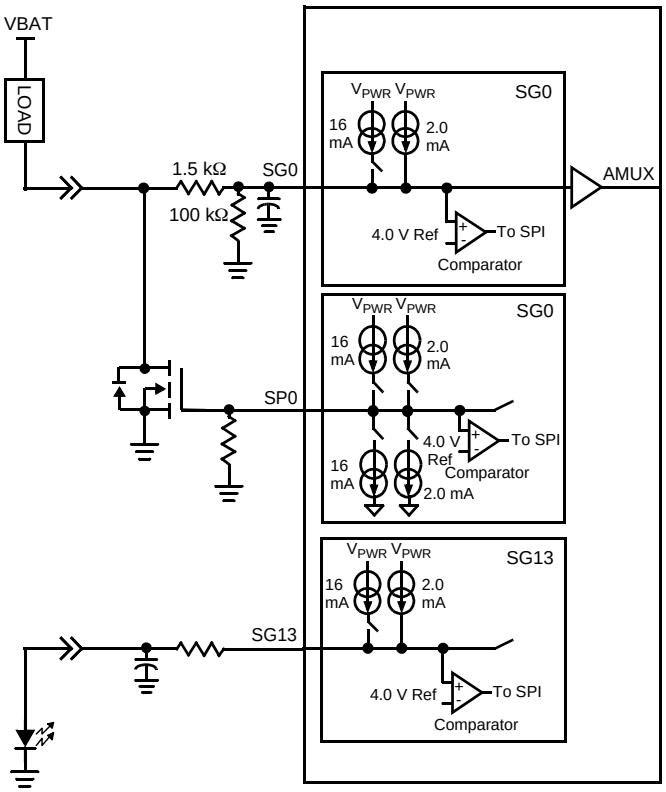

Figure 12. MOSFET or LED Driver Output

The sequence of commands (from Normal mode with inputs tri-state) required to set up the device to drive a MOSFET are as follows:

- *wetting current timer enable command* – Disable SPn wetting current timer (refer to Table 4, page 14).
- *metallic command* – Set SPn to 16 mA or 2.0 mA gate drive current (refer to Table 3, page 13).
- *settings command* – Set SPn as switch-to-battery (refer to Table 1, page 12).
- *tri-state command* – Disable tri-state for SPn (refer to Table 5, page 14).

After the *tri-state command* has been sent (tri-state disable), the MOSFET gate will be pulled to ground. From this point forward the MOSFET may be turned on and off by sending the *settings command*:

- *settings command* – SPn as switch-to-ground (MOSFET ON).
- *settings command* – SPn as switch-to-battery (MOSFET OFF).

Monitoring of the MOSFET drain in the OFF state provides open load detection. This is done by using an SGn input comparator. With the SGn input in tri-state, the load will pull up the SGn input to battery. With open load the SGn terminal is pulled down to ground through an external resistor. The open load is indicated by a logic [1] in the SO data bit.

The *analog command* may be used to monitor the drain voltage in the MOSFET ON state. By sourcing 2.0 mA of current to the 1.5 kΩ resistor, the analog voltage on the SGn terminal will be approximately:

$$V_{SGn} = I_{SGn} \times 1.5\ k\Omega + V_{DS}$$

As the voltage on the drain of the MOSFET increases, so does the voltage on the SGn terminal. With the SGn terminal selected as analog, the MCU may perform the A/D conversion.

Using this method for controlling unclamped inductive loads is not recommended. Inductive flyback voltages greater than V_{PWR} may damage the IC.

The SP0:SP7 terminals of this device may also be used to send signals from one module to another. Operation is similar to the gate control of a MOSFET.

For LED applications a resistor in series with the LED is recommended but not required. The switch-to-ground inputs are recommended for LED application. To drive the LED use the following commands:

- *wetting current timer enable command* – Disable SGn wetting current timer.
- *metallic command* – Set SGn to 16 mA.

From this point forward the LED may be turned on and off using the *tri-state command*:

- *tri-state command* – Disable tri-state for SGn (LED ON).
- *tri-state command* – Enable tri-state for SGn (LED OFF).

These parameters are easily programmed via SPI commands in Normal mode.

Multiple 33972 Devices in a Module System

Connecting power to the 33972 and the MCU for Sleep mode operation may be done in several ways. Table 16 shows several system configurations for power between the MCU and the 33972 and their specific requirements for functionality.

Table 16. Sleep Mode Power Supply

MCU V_{DD}	33972 V_{DD}	Comments
5.0 V	5.0 V	All wake-up conditions apply. (Refer to Sleep Mode, page 18.)
5.0 V	0 V	SPI wake-up is not possible.
0 V	5.0 V	Sleep mode not possible. Current from $\overline{CS}$ pullup will flow through MCU to V_{DD} that has been switched off. Negative edge of $\overline{CS}$ will put 33972 in Normal mode.
0 V	0 V	SPI wake-up is not possible.

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Multiple 33972 devices may be used in a module system. SPI control may be done in parallel or serial. However when parallel mode is used, each device is addressed independently (refer to MCU Interface Description, page 11). Therefore when sending the *sleep command*, one device will enter sleep before the other. For multiple devices in a system, it is recommended that the devices are controlled in serial (S0 from first device is connected to SI of second device). With two devices, 48 clock pulses are required to shift data in. When the $\overline{\text{WAKE}}$ feature is used to enable the power supply, both $\overline{\text{WAKE}}$ terminals should be connected to the enable terminal on the power supply. The $\overline{\text{INT}}$ terminals may be connected to one interrupt terminal on the MCU or may have their own dedicated interrupt to the MCU.

The transition from Normal to Sleep mode is done by sending the *sleep command*. With the devices connected in serial and the *sleep command* sent, both will enter Sleep mode on the rising edge of $\overline{\text{CS}}$. When Sleep mode is entered, the $\overline{\text{WAKE}}$ terminal will be logic [1]. If either device wakes up, the $\overline{\text{WAKE}}$ terminal will transition LOW, waking the other device.

A condition exists where the MCU is sending the *sleep command* ($\overline{\text{CS}}$ logic [0]) and a switch input changes state. With this event the device that detects this input will not transition to Sleep mode, while the second device will enter Sleep mode. In this case two *switch status commands* must be sent to receive accurate switch status data. The first *switch status command* will wake the device in Sleep mode. Switch status data may not be valid from the first *switch status command* because of the time required for the input voltage to rise above the 4.0 V input comparator threshold. This time is dependant on the impedance of SGn or SPn node. The second *switch status command* will provide accurate switch status information. It is recommended that software wait 10 ms to 20 ms between the two *switch status commands,* allowing time for switch input voltages to stabilize. With all switch states acknowledged by the MCU, the sleep sequence may be initiated. All parameters for Sleep mode should be updated prior to sending the *sleep command*.

The 33972 IC has an internal 5.0 V supply from V_{PWR} terminal. A POR circuit monitors the internal 5.0 V supply. In the event of transients on the V_{PWR} terminal, an internal reset may occur. Upon reset the 33972 will enter Normal mode with the internal registers as defined in Table 10, page 17. Therefore it is recommended that the MCU periodically update all registers internal to the IC.

Using the $\overline{\text{WAKE}}$ Feature

The 33972 provides a $\overline{\text{WAKE}}$ output and wake-up input designed to control an enable terminal on system power supply. While in the Normal mode, the $\overline{\text{WAKE}}$ output is LOW, enabling the power supply. In the Sleep mode, the $\overline{\text{WAKE}}$ terminal is HIGH, disabling the power supply. The $\overline{\text{WAKE}}$ terminal has a passive pullup to the internal 5.0 V supply but may be pulled up through a resistor to V_{PWR} supply (see Figure 14, page 24)

When the $\overline{\text{WAKE}}$ output is not used the terminal should be pulled up to the V_{DD} supply through a resistor as shown in Figure 13, page 24.

During the Sleep mode, a switch closure will set the $\overline{\text{WAKE}}$ terminal LOW, causing the 33972 to enter the Normal mode. The power supply will then be activated, supplying power to the V_{DD} terminal and the microprocessor and the 33972. The microprocessor can determine the source of the wake-up by reading the interrupt flag.

Cost and Flexibility

Systems requiring a significant number of switch interfaces have many discrete components. Discrete components on standard PWB consume board space and must be checked for solder joint integrity. An integrated approach reduces solder joints, consumes less board space, and offers wider operating voltage, analog interface capability, and greater interfacing flexibility.

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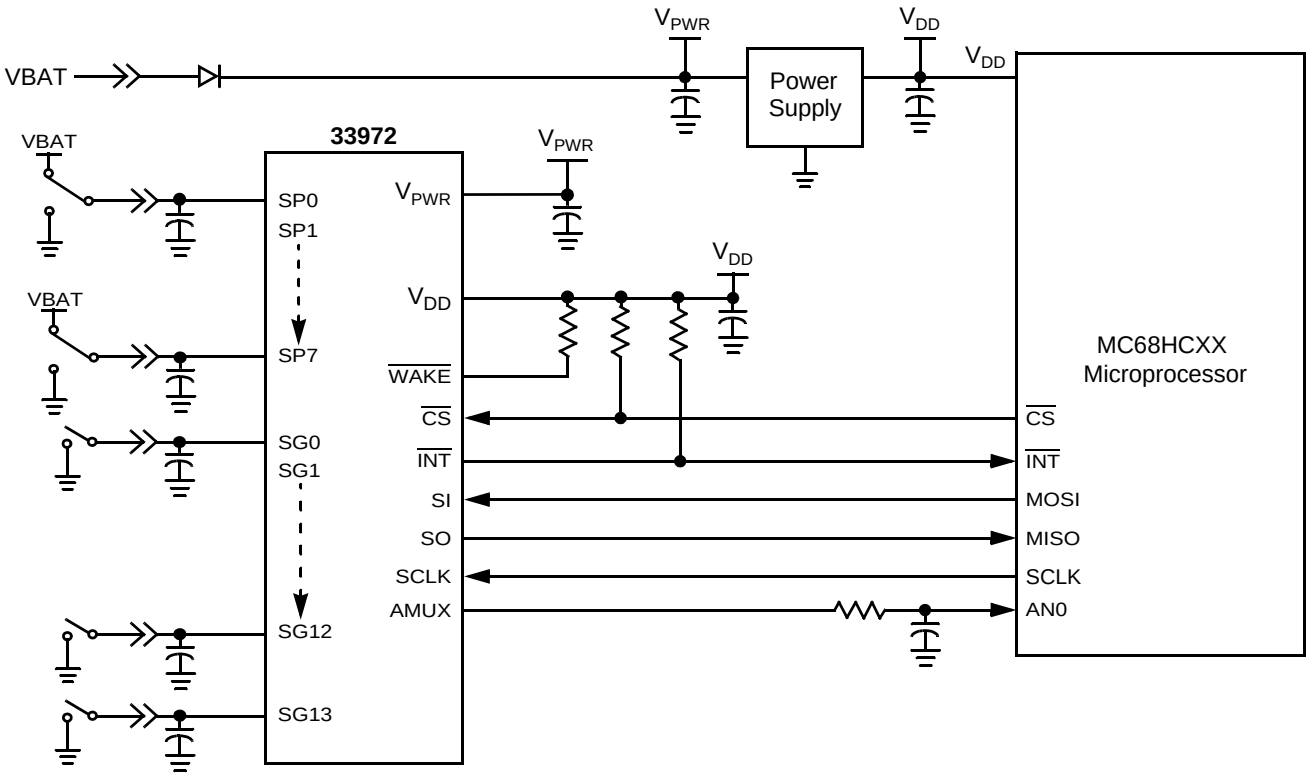

Figure 13. Power Supply Active in Sleep Mode

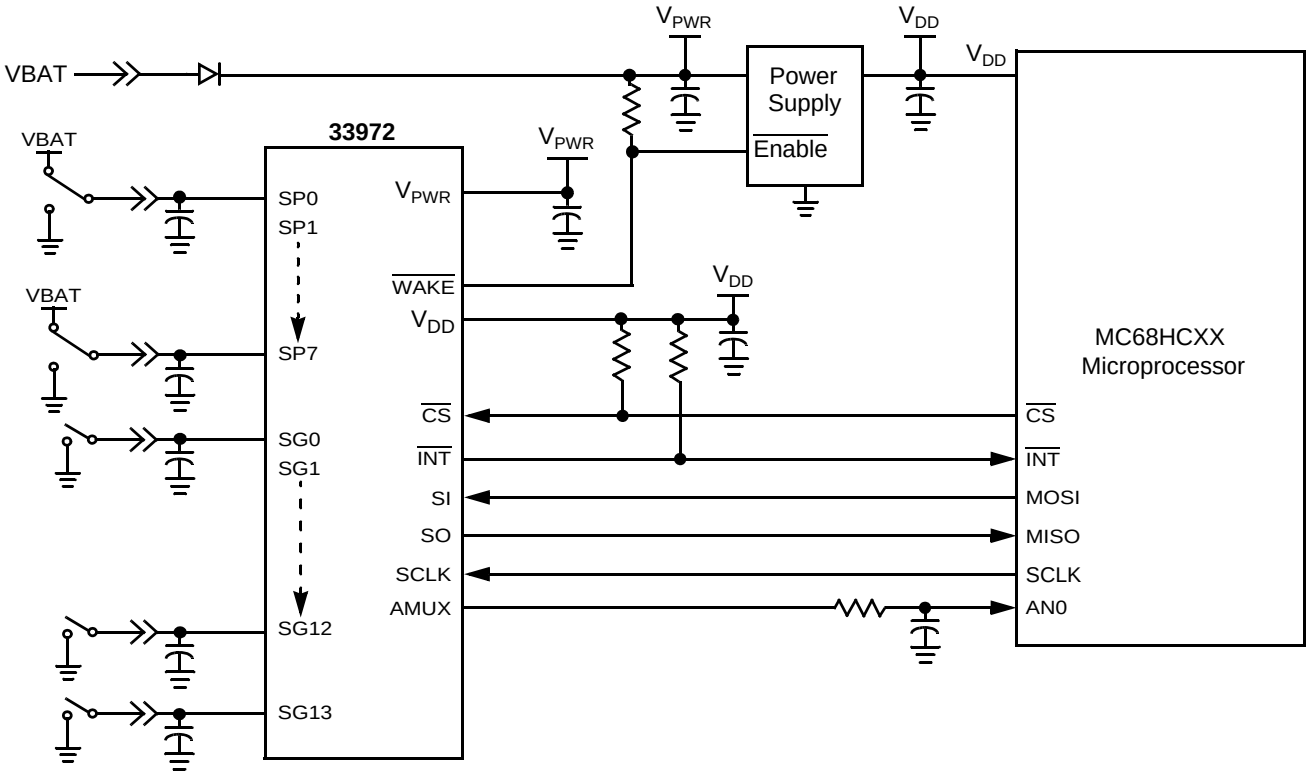

Figure 14. Power Supply Shutdown in Sleep Mode

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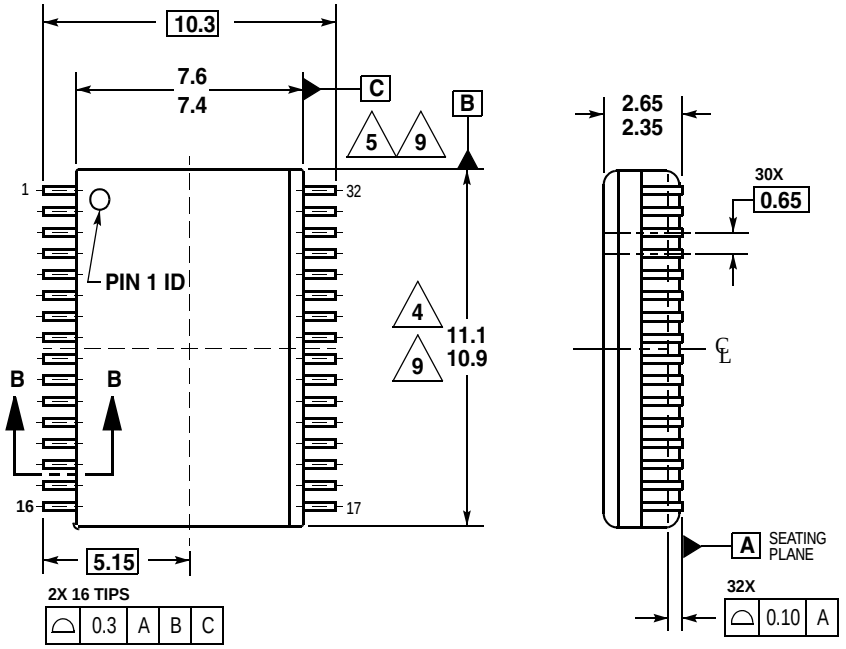
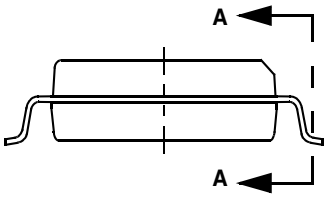
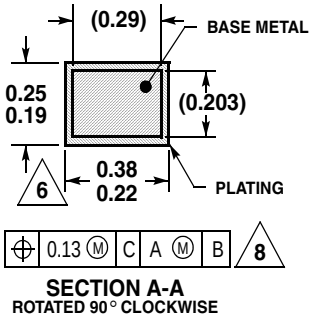
PACKAGE DIMENSIONS

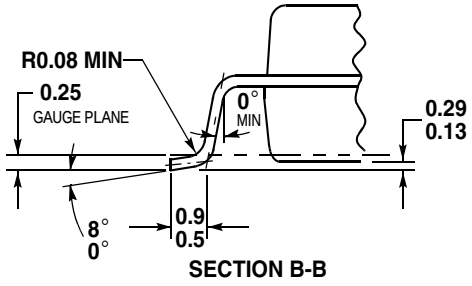
DWB SUFFIX
EW (Pb-FREE) SUFFIX
32-LEAD SOIC WIDE BODY
PLASTIC PACKAGE
CASE 1324-02
ISSUE A



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 MM PER SIDE. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.







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