



2SD1835

Bipolar Transistor 50V, 2A, Low VCE(sat), NPN Single NP

ON Semiconductor®
<http://onsemi.com>

Applications

- Voltage regulators, relay drivers, lamp drivers, electrical equipment

Features

- Adoption of FBET, MBIT processes
- Low collector-to-emitter saturation voltage
- Large current capacity
- Fast switching time

Specifications

Absolute Maximum Ratings at Ta=25°C

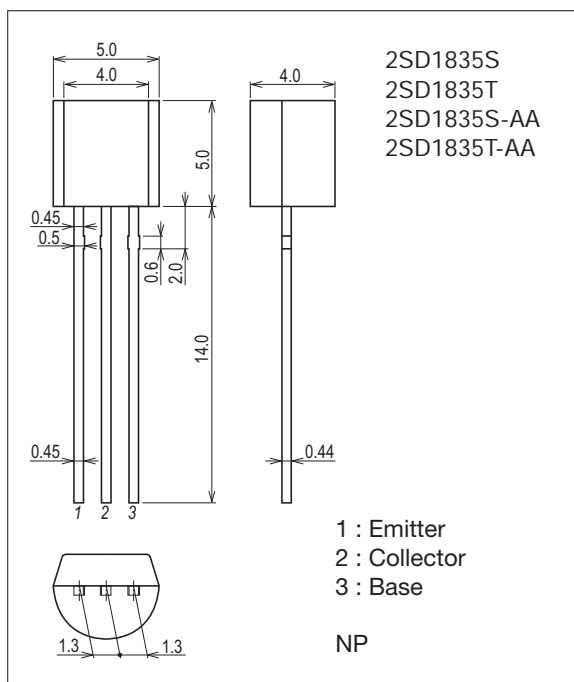
Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	VCBO		60	V
Collector-to-Emitter Voltage	VCEO		50	V
Emitter-to-Base Voltage	VEBO		6	V
Collector Current	IC		2	A
Collector Current (Pulse)	ICP		3	A
Collector Dissipation	PC		0.75	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

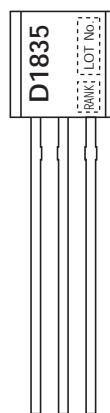
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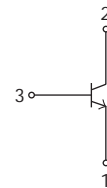
Product & Package Information

- Package : NP
- JEITA, JEDEC : SC-34A, TO-92, TO-226AA, SOT-54
- Minimum Packing Quantity : 1,500 pcs./box, 500pcs./bag

Marking



Electrical Connection



2SD1835

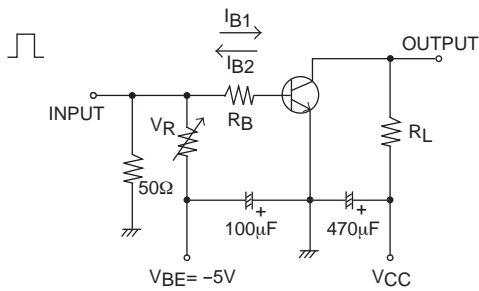
Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	ICBO	V _{CB} =50V, I _E =0A			100	nA
Emitter Cutoff Current	I _{EBO}	V _{EB} =4V, I _C =0A			100	nA
DC Current Gain	h _{FE1}	V _{CE} =2V, I _C =100mA	100*		560*	
	h _{FE2}	V _{CE} =2V, I _C =1.5A	40			
Gain-Bandwidth Product	f _T	V _{CE} =10V, I _C =50mA		150		MHz
Output Capacitance	C _{ob}	V _{CB} =10V, f=1MHz		12		pF
Collector-to-Emitter Saturation Voltage	V _{CE(sat)}	I _C =1A, I _B =50mA		0.15	0.4	V
Base-to-Emitter Saturation Voltage	V _{BE(sat)}	I _C =1A, I _B =50mA		0.9	1.2	V
Collector-to-Base Breakdown Voltage	V _{(BR)CBO}	I _C =10μA, I _E =0A	60			V
Collector-to-Emitter Breakdown Voltage	V _{(BR)CEO}	I _C =1mA, R _{BE} =∞	50			V
Emitter-to-Base Breakdown Voltage	V _{(BR)EBO}	I _E =10μA, I _C =0A	6			V
Turn-ON Time	t _{on}	See specified Test Circuit.		60		ns
Storage Time	t _{stg}			550		ns
Fall Time	t _f			30		ns

* : The 2SD1835 is classified by 100mA h_{FE} as follows :

Rank	R	S	T	U
h _{FE}	100 to 200	140 to 280	200 to 400	280 to 560

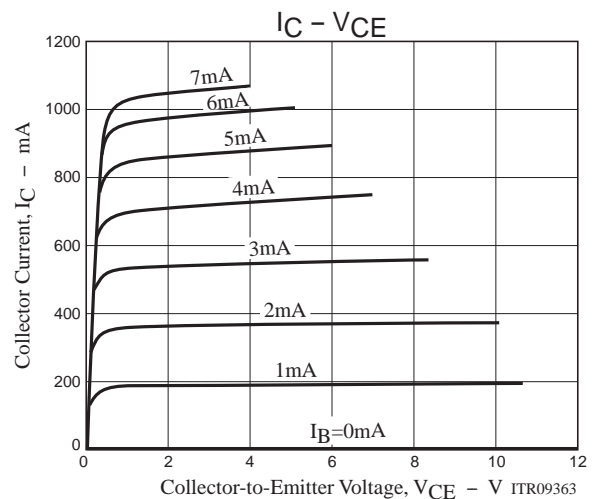
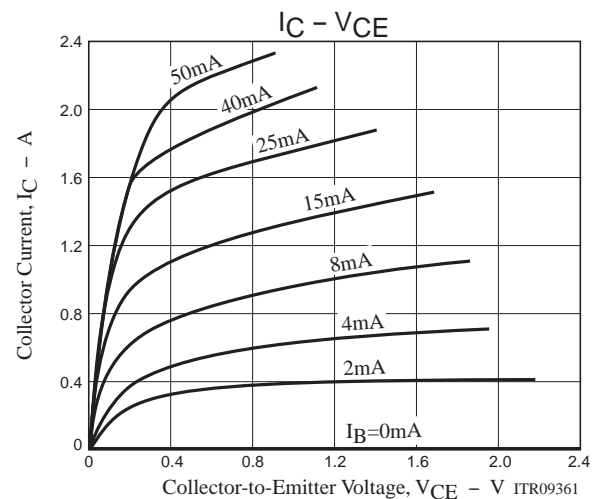
Switching Time Test Circuit

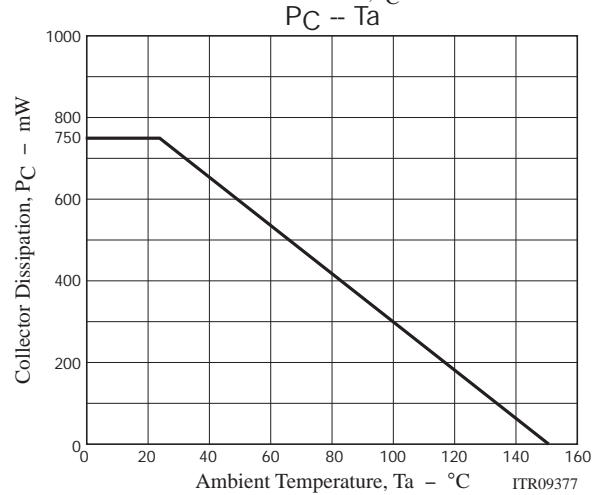
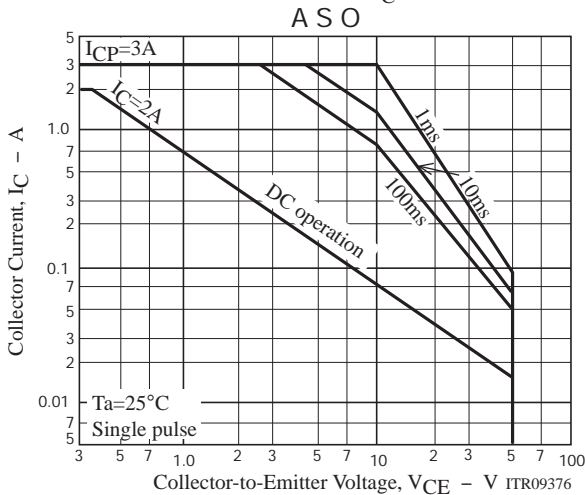
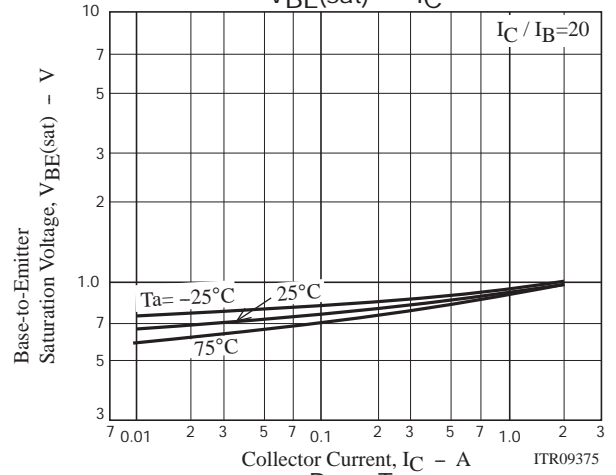
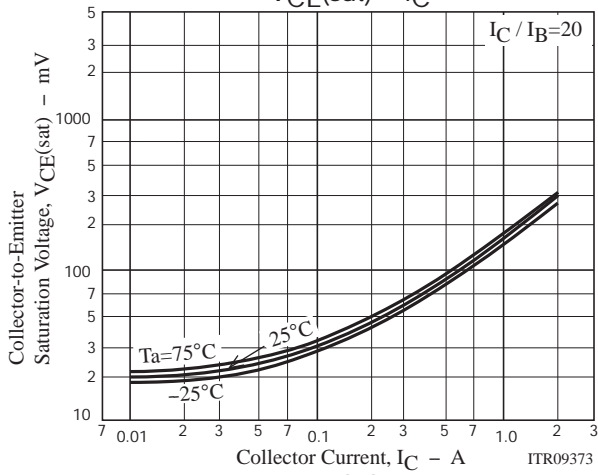
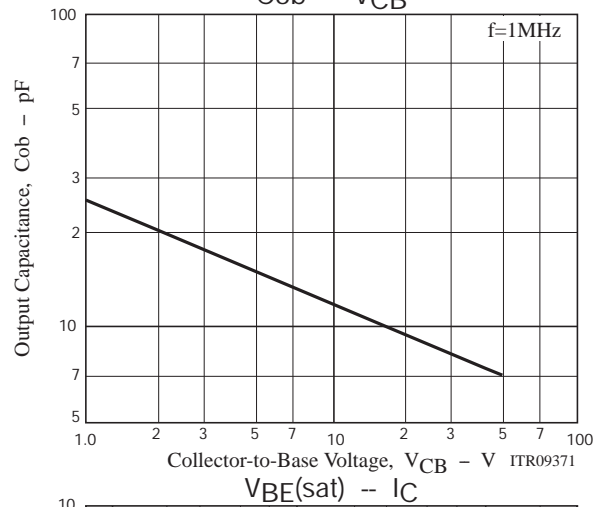
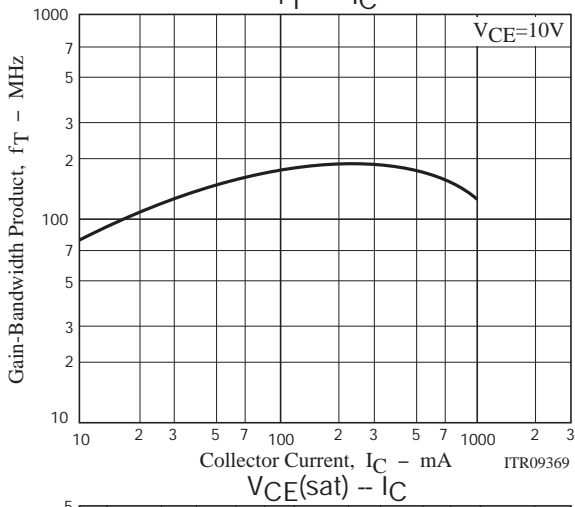
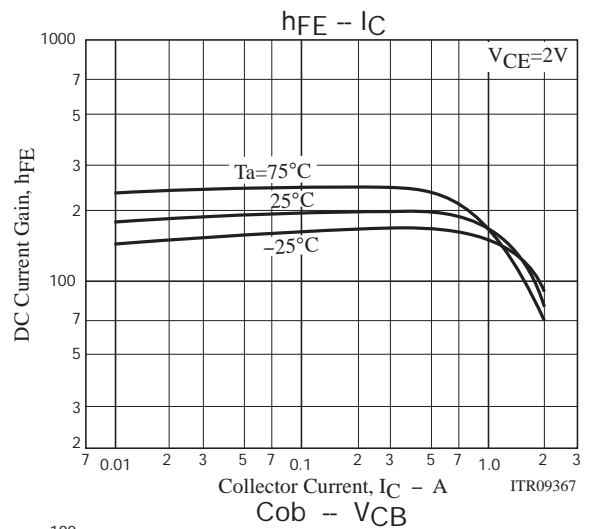
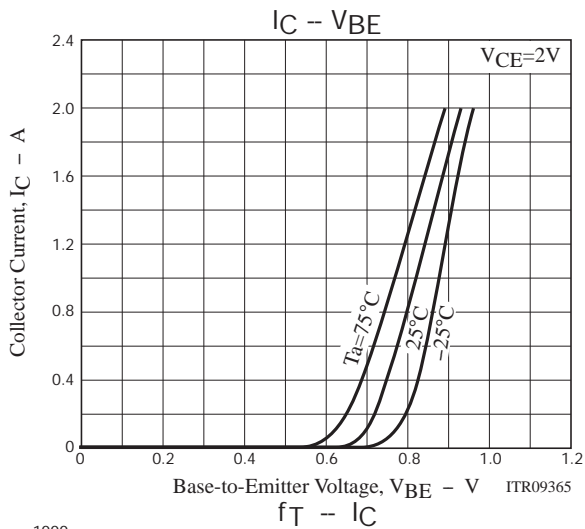


$$I_C = 10I_{B1} = -10I_{B2} = 500\text{mA}, V_{CC} = 25\text{V}$$

Ordering Information

Device	Package	Shipping	memo
2SD1835S	NP	500pcs./bag	Pb Free
2SD1835T	NP	500pcs./bag	
2SD1835S-AA	NP	1,500pcs./box	
2SD1835T-AA	NP	1,500pcs./box	





Taping Specification

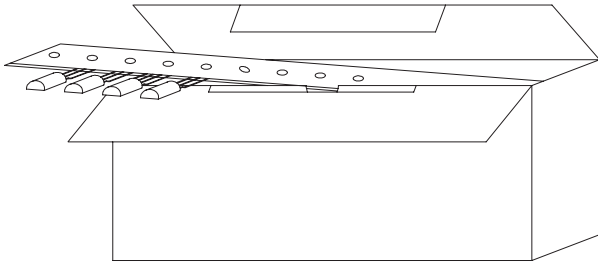
2SD1835S-AA, 2SD1835T-AA

1. Packing Format

Package Name	Packing Type	Maximum Number of devices contained (pcs)		Packing format
		Inner BOX (C-2)	number of contained	
N P	A A	Dimensions:mm (external)	1,500	16 inner boxes contained (24,000pcs) Dimensions:mm (external) 585×345×200
		330×45×145		

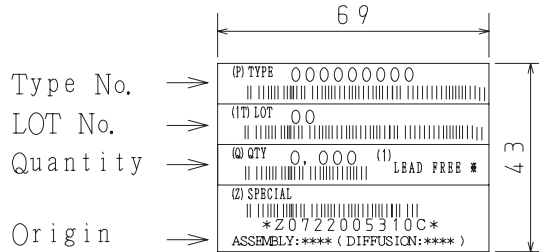
Packing method

Put zigzag folding in an inner box.



Inner box label

(unit:mm)



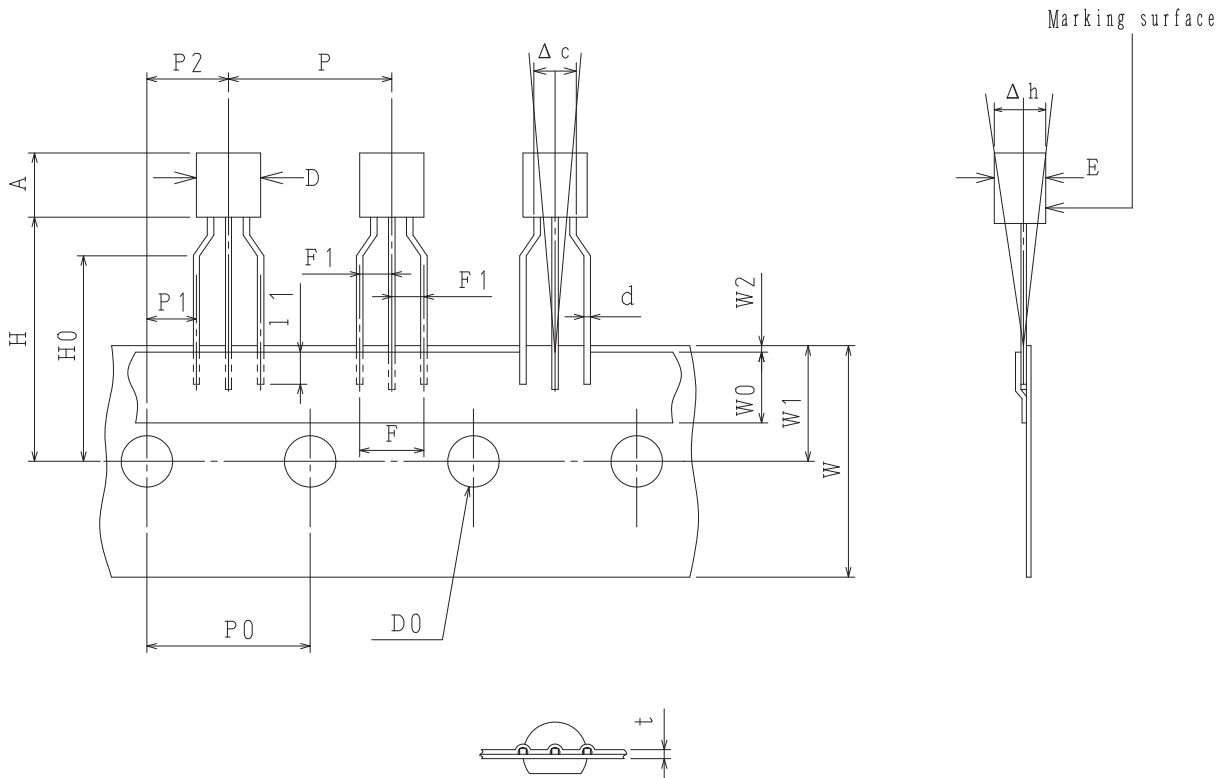
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping specifications

2-1. Carrier tape size



2-2. Taping size standard

unit:mm

Item	Symbol	Standard	Tolerance	
Work piece outside diameter	D	5.0	±0.2	
	E	4.0	±0.2	
Work piece height	A	5.0	±0.2	
Lead wire diameter	d	0.45×0.44t	±0.1	
Bonded lead wire	l1	2.0MIN		
Pitch between products	P	12.7	±0.5	
Pitch between perforations	P0	12.7	±0.2	
Distance between lead wire	F	5.0	+0.8 -0.2	
Lead wire pitch distance	F1	2.5	+0.2 -0.1	
Product inclination	Δh	0	±2.0	
Displacement of perforations	P1	3.85	±0.3	Measurement position is the bottom of the clinch
	P2	6.35	±0.3	
Displacement of tape	W2	0.5MAX		Not to be displaced to the outside of the board
Tape width	W	18.0	+1.0 -0.5	
Adhesive tape	W0	6.0	±1.5	
Displacement of perforations	W1	9.0	±0.5	
Work piece bottom surface position	H	19.0	±1.0	
Insert stopper position	H0	16.0	±0.5	
Work piece upper limit position	H1	24.5	±1.5	
Perforations diameter	D0	φ4.0	±0.2	
Tape thickness	t	0.6	±0.2	
Product inclination	Δc	0	±1.0	

Bag Packing Specification

2SD1835S, 2SD1835T

1. Packing condition

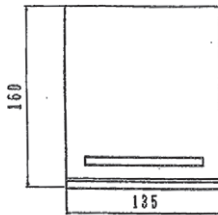
Storage package outline name	Maximum number of devices contained (pcs.)		Packing condition	
	Bags	Inner box	Devices contained	Outer box (A-1)
NP	500	B-1 Inner box dimensions : mm (external) 445×225×55	10,000	5 inner boxes contained 50,000 Outer box dimensions : mm (external) 470 × 250 × 300
				Outer box (A-2) 3 inner boxes contained 30,000 Outer box dimensions : mm (external) 470 × 250 × 190

3. Bar code label

(Unit : mm)

2. Bag dimensions

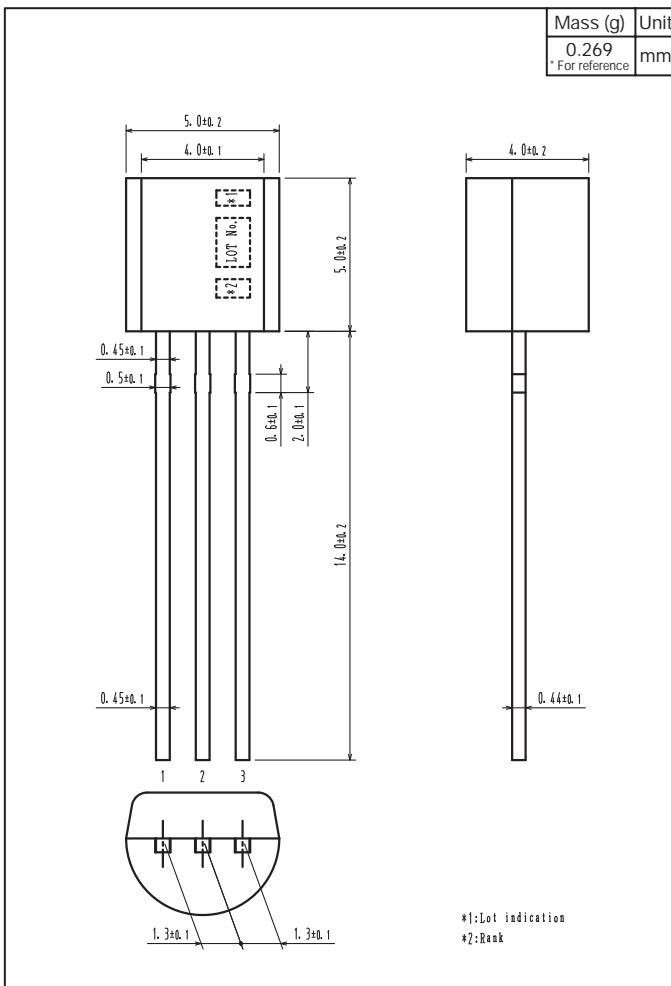
(Unit : mm)



*LEAD FREE 1 :
Lead-free External terminal surface
treatment product.

Outline Drawing

2SD1835S, 2SD1835T



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