STL27N15

N-CHANNEL 150V - 0.045 Ω - 27A PowerFLAT™ LOW GATE CHARGE STripFET™ MOSFET

TARGET DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STL15N15	150 V	<0.060 Ω	27 A(1)

- TYPICAL $R_{DS}(on)$ = 0.045 Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- VERY LOW GATE CHARGE



PowerFLAT™(6x5)

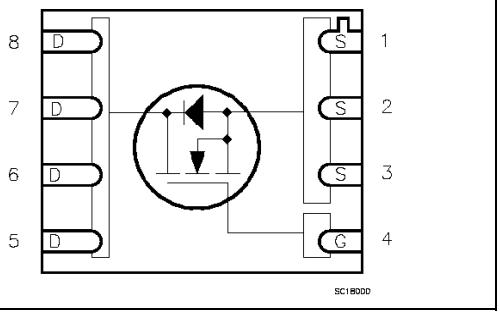
DESCRIPTION

This MOSFET series realized with STMicroelectronics unique "STripFET™" process has specifically been designed to minimize input capacitance and gate charge. It's therefore suitable as primary switch in advanced high efficiency, high frequency isolated DC-DC converter for telecom an computer application. The new PowerFLAT™ package allows e significant reduction in a board space without compromising performance.

APPLICATIONS

- HIGH-EFFICIENCY ISOLATED DC-DC CONVERTERS
- TELECOM AND BATTERY CHARGER ADAPTOR
- SYNCHRONOUS RECTIFICATION

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STL27N15	L27N15	PowerFLAT	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	150	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	150	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C (Steady State)	6	A
I_D	Drain Current (continuous) at T_C = 100°C	4	A
I_{DM}(3)	Drain Current (pulsed)	24	A
P_{tot}(2)	Total Dissipation at T_C = 25°C (Steady State)	4	W
P_{tot}(1)	Total Dissipation at T_C = 25°C	80	W
	Derating Factor	0.03	W/°C
dv/dt (5)	Peak Diode Recovery voltage slope	TBD	V/ns
T_{stg}	Storage Temperature	-55 to 150	°C
T_j	Operating Junction Temperature		

This is preliminary information on a new product forseen to be developped. Details are subject to change without notice

THERMAL DATA

Rthj-F Rthj-pcb(2)	Thermal Resistance Junction-Foot (Drain) Thermal Operating Junction-pcb	1.56 31.2	°C/W °C/W

.

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA

ON (6)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 3 A		0.045	0.060	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (6)	Forward Transconductance	V_{DS} = 50 V I_D = 5 A		TBD		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		TBD TBD TBD		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 50 V I_D = 3 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 50V I_D= 6A V_{GS}=10V		TBD TBD TBD	28	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 50 V I_D = 3 A R_G = 4.7Ω, V_{GS} = 10 V (Resistive Load, Figure 3)		TBD TBD		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(3)	Source-drain Current Source-drain Current (pulsed)				6 24	A A
V_{SD} (6)	Forward On Voltage	I_{SD} = 3 A V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} =6 A di/dt = 100A/µs V_{DD} = 30 V $_j$ = 150°C (see test circuit, Figure 5)		TBD TBD TBD		ns nC A

(1) The value is rated according $R_{thj\text{-}F}$.
(2) When Mounted on FR-4 board of 1 inch², 2oz Cu
(3) Pulse width limited by safe operating area.
(5) I_{SD} ≤6A, di/dt ≤300A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
(6) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Fig. 1: Unclamped Inductive Load Test Circuit

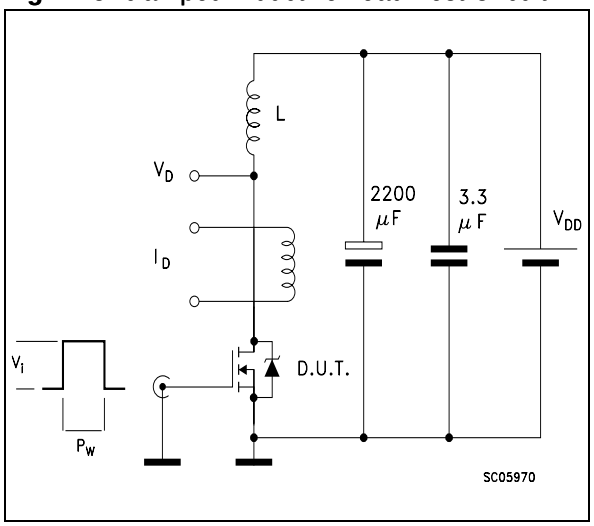


Fig. 2: Unclamped Inductive Waveform

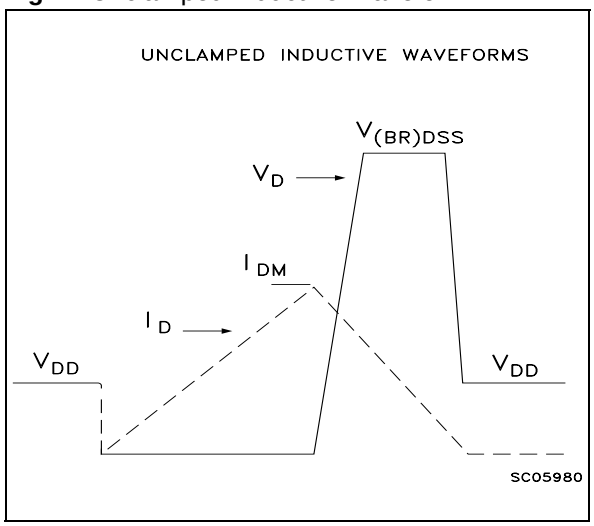


Fig. 3: Switching Times Test Circuits For Resistive Load

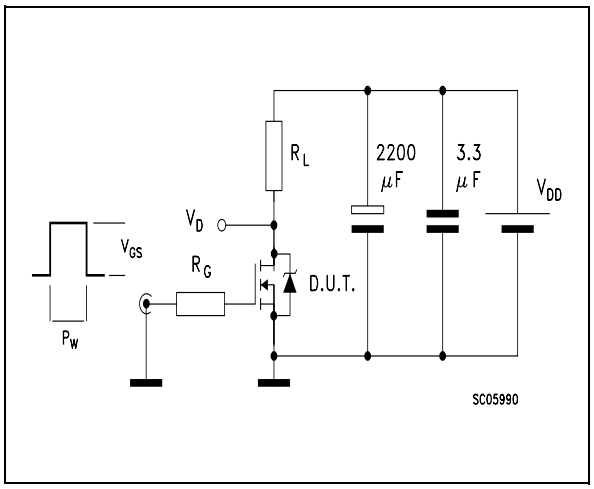


Fig. 4: Gate Charge test Circuit

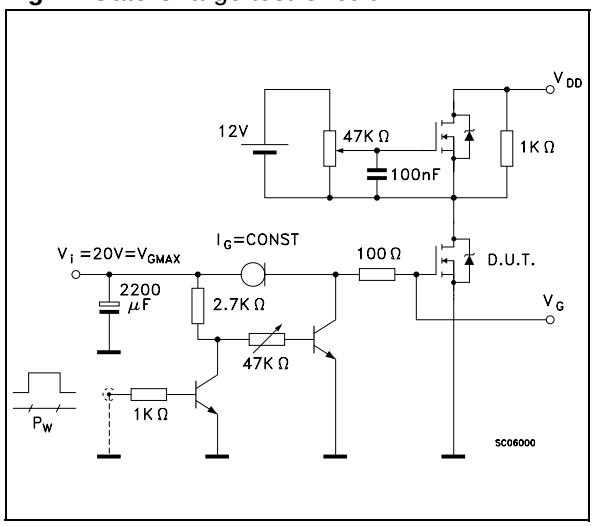
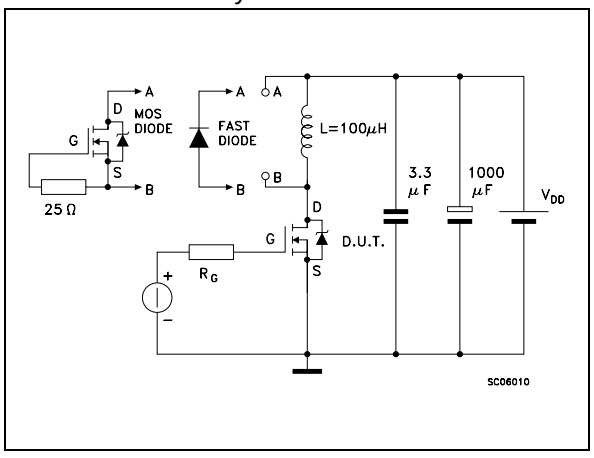
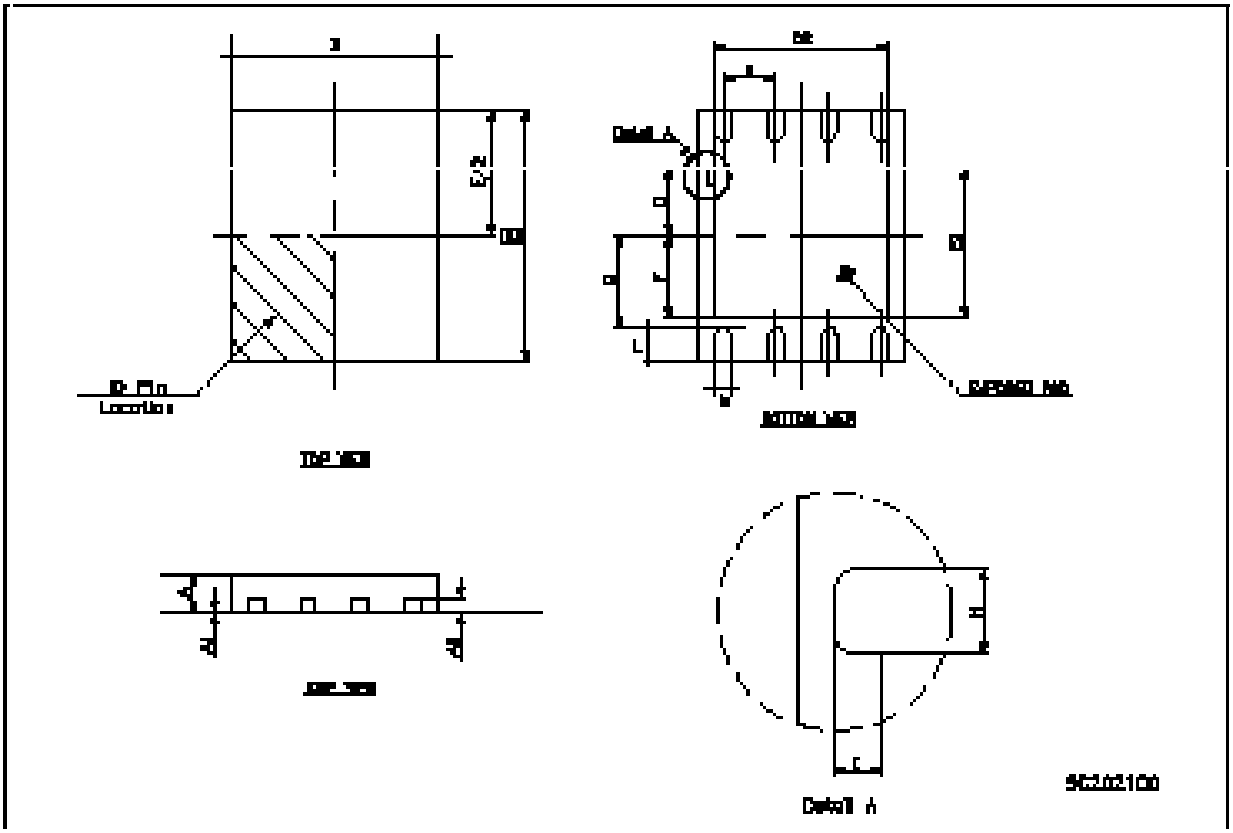


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerFLAT™(6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		1.00	0.031		0.039
A1		0.02			0.001	
b	0.35		0.47	0.014		0.018
C		1.61			0.063	
D		5.00			0.197	
D2	4.15		4.25	0.163		0.167
E		6.00			0.236	
E2	3.55		3.65	0.140		0.144
e		1.27			0.049	
F		1.99			0.078	
G		2.20			0.086	
H		0.40			0.015	
I		0.219			0.0086	
L	0.70		0.90	0.028		0.035



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
® 2003 STMicroelectronics - All Rights Reserved

All other names are the property of their respective owners.

STMicroelectronics GROUP OF COMPANIES
Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

http://www.st.com