19-1066; Rev 1; 11/09

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

General Description

The MAX1245 12-bit data-acquisition system combines an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and ultra-low power consumption. It operates from a single +2.375V to +3.3V supply, and its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™, and MICROWIRE™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1245 works with an external reference, and uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

This device provides a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down, and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface powers up the MAX1245, and the quick turn-on time allows it to be shut down between conversions. This technique can cut supply current to under 10µA at reduced sampling rates.

The MAX1245 is available in a 20-pin DIP package and an SSOP that occupies 30% less area than an 8-pin DIP. For supply voltages from +2.7V to +5.25V, use the pin-compatible MAX147.

Applications

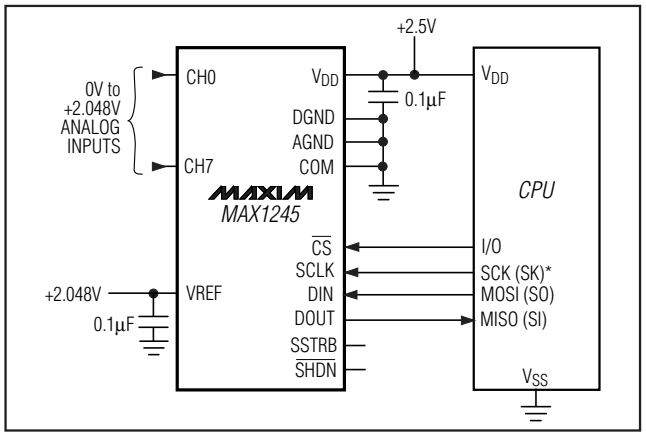
Portable Data Logging

Battery-Powered Instruments

Medical Instruments

Data Acquisition

Typical Operating Circuit



Features

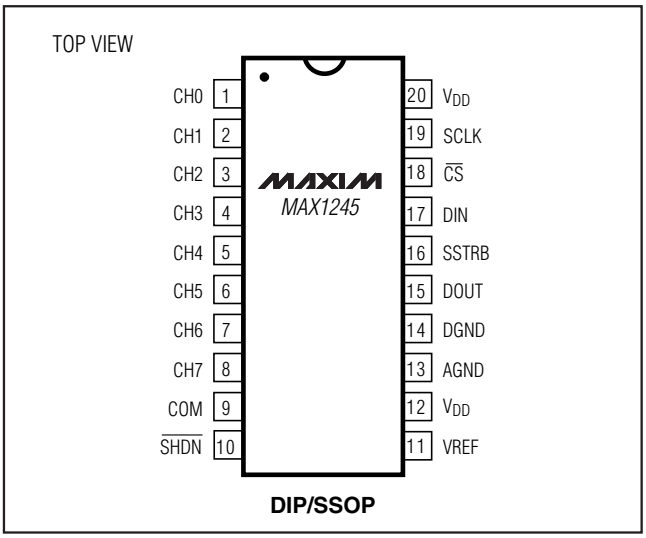
- ♦ **Single +2.375V to +3.3V Operation**
- ♦ **8-Channel Single-Ended or 4-Channel Differential Analog Inputs**
- ♦ **Low Power: 0.8mA (100ksps)**
  10µA (1ksps)
  1µA (power-down mode)
- ♦ **Internal Track/Hold, 100kHz Sampling Rate**
- ♦ **SPI/QSPI/MICROWIRE/TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **20-Pin DIP/SSOP Packages**

Ordering Information

PART*	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1245ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX1245BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX1245ACAP	0°C to +70°C	20 SSOP	±1/2
MAX1245BCAP	0°C to +70°C	20 SSOP	±1
MAX1245AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX1245BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX1245AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX1245BEAP	-40°C to +85°C	20 SSOP	±1

*Contact factory for availability of alternate surface-mount packages.

Pin Configuration



DIP/SSOP

SPI and QSPI are trademarks of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to +6V
AGND to DGND..... -0.3V to +0.3V
CH0–CH7, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND..... -0.3V to +6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C)..... 889mW
Operating Temperature Ranges
MAX1245_C_P ..... 0°C to +70°C
MAX1245_E_P ..... -40°C to +85°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.375V to +3.3V, COM = 0V, f_{CLK} = 1.5MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (100ksps), VREF = 2.048V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL	MAX1245A			±0.5	LSB
		MAX1245B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error				±0.5	±4	LSB
Gain Error (Note 3)				±0.5	±4	LSB
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.2		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0Vp-p to 2.048Vp-p, 100ksps, 1.5MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD		68			dB
Total Harmonic Distortion	THD	Up to the 5th harmonic			-76	dB
Spurious-Free Dynamic Range	SFDR		76			dB
Channel-to-Channel Crosstalk		50kHz, $2V_{p-p}$ (Note 4)		-85		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 1.5MHz, 12 clocks/conversion	8			
Track/Hold Acquisition Time	t_{ACQ}	External clock = 1.5MHz			2.0	µs
Aperture Delay				40		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.5		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		1.5	MHz
		Data transfer only	0		1.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.375V to +3.3V, COM = 0V, f_{CLK} = 1.5MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (100ksps), VREF = 2.048V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF/2			±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance		(Note 7)		16		pF
EXTERNAL REFERENCE						
VREF Input Voltage Range (Note 8)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.048V		82	120	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}		2.0			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 7)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.4	V
$\overline{SHDN}$ Input Current	I_{IN}	$\overline{SHDN}$ = 0V or V_{DD}			±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		V_{DD}/2 - 0.3		V_{DD}/2 + 0.3	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		V_{DD}/2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = open			±80	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.5		
Output Voltage High	V_{OH}	I_{SOURCE} =0.5mA	V_{DD} - 0.375			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 7)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		2.375		3.3	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input		0.8	1.3	mA
		Power-down		1.2	10	µA
Supply Rejection (Note 9)	PSR	V_{DD} = 2.375V to 3.3V, full-scale input, external reference = 2.048V		±0.3		mV

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

TIMING CHARACTERISTICS

(V_{DD} = +2.375V to +3.3V, COM = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

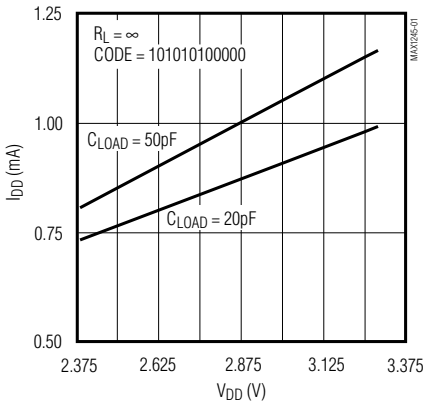
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}		2.0			µs
DIN to SCLK Setup	t_{DS}		200			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	20		260	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1			240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2			400	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		200			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse Width High	t_{CH}		300			ns
SCLK Pulse Width Low	t_{CL}		300			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1			260	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1			240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2			400	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 7)	0			ns

Note 1: Tested at V_{DD} = +2.375V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: External reference (VREF = +2.048V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: Guaranteed by design. Not subject to production testing.
Note 8: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 9: Measured as $|V_{FS}(2.375V) - V_{FS}(3.3V)|$.

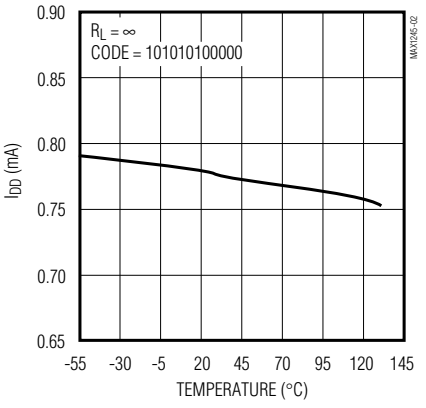
Typical Operating Characteristics

(V_{DD} = 2.5V, VREF = 2.048V, f_{CLK} = 1.5MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

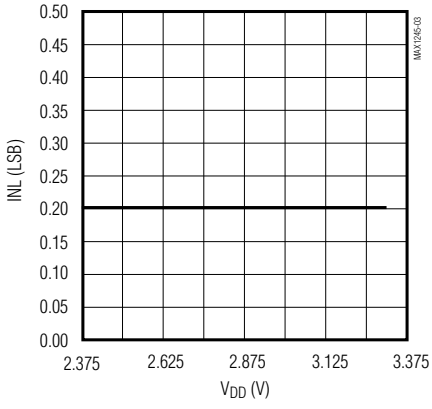
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



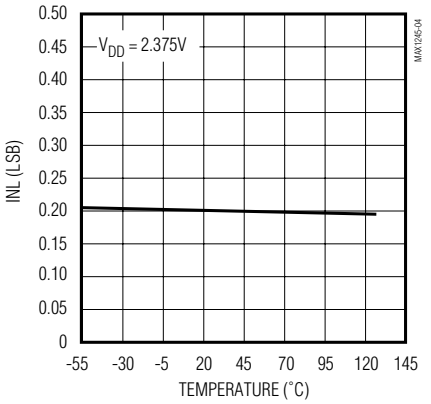
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



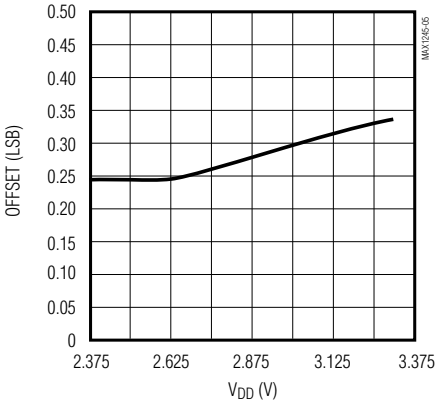
Typical Operating Characteristics (continued)

(V_{DD} = 2.5V, VREF = 2.048V, f_{CLK} = 1.5MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

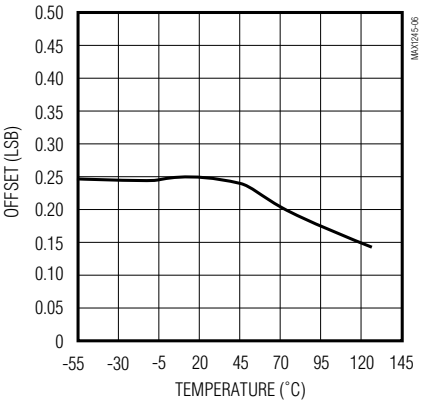
INTEGRAL NONLINEARITY vs. TEMPERATURE



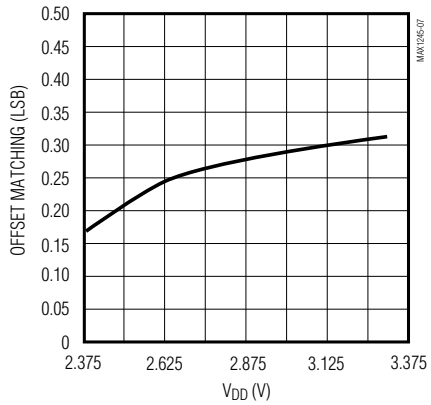
OFFSET vs. SUPPLY VOLTAGE



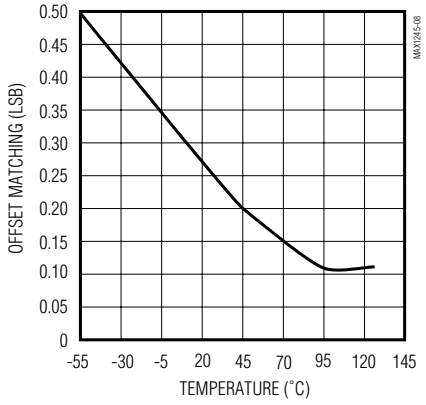
OFFSET vs. TEMPERATURE



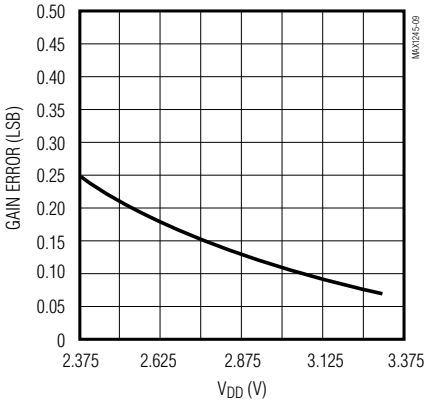
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. SUPPLY VOLTAGE



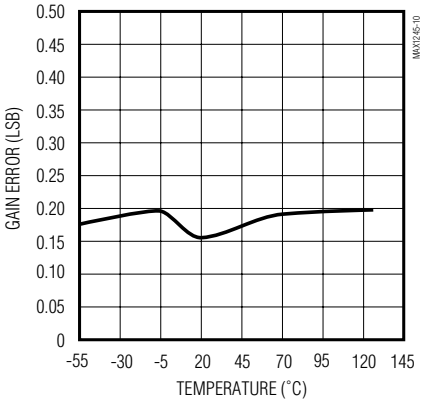
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



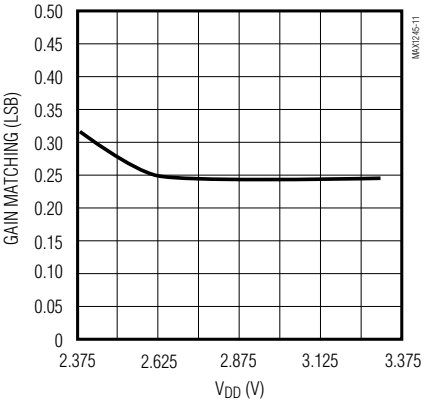
GAIN ERROR vs. SUPPLY VOLTAGE



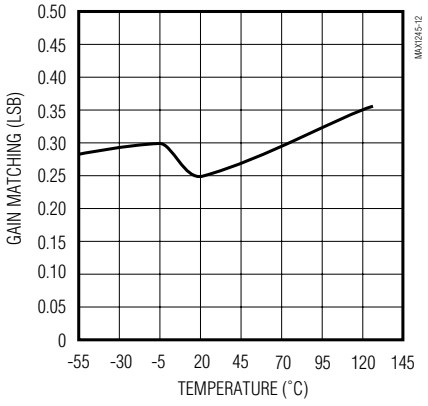
GAIN ERROR vs. TEMPERATURE



CHANNEL-TO-CHANNEL GAIN MATCHING vs. SUPPLY VOLTAGE



CHANNEL-TO-CHANNEL GAIN MATCHING vs. TEMPERATURE

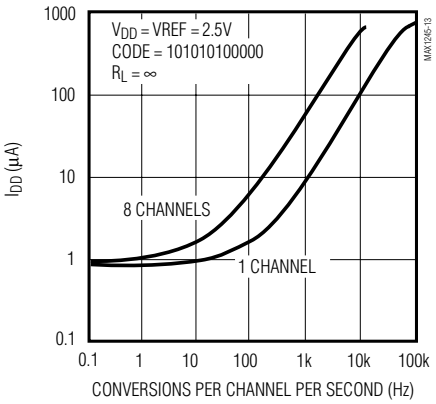


+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

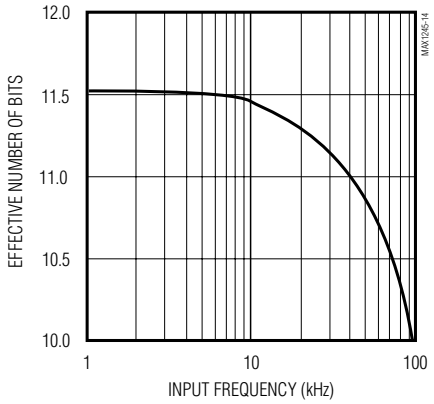
Typical Operating Characteristics (continued)

(V_{DD} = 2.5V, VREF = 2.048V, f_{CLK} = 1.5MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

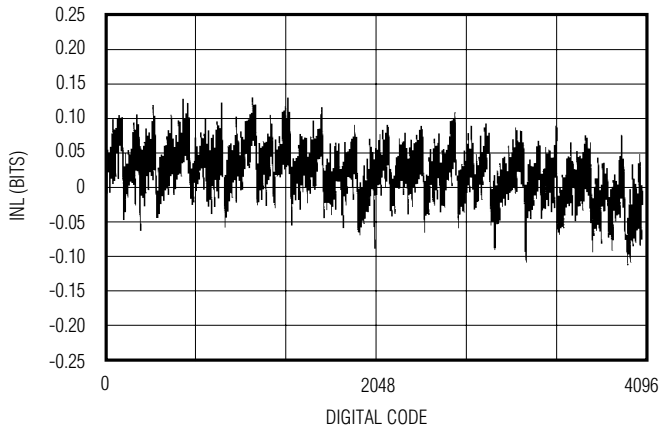
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE



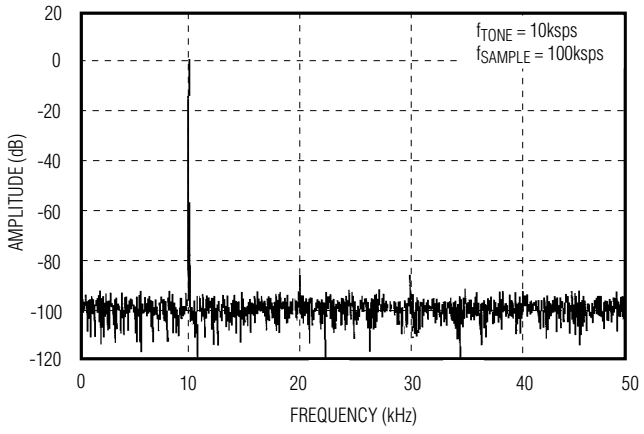
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



INTEGRAL NONLINEARITY



FFT PLOT



Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	COM	Ground reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1245 down to 10µA (max) supply current; otherwise, the MAX1245 is fully operational. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.5MHz. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. See *Hardware Power-Down* section.
11	VREF	External Reference Voltage Input for analog-to-digital conversion
12, 20	V_{DD}	Positive Supply Voltage
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX1245 begins the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

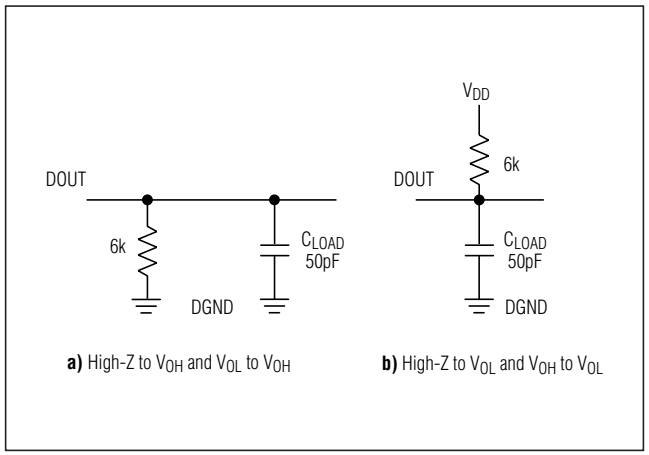


Figure 1. Load Circuits for Enable Time

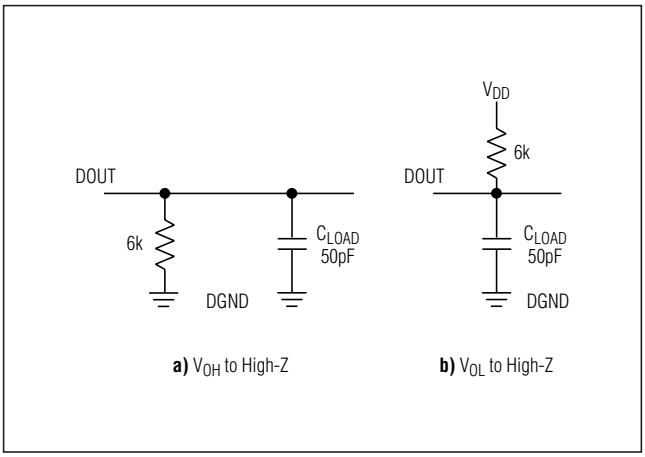


Figure 2. Load Circuits for Disable Time

+2.375V, Low-Power, 8-Channel, Serial 12-Bit ADC

Detailed Description

The MAX1245 analog-to-digital converter (ADC) uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). No external hold capacitors are required. Figure 3 is a block diagram of the MAX1245.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels with Tables 2 and 3.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input, IN+, to the negative input, IN- (In single-ended mode, IN- is simply COM). This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x [(V_{IN+}) - (V_{IN-})] from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 16pF$$

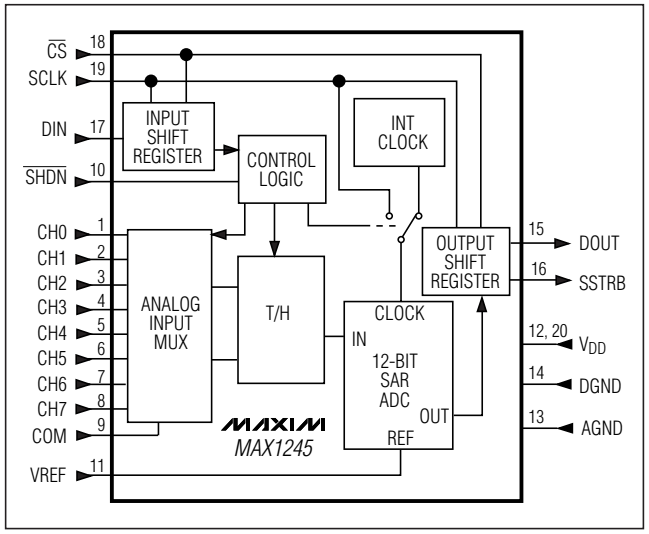


Figure 3. Block Diagram

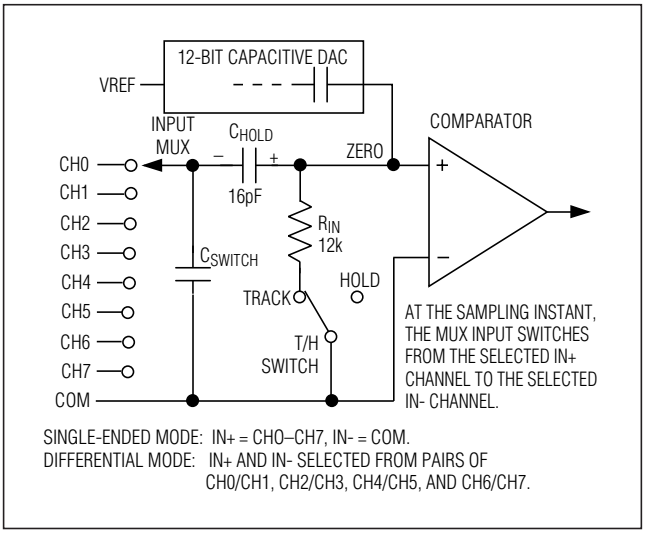


Figure 4. Equivalent Input Circuit

where R_{IN} = 12kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 2.0µs. Note that source impedances below 1kΩ do not significantly affect the AC performance of the ADC. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over two milliamperes, as excessive current will degrade the conversion accuracy of the on channel.

Quick Look

To quickly evaluate the MAX1245's analog performance, use the circuit of Figure 5. The MAX1245 requires a control byte to be written to DIN before each conversion. Tying DIN to V_{DD} feeds in control bytes of $FF (HEX), which trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 alters the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1245's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1245 is compatible with Microwire, SPI, and QSPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit,* the simplest software interface requires only three 8-bit transfers to

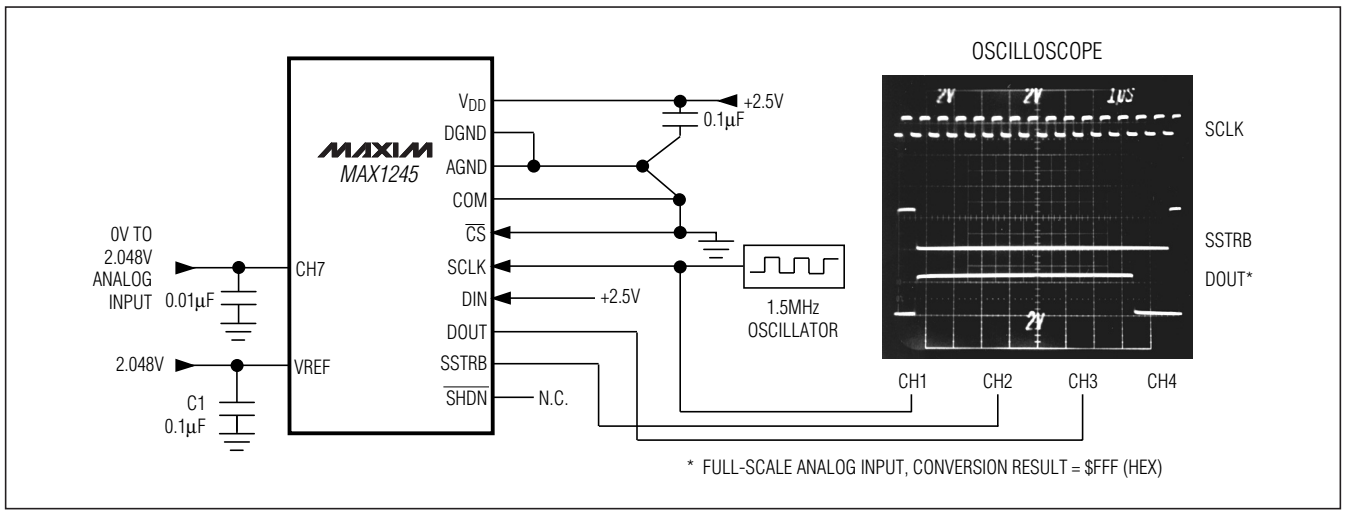


Figure 5. Quick-Look Circuit

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Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/BIP	SGL/DIF	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion (Tables 2 and 3).
3	UNI/BIP	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/DIF	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Power-down (I_Q = 1.2µA) 0 1 Unassigned 1 0 Internal clock mode 1 1 External clock mode

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result). See Figure 17 for MAX1245 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 1.5MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 HEX) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 HEX) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (Figure 14). For bipolar inputs, the output is two's-complement (Figure 15). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX1245 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1245. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion. SSTRB pulses high for one clock period after the control byte's last bit. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

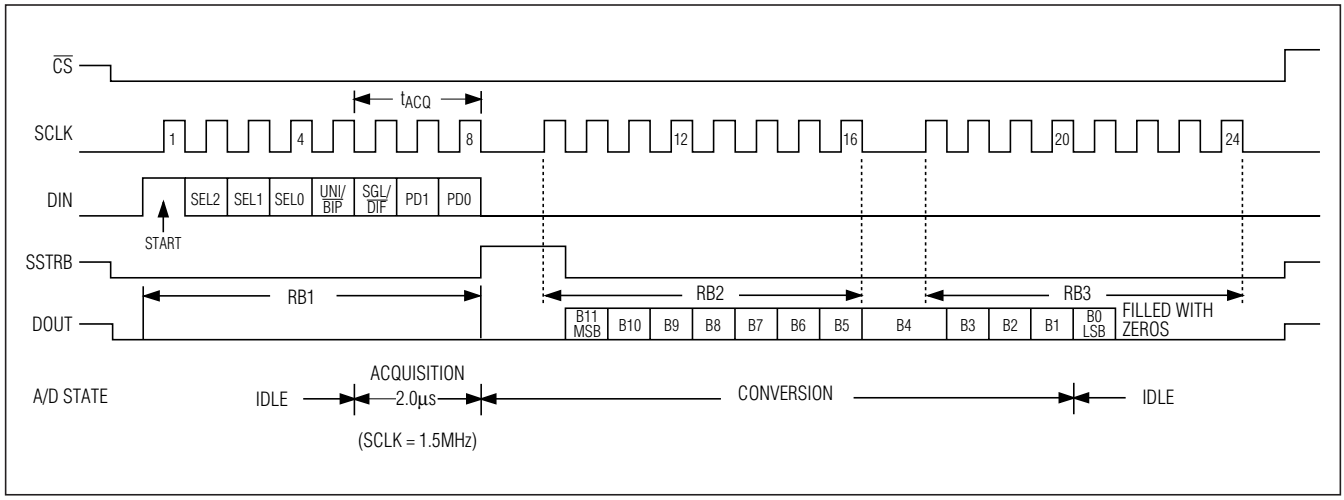


Figure 6. 24-Clock External-Clock-Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{CLK} \leq 1.5MHz$)

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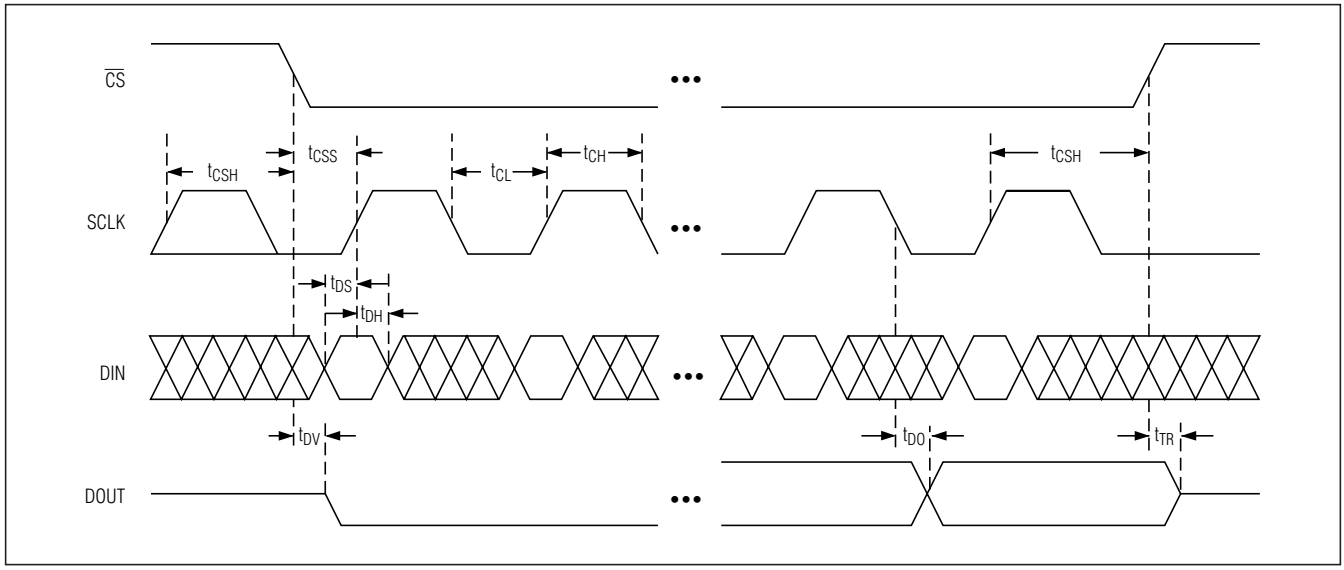


Figure 7. Detailed Serial-Interface Timing

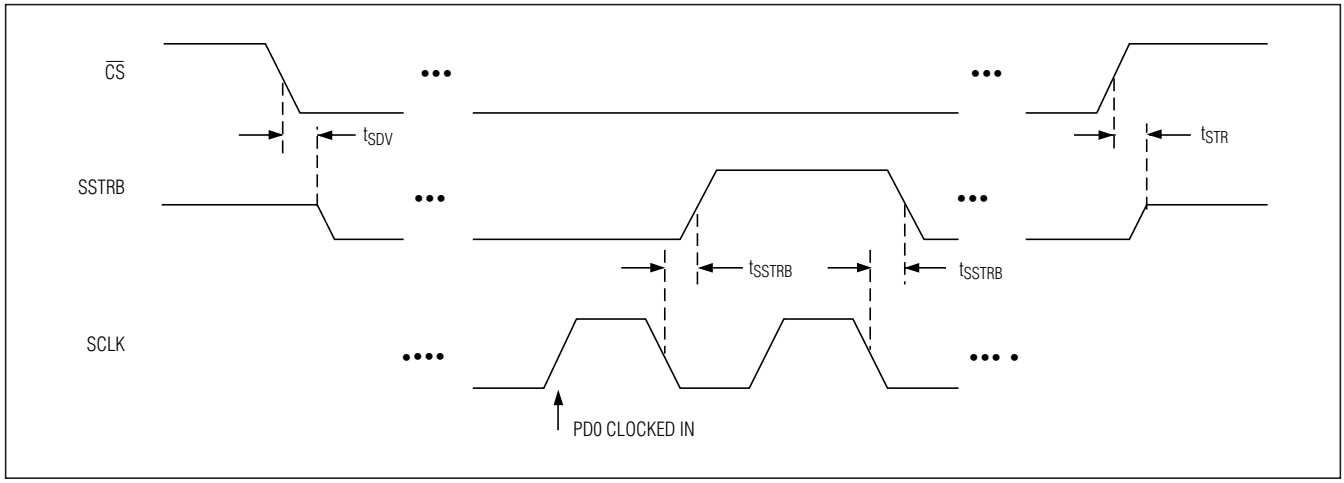


Figure 8. External-Clock-Mode SSTRB Detailed Timing

Internal Clock

In internal clock mode, the MAX1245 generates its own conversion clock internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to 1.5MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1245 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is

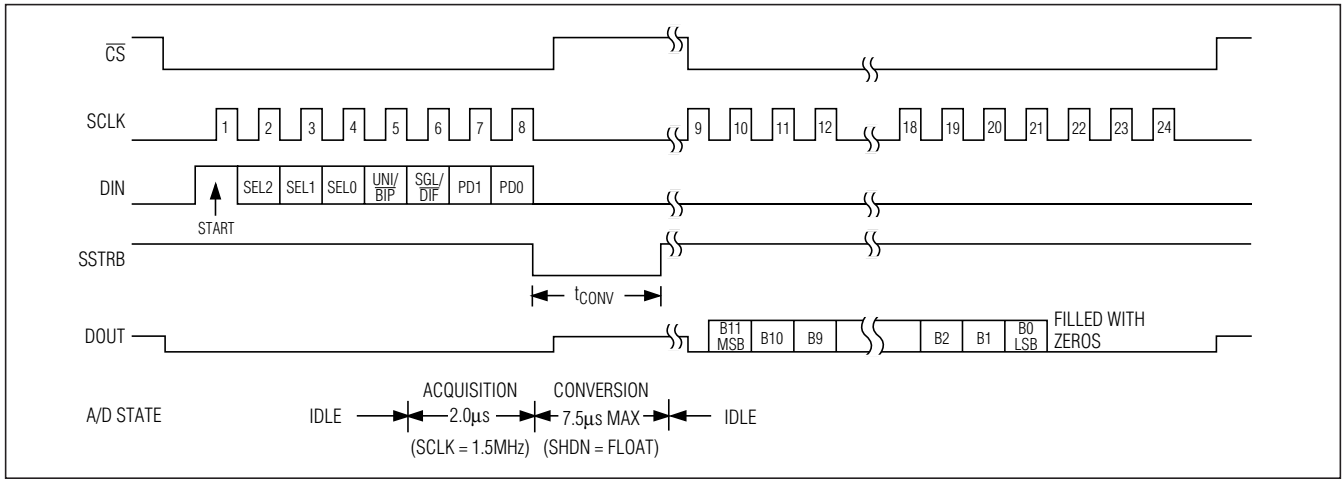


Figure 9. Internal Clock Mode Timing

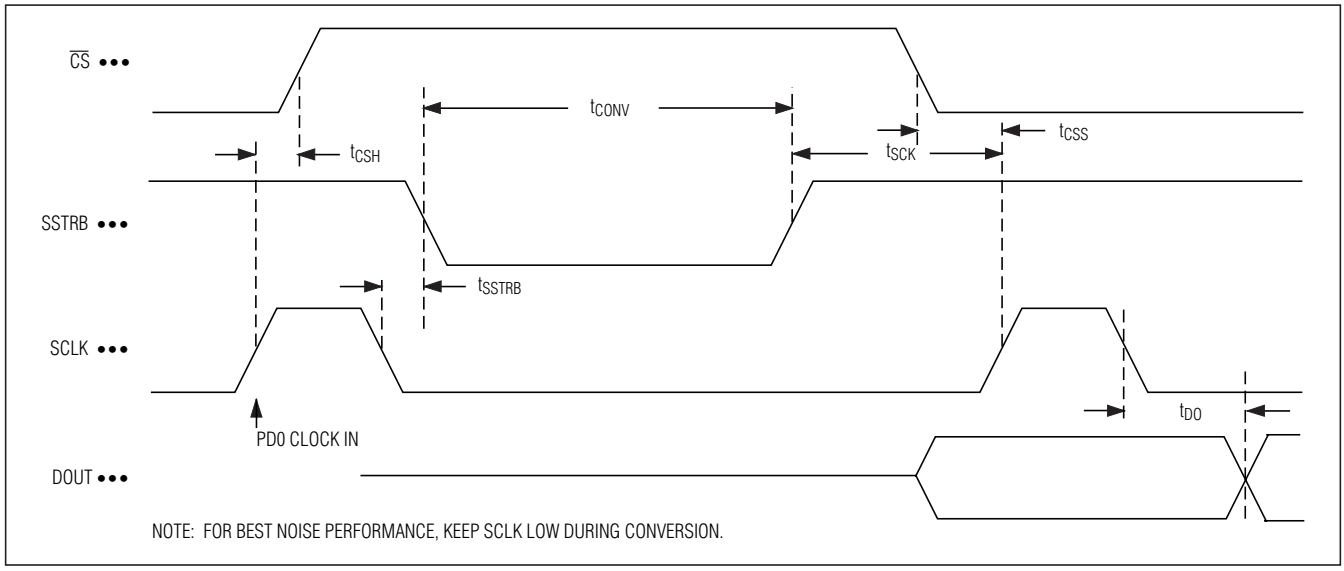


Figure 10. Internal Clock Mode SSTRB Detailed Timing

selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1245 at clock rates exceeding 1.5MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 2.0µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX1245. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If CS is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

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The fastest the MAX1245 can run is 15 clocks per conversion with $\overline{CS}$ held low between conversions. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX1245. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1245 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have stabilized, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros.

Power-Down

The MAX1245's automatic power-down mode can save considerable power when operating at speeds below the maximum sampling rate. Figure 13 shows the average supply current as a function of the sampling rate. You can save power by placing the converter in a low-current shutdown state between conversions.

Select power-down via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high (Tables 1 and 4). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte (Table 5).

Power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} typically to 1.2µA.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 4, PD1 and PD0

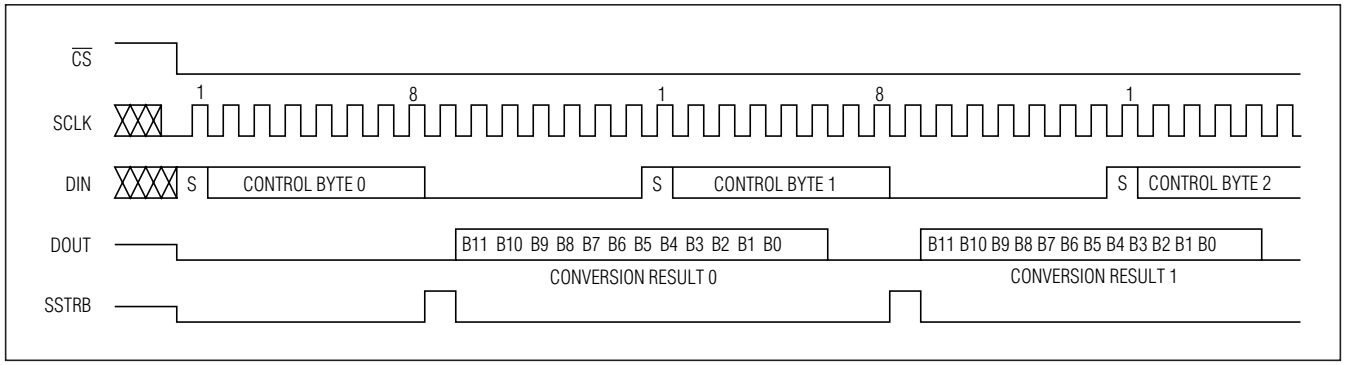


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

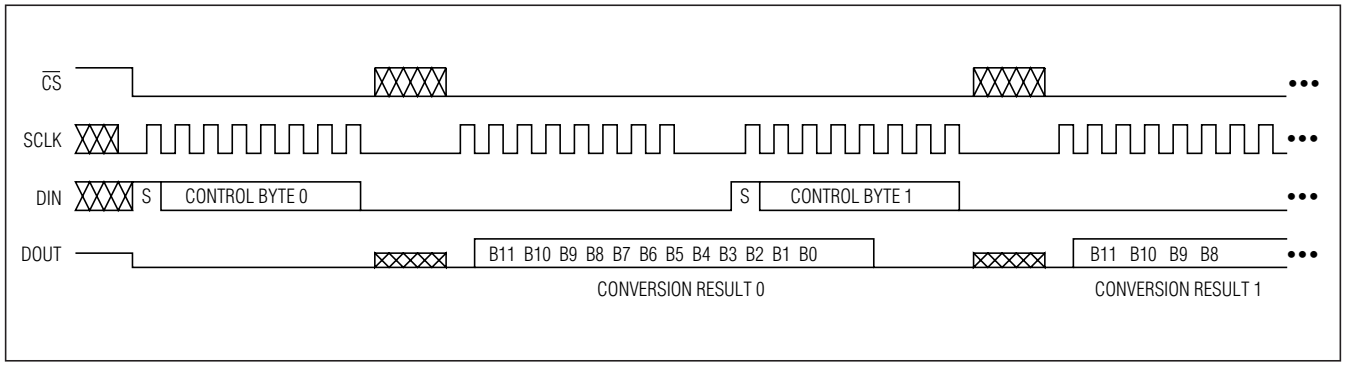


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

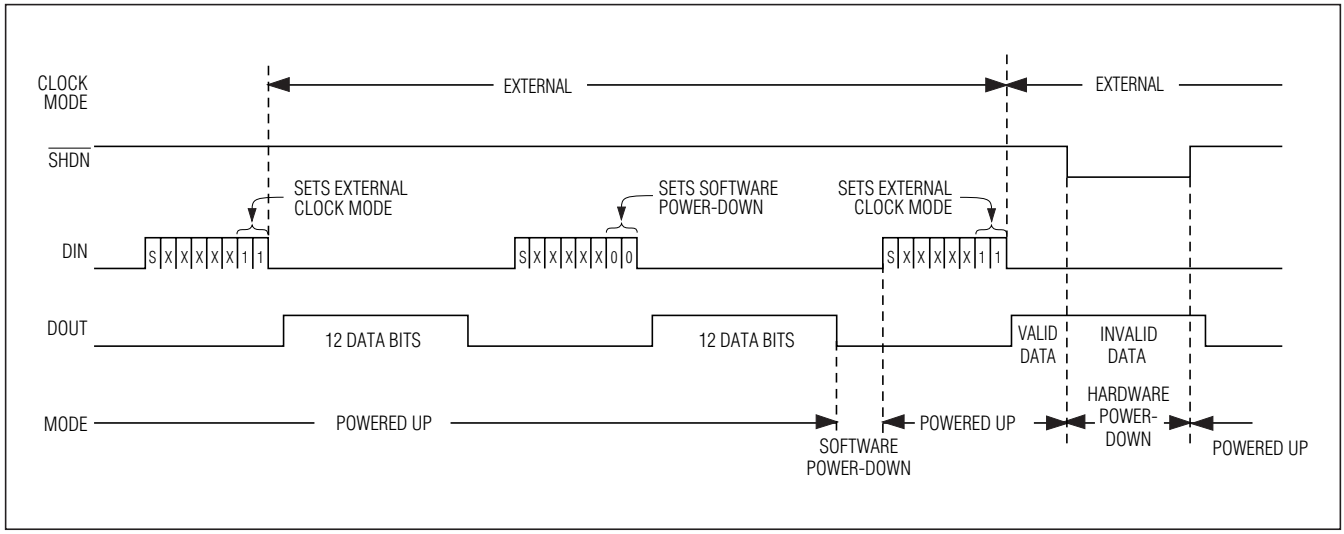


Figure 12a. Timing Diagram Power-Down Modes, External Clock

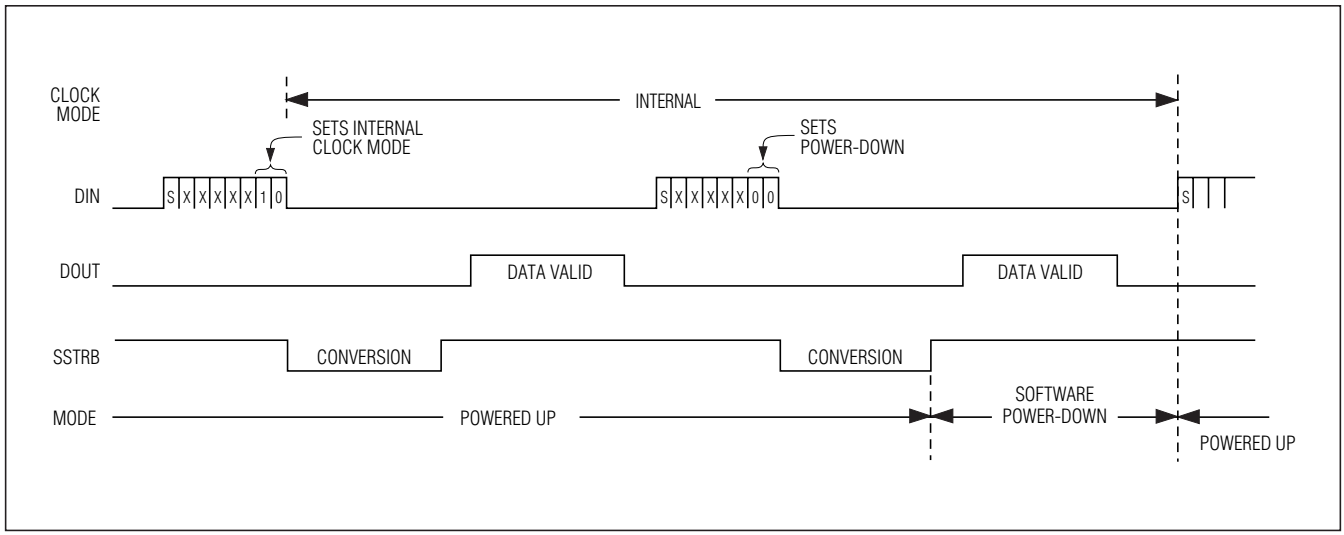


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Table 4. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
1	1	External Clock
1	0	Internal Clock
0	1	Unassigned
0	0	Power-Down

Table 5. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	INTERNAL CLOCK FREQUENCY
1	Enabled	225kHz
Floating	Enabled	1.5MHz
0	Power-Down	N/A

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Table 6. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF/2 + COM	COM	-VREF/2 + COM

also specify the clock mode. When software shutdown is asserted, the ADC continues to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results can be clocked out after the MAX1245 has entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit, and powers up the MAX1245. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Hardware Power-Down

Pulling SHDN low places the converter in hardware power-down. Unlike the software power-down mode, the conversion is not completed; it stops coincidentally with SHDN being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.5MHz. When returning to normal operation with SHDN floating, there is a t_{RC} delay of approximately $2M\Omega \times C_L$, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage.

External Reference

An external reference is required for the MAX1245. The reference voltage range is 1V to V_{DD}.

At VREF, the input impedance is a minimum of 18kΩ for DC currents. During a conversion, the reference must be able to deliver up to 250µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 0.1µF capacitor.

Transfer Function

Table 6 shows the full-scale voltage ranges for unipolar and bipolar modes using a 2.048V reference.

The external reference must have a temperature coefficient of 4ppm/°C or less to achieve accuracy to within 1LSB over the commercial temperature range of 0°C to +70°C.

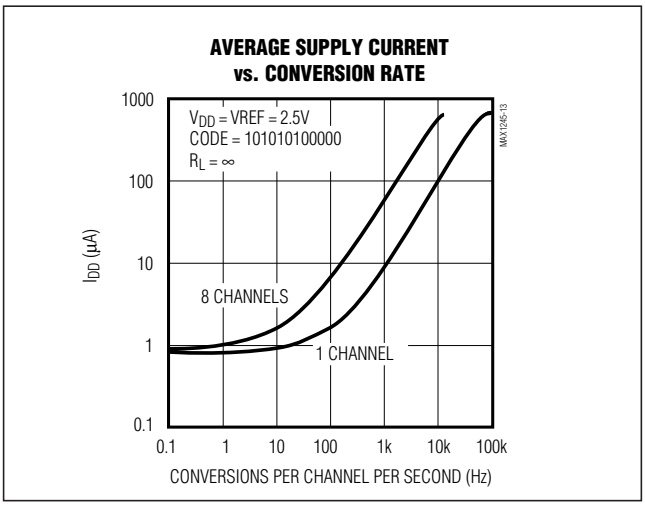


Figure 13. Average Supply Current vs. Conversion Rate

Figure 14 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 15 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 500µV (2.048V / 4096) for unipolar operation and 1LSB = 500µV [(2.048V / 2 - -2.048V / 2) / 4096] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 16 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star

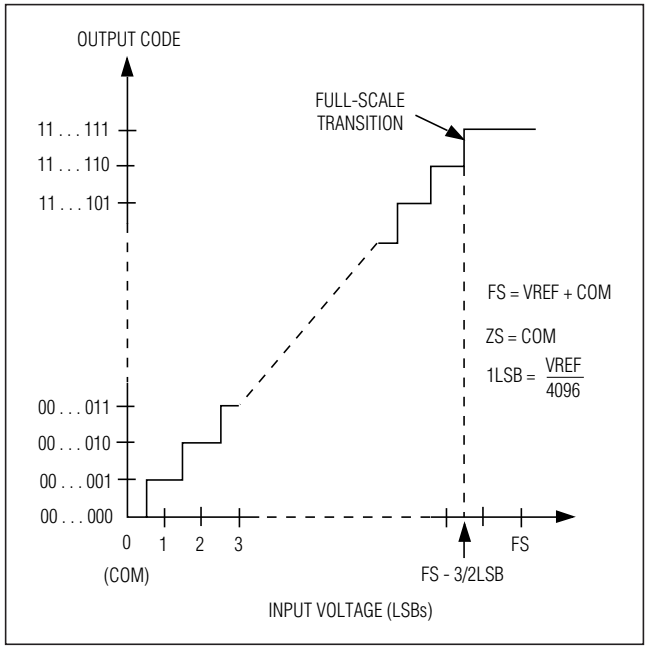


Figure 14. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

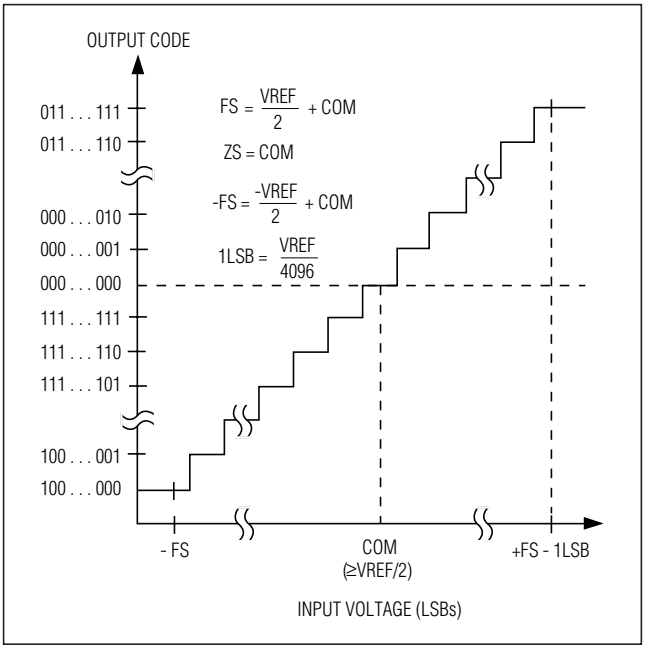


Figure 15. Bipolar Transfer Function, Full Scale (FS) = VREF / 2 + COM, Zero Scale (ZS) = COM

ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 4.7µF capacitors close to pin 20 of the MAX1245. Minimize capacitor lead lengths for best supply-noise rejection. If the +2.5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 16).

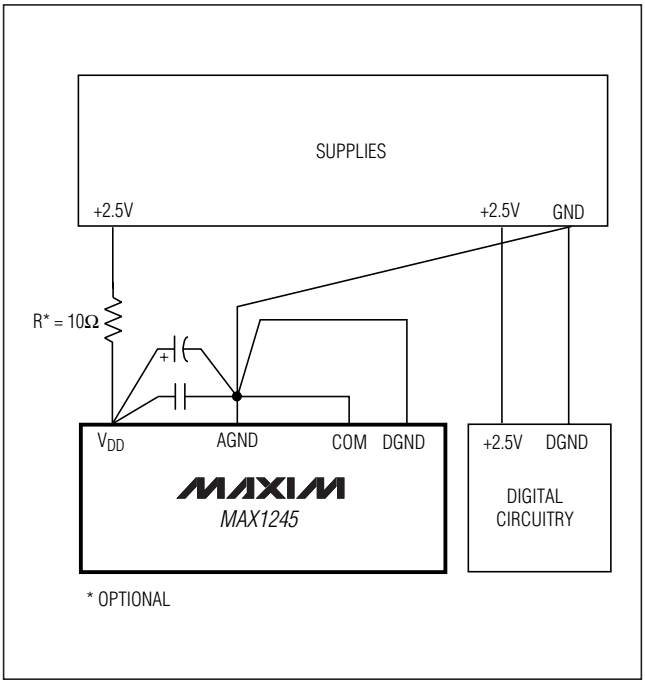


Figure 16. Power-Supply Grounding Connection

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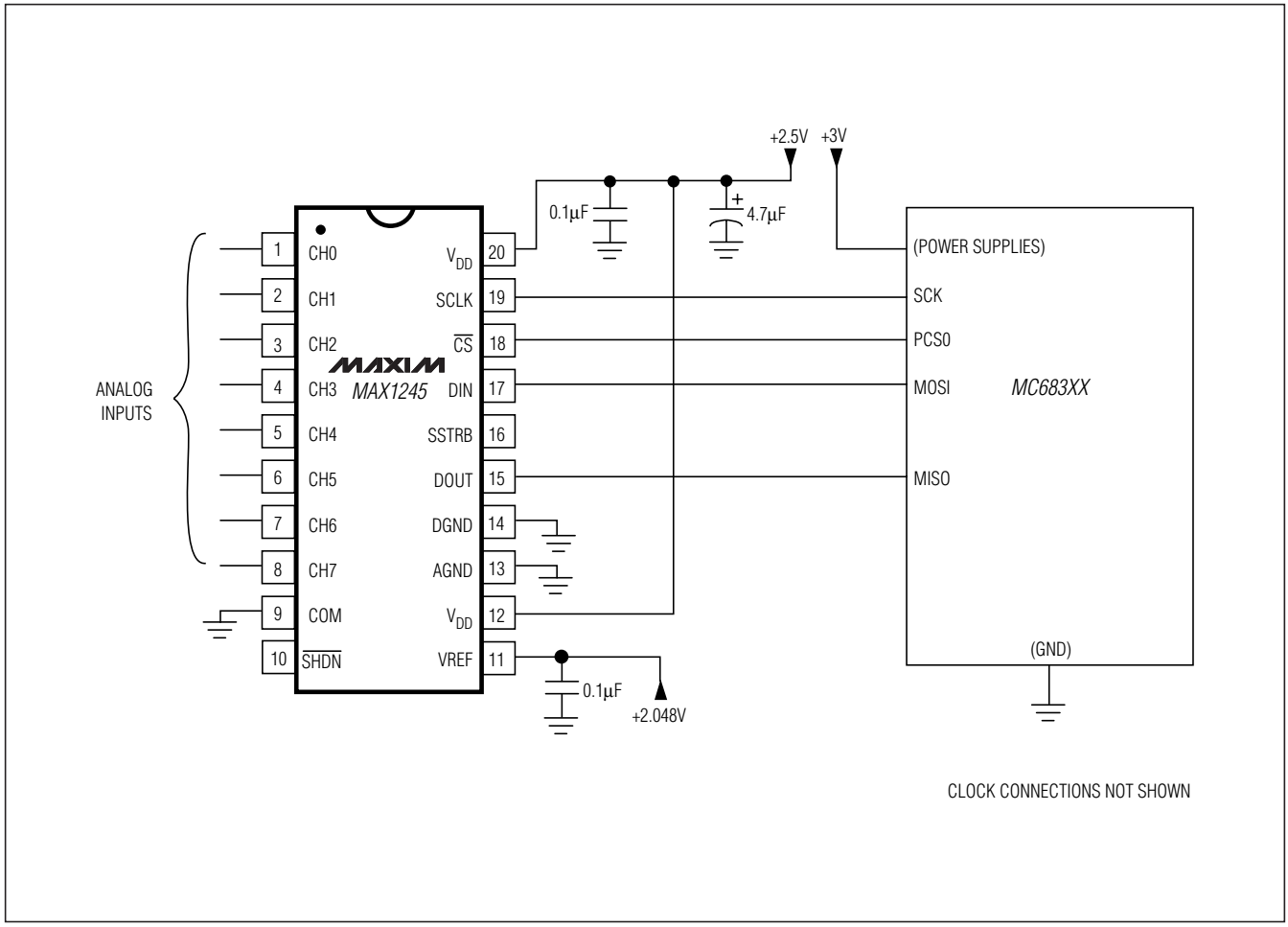


Figure 17. MAX1245 QSPI Connections

High-Speed Digital Interfacing with QSPI

The MAX1245 can interface with QSPI using the circuit in Figure 17 (f_{SCLK} = 1.5MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own micro-sequencer.

Because the maximum external clock frequency is 1.5MHz, the MAX1245 is QSPI compatible up to 1.5MHz.

TMS320LC3x-to-MAX1245 Interface

Figure 18 shows an application circuit to interface the MAX1245 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 19.

Use the following steps to initiate a conversion in the MAX1245 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX1245's SCLK input.
2) The MAX1245's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port, to enable data to be clocked into the MAX1245's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX1245 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1245's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1245.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1245 until the next conversion is initiated.

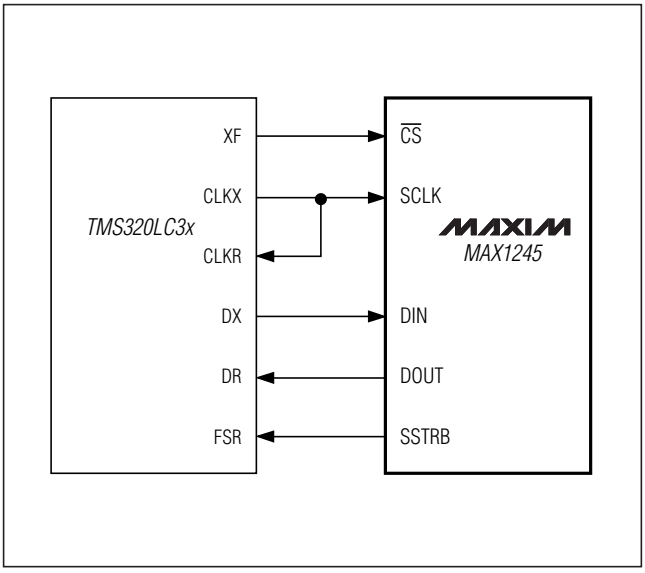


Figure 18. MAX1245-to-TMS320 Serial Interface

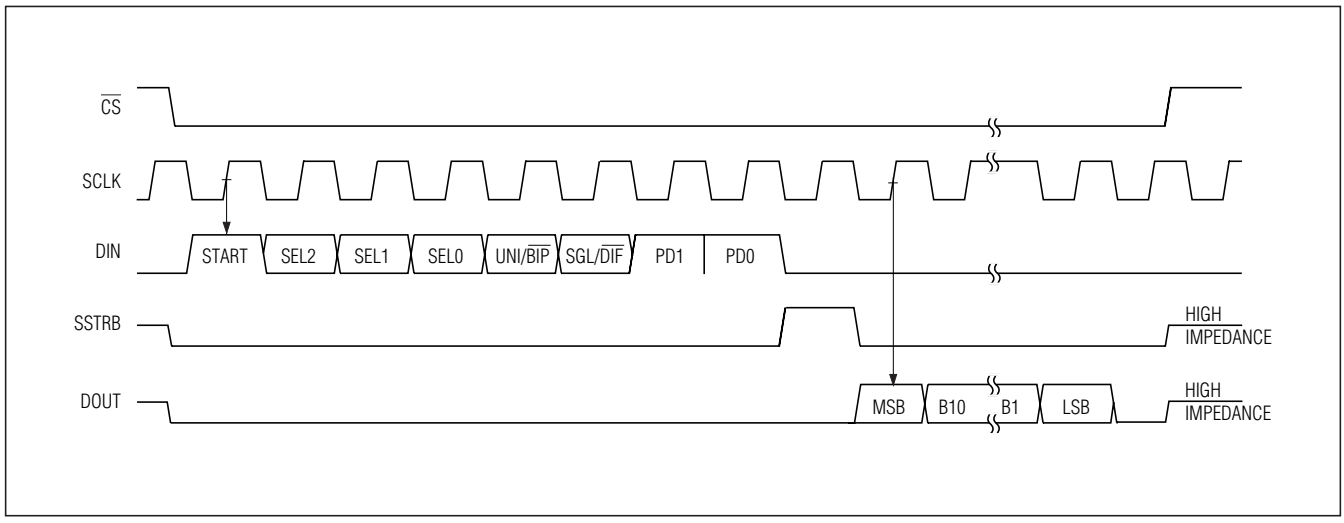


Figure 19. TMS320 Serial-Interface Timing Diagram

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Chip Information

TRANSISTOR COUNT: 2554

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 PDIP	A20-1	**21-0056**
20 SSOP	P20-4	**21-0043**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/96	Initial release.	—
1	11/09	Removed the dice package from the *Ordering Information* table.	1

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