OPAx317-Q1 Zerø-Drift, Low-Offset, Rail-to-Rail I/O Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification level C6
- Supply Voltage: 1.8 V to 5.5 V
- microPackages:
  - Single: SOT23-5
  - Dual: VSSOP-8
  - Quad: TSSOP-14
- Low Offset Voltage: 20 μV (Typical)
- CMRR: 108-dB (Typical) PSRR
- Quiescent Current: 35 μA (Maximum)
- Gain Bandwidth: 300 kHz
- Rail-to-Rail Input and Output
- Internal EMI and RFI Filtering

2 Applications

- HEV-EV power train
- Advanced driver assist (ADAS)
- Automatic climate control
- Low noise, low power circuits
- Avionics, landing gear
- Medical instrumentation
- Current sense

3 Description

The OPA317-Q1 series of CMOS operational amplifiers offer precision performance at a very competitive price. These devices are members of the Zerø-Drift family of amplifiers that use a proprietary autocalibration technique to simultaneously provide low offset voltage (90 μV maximum) and near-zero drift over time and temperature at only 35 μA (maximum) of quiescent current.

The OPA317-Q1 family features rail-to-rail input and output in addition to near flat 1/f noise, making this amplifier ideal for many applications, and much easier to design into a system. These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V).

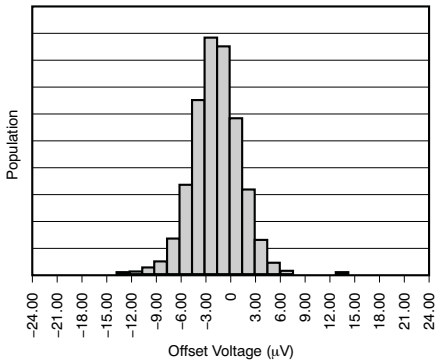
The OPA317-Q1 (single version) is available in the SOT23-5 package. The OPA2317-Q1 (dual version) is offered in the VSSOP-8 package. The OPA4317-Q1 is offered in the TSSOP-14 package. All versions are specified for operation from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA317-Q1	SOT-23 (5)	1.60 mm × 2.90 mm
OPA2317-Q1	VSSOP (8)	3.00 mm × 3.00 mm
OPA4317-Q1	TSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Distribution of Offset Voltage



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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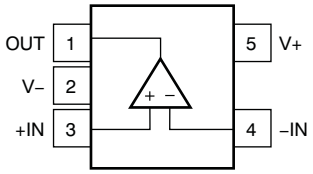
4 Revision History

DATE	REVISION	NOTES
July 2016	*	Initial release.

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5 Pin Configuration and Functions

OPA317-Q1: DBV Package
5-Pin SOT-23
Top View

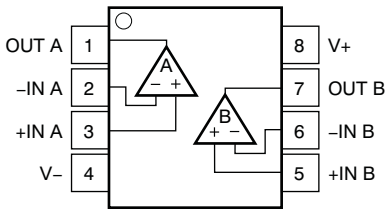


Pin Functions: OPA317-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	SOT-23		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output
V+	5	—	Positive (highest) power supply
V–	2	—	Negative (lowest) power supply

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OPA2317-Q1: DGK Package
8-Pin VSSOP
Top View

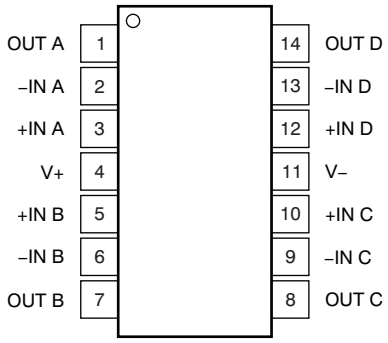


Pin Functions: OPA2317-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	VSSOP		
+IN A	3	I	Noninverting input, channel A
–IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

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OPA4317-Q1: SW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4317-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	TSSOP		
+IN A	3	I	Noninverting input, channel A
–IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN B	6	I	Inverting input, channel B
+IN C	10	I	Noninverting input, channel C
–IN C	9	I	Inverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
V_S = (V+) – (V–)	Supply voltage		7	V
	Signal input terminals (2)	(V–) – 0.3	(V+) + 0.3	V
	Signal input terminals(2)	–10	10	mA
	Output short circuit(3)	Continuous		
T_A	Operating temperature	–40	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±4000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
(V+ – V–)	Supply voltage	1.8 (±0.9)	5.5 (±2.25)	V
T_A	Specified temperature	–40	125	°C

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6.4 Thermal Information: OPA317-Q1

THERMAL METRIC(1)		OPA317-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2317-Q1

THERMAL METRIC(1)		OPA2317-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4317-Q1

THERMAL METRIC(1)		OPA4317-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.7 Electrical Characteristics: V_S = 1.8 V to 5.5 V

At T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		20	±90	µV
		T_A = –40°C to +125°C, V_S = 5 V			±100	
dV_{OS}/dT	Input offset voltage vs temperature	T_A = –40°C to +125°C		0.05		µV/°C
PSRR	Input offset voltage vs power supply	T_A = –40°C to +125°C, V_S = 1.8 V to 5.5 V		1	10	µV/V
	Long-term stability(1)			See (1)		
	Channel separation, DC			5		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±275		pA
		OPA4317-Q1		±155		
		T_A = –40°C to +125°C		±300		
I_{OS}	Input offset current			±400		pA
		OPA4317-Q1		±140		
NOISE						
e_n	Input voltage noise density	f = 1 kHz		55		nV/√Hz
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		μV_{PP}
		f = 0.1 Hz to 10 Hz		1.1		
i_n	Input current noise	f = 10 Hz		100		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	T_A = –40°C to +125°C (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	95	108		dB
		OPA4317 T_A = –40°C to +125°C (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, V_S = 5.5 V	95	108		
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	T_A = –40°C to +125°C, R_L = 10 kΩ (V–) + 100 mV < V_O < (V+) – 100 mV	100	110		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		300		kHz
SR	Slew rate	G = 1		0.15		V/µs
OUTPUT						
	Voltage output swing from rail	T_A = –40°C to +125°C		30	100	mV
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive		See the *Typical Characteristics* section			
	Open-loop output impedance	f = 350 kHz, I_O = 0		2		kΩ
POWER SUPPLY						
V_S	Specified voltage		1.8		5.5	V
I_Q	Quiescent current per amplifier	T_A = –40°C to +125°C, I_O = 0		21	35	µA
	Turnon time	V_S = 5 V		100		µs

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

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6.8 Typical Characteristics

At T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

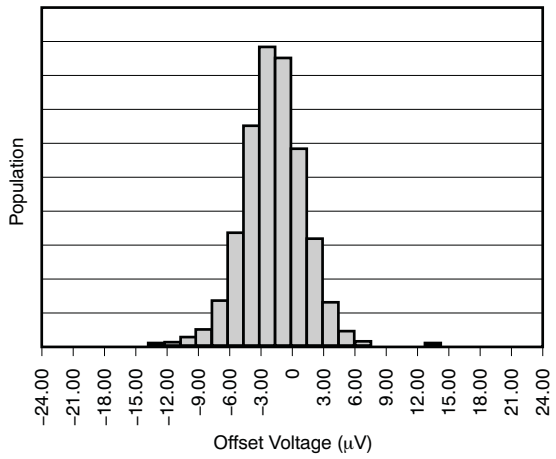


Figure 1. Offset Voltage Production Distribution

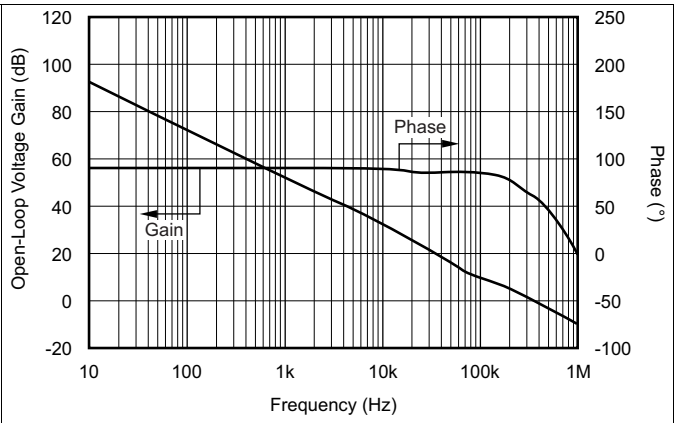


Figure 2. Open-Loop Gain vs Frequency

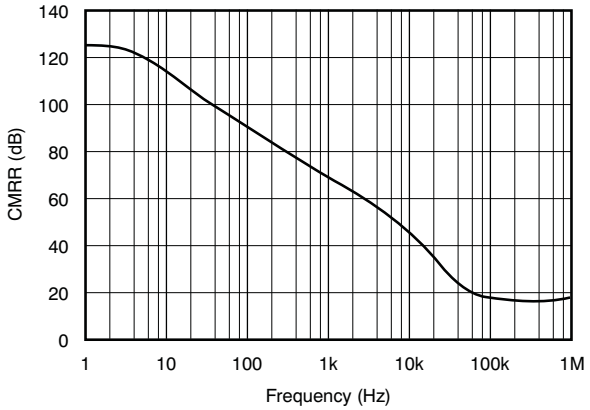


Figure 3. Common-Mode Rejection Ratio vs Frequency

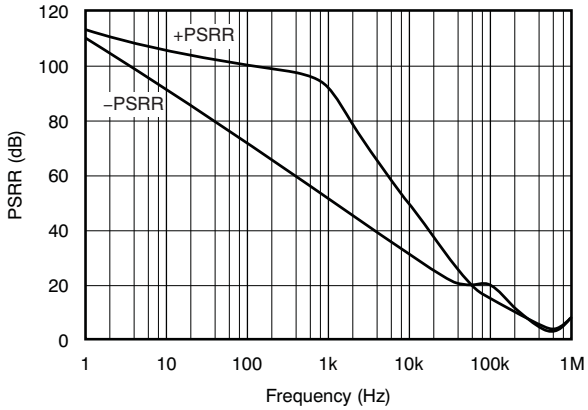


Figure 4. Power-Supply Rejection Ratio vs Frequency

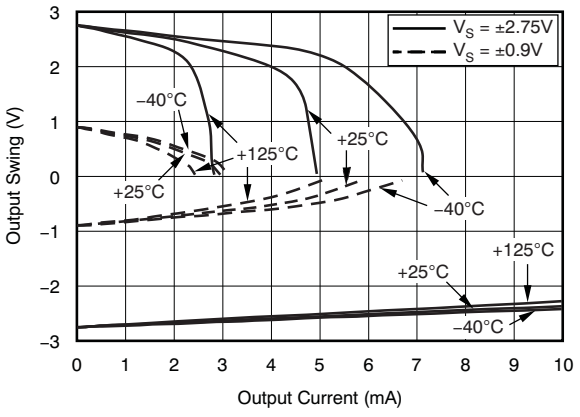


Figure 5. Output Voltage Swing vs Output Current

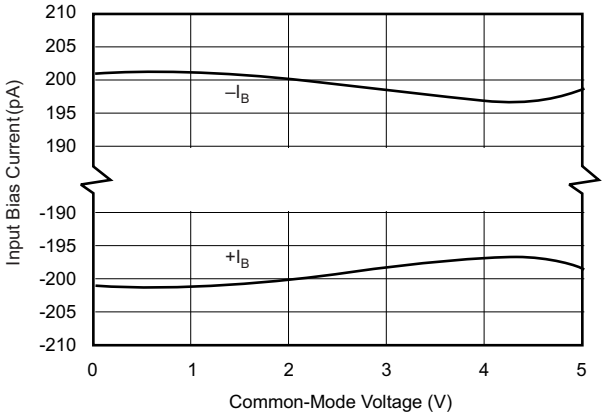


Figure 6. Input Bias Current vs Common-Mode Voltage

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Typical Characteristics (continued)

At T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

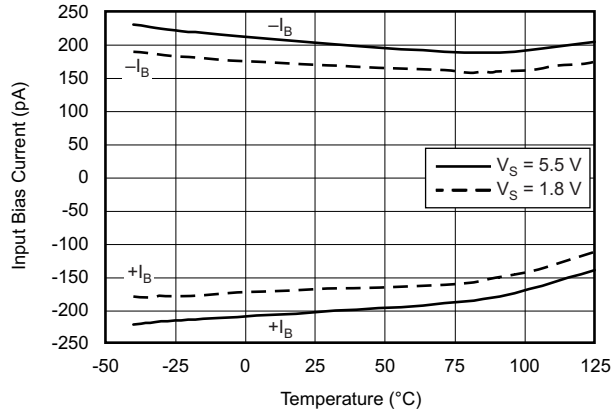


Figure 7. Input Bias Current vs Temperature

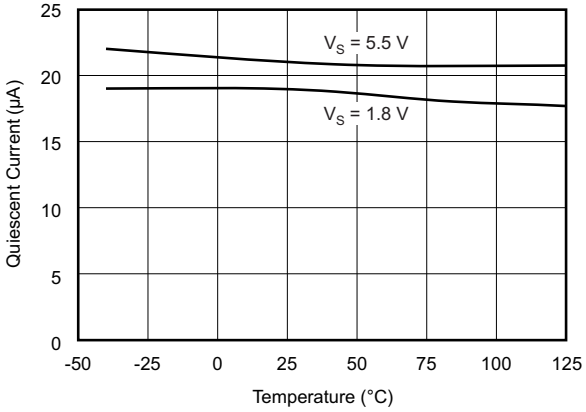
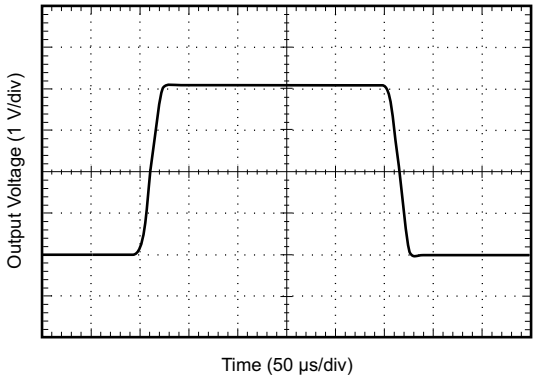
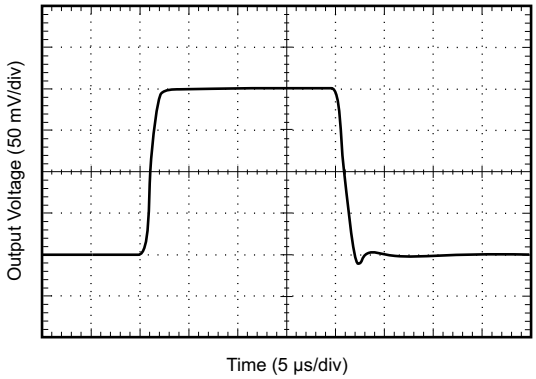


Figure 8. Quiescent Current vs Temperature



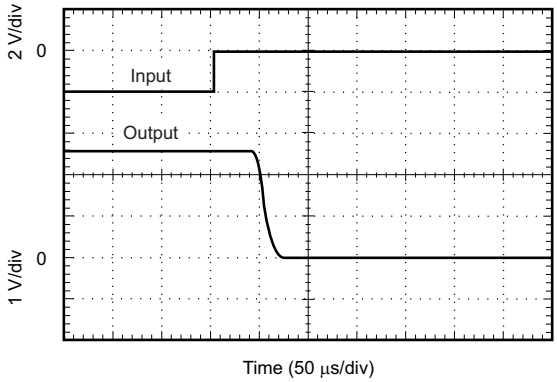
G = 1 R_L = 10 kΩ

Figure 9. Large-Signal Step Response



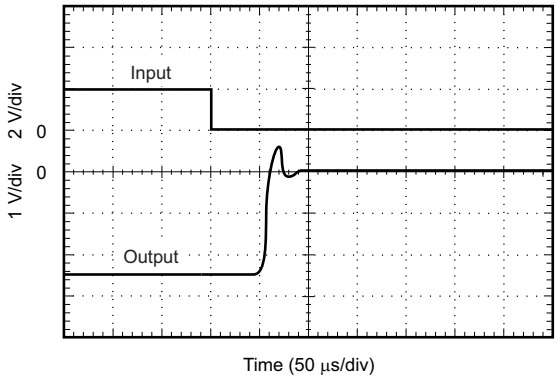
G = 1 R_L = 10 kΩ

Figure 10. Small-Signal Step Response



See Figure 18

Figure 11. Positive Overvoltage Recovery



See Figure 18

Figure 12. Negative Overvoltage Recovery

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Typical Characteristics (continued)

At T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

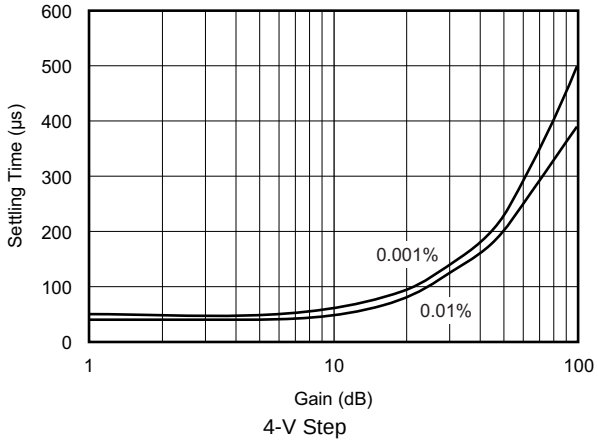


Figure 13. Settling Time vs Closed-Loop Gain

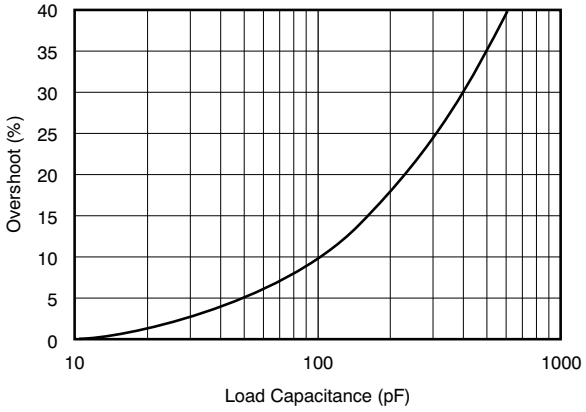


Figure 14. Small-Signal Overshoot vs Load Capacitance

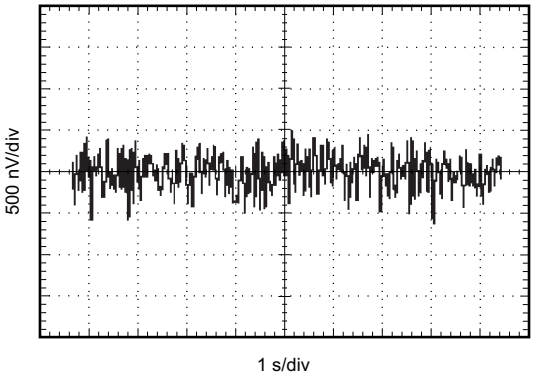


Figure 15. 0.1-Hz to 10-Hz Noise

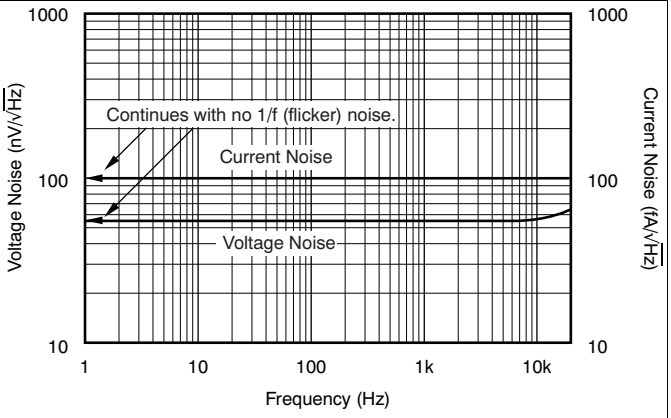
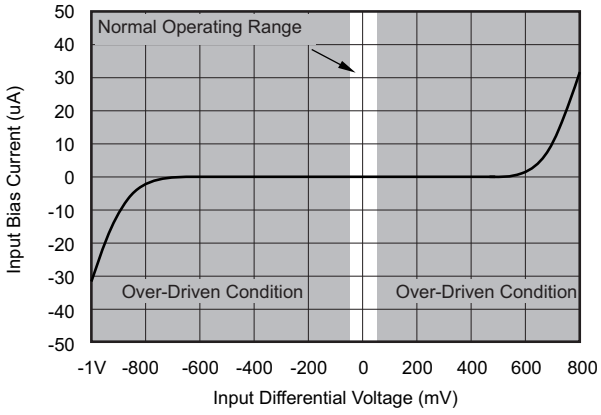


Figure 16. Current and Voltage Noise Spectral Density vs Frequency



See the *Input Differential Voltage* section

Figure 17. Input Bias Current vs Input Differential Voltage

7 Parameter Measurement Information

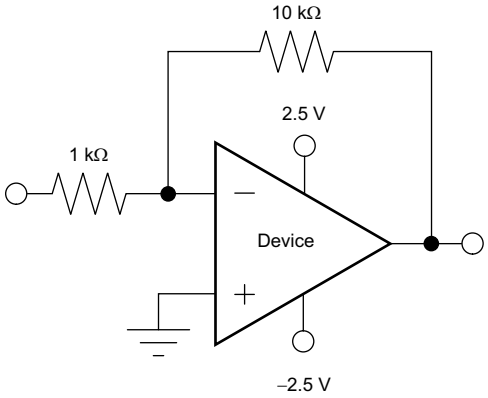


Figure 18. Overvoltage Recovery Circuit

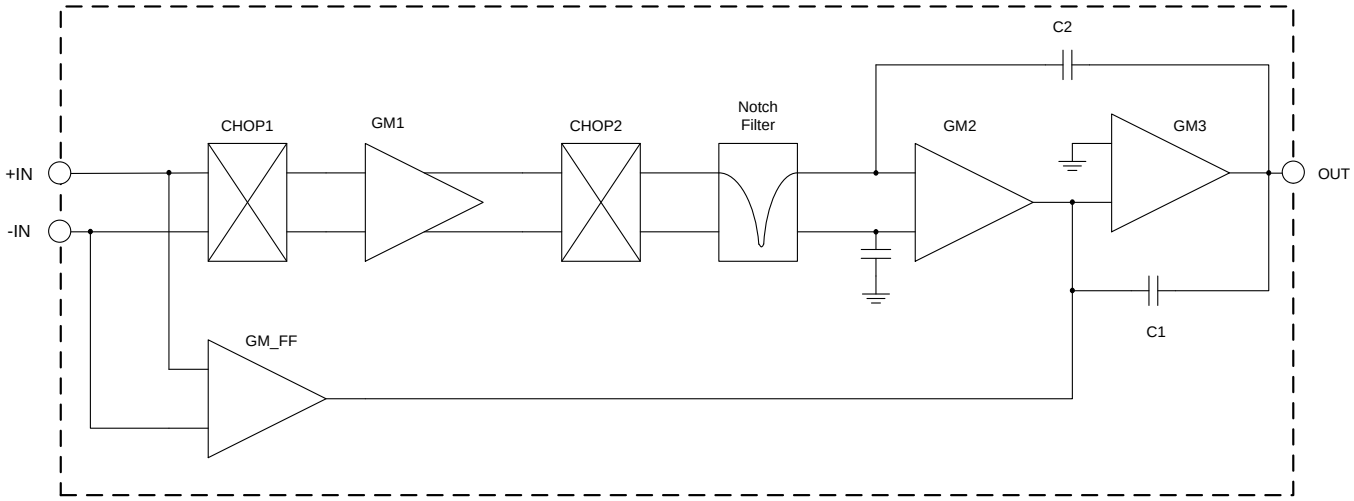
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8 Detailed Description

8.1 Overview

The OPA317-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the OPA317 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Operating Voltage

The OPA317-Q1 series of operational amplifiers can be used with single or dual supplies from an operating range of V_S = 1.8 V (±0.9 V) up to 5.5 V (±2.75 V).

CAUTION

Supply voltages greater than 7 V can permanently damage the device.

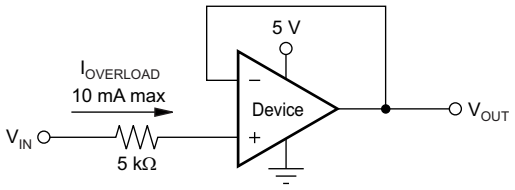
See the *Absolute Maximum Ratings* table. Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics* section.

Feature Description (continued)

8.3.2 Input Voltage

The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA317-Q1 device is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is about 200 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 19.



NOTE: Current limiting resistor required if input voltage exceeds supply rails by ≥ 0.3 V.

Figure 19. Input Current Protection

8.3.3 Input Differential Voltage

The typical input bias current of the OPA317-Q1 during normal operation is approximately 200 pA. In overdriven conditions, the bias current can increase significantly (see Figure 17).The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied, and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 20.

NOTE

The input bias current remains within specification within the linear region.

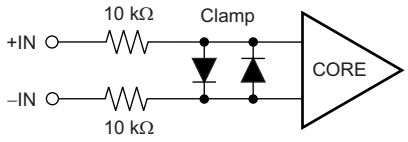


Figure 20. Equivalent Input Circuit

8.3.4 Internal Offset Correction

The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 operational amplifiers use an auto-calibration technique with a time-continuous, 125-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

8.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from its nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA317-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 8 MHz (–3 dB), with a roll-off of 20 dB per decade.

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8.4 Device Functional Modes

The OPAx317-Q1 family of devices are powered on when the supply is connected. The device can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. Proprietary Zerø-Drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPA317-Q1 family is optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high impedance inputs that have a common-mode range 100 mV beyond the supplies, and a rail-to-rail output that swings within 100 mV of the supplies under normal test conditions. The OPA317-Q1 series are precision amplifiers for cost-sensitive applications.

9.1.1 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply operational amplifiers, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply operational amplifier. A good single-supply operational amplifier may swing close to single-supply ground, but does not reach ground. The output of the OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative power supply than the operational amplifier negative supply. A pulldown resistor can be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 21.

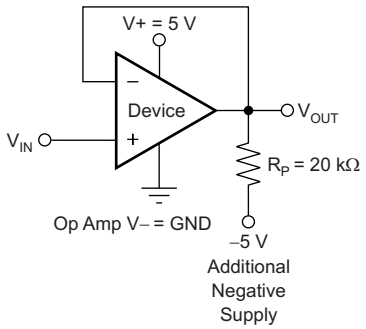


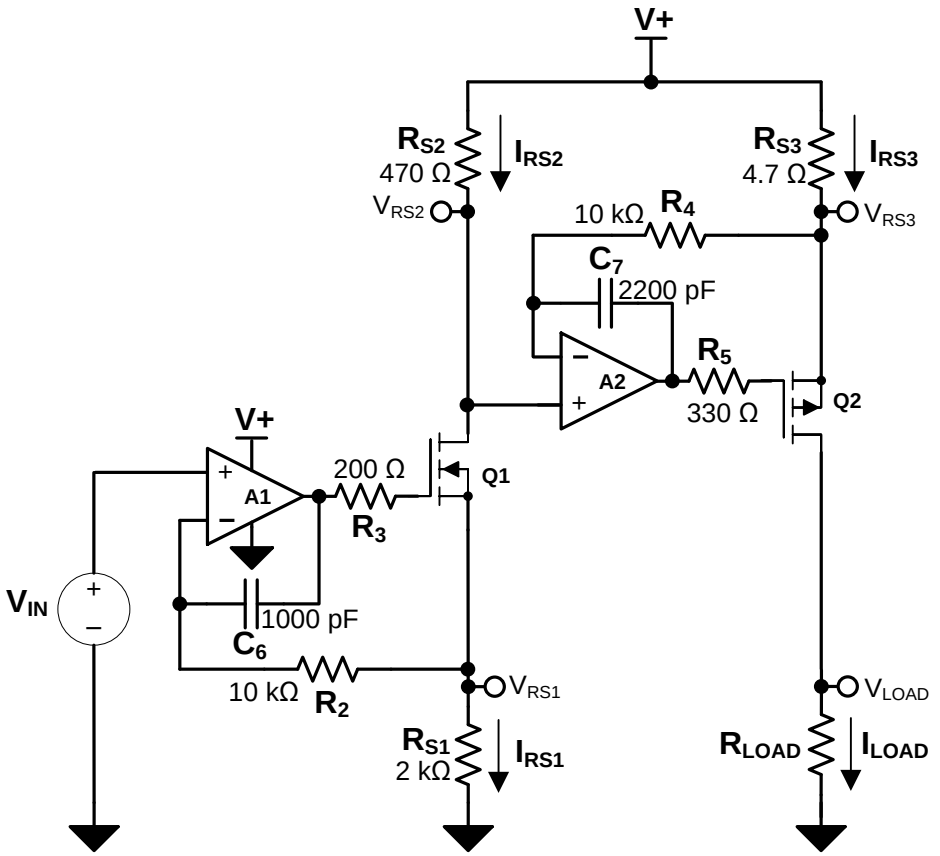
Figure 21. For V_{OUT} Range to Ground

The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 have been characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ. This configuration increases the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns as the output drives back up above –2 mV. Lowering the resistance of the pulldown resistor allows the operational amplifier to swing even further below the negative rail. Use resistances as low as 10 kΩ to achieve excellent accuracy down to –10 mV.

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9.2 Typical Applications

The circuit shown in Figure 22 is a high-side voltage-to-current (V-I) converter. It translates an input voltage of 0 V to 2 V to an output current of 0 mA to 100 mA. Figure 23 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA317 facilitate excellent DC accuracy for the circuit.



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Figure 22. High-Side Voltage-to-Current (V-I) Converter

9.2.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5-V DC
- Input: 0-V to 2-V DC
- Output: 0-mA to 100-mA DC

9.2.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current-sensing resistors: R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

Typical Applications (continued)

For a successful design, pay close attention to the DC characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2317 CMOS operational amplifier is a high-precision, 5-µV offset, 0.05-µV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 50 mV of the positive rail. The OPA2317 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise DC control. The rail-to-rail output stage of the OPA2317 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

9.2.3 Application Curve

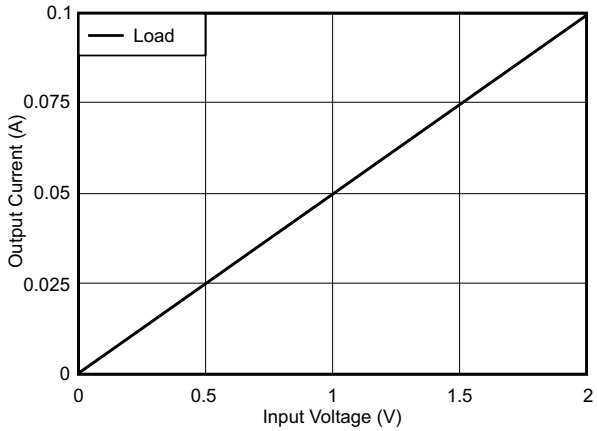
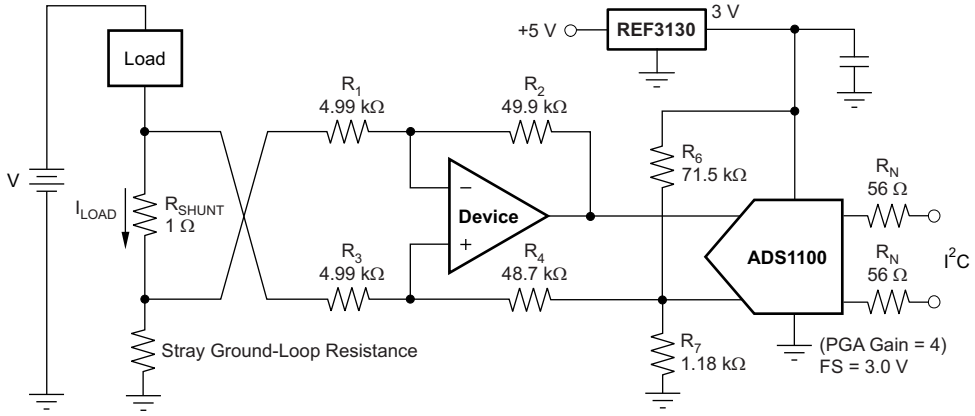


Figure 23. Measured Transfer Function for High-Side V-I Converter

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9.3 System Example

R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. The ADS1100 device is a 16-bit converter; therefore, a precise reference is essential for maximum accuracy. If absolute accuracy is not required and the 5-V power supply is sufficiently stable, the REF3130 device may be omitted.



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NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 24. Low-Side Current Monitor

10 Power Supply Recommendations

The OPAx317-Q1 device is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Electrical Characteristics: V_S = 1.8 V to 5.5 V* table presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*) table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

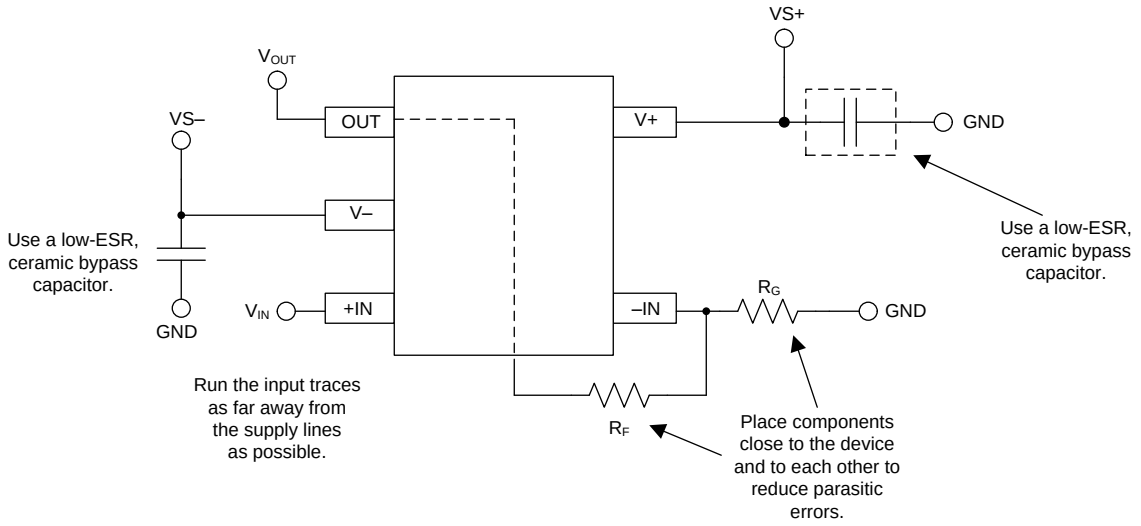
Attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Optimize circuit layout and mechanical conditions for lowest offset voltage and precision performance. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 μV/°C or higher, depending on the materials used.

11.2 Layout Example



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Figure 25. OPAx317-Q1 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Self-Calibrating, 16-Bit Analog-to-Digital Converter*,
- *15ppm/°C Max, 100μA, SOT23-3 Series Voltage Reference*,

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Related Links

lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA317-Q1	Click here	Click here	Click here	Click here	Click here
OPA2317-Q1	Click here	Click here	Click here	Click here	Click here
OPA4317-Q1	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2317QDGKRQ1	PREVIEW	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2317	
OPA317QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	317Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA2317-Q1, OPA317-Q1 :

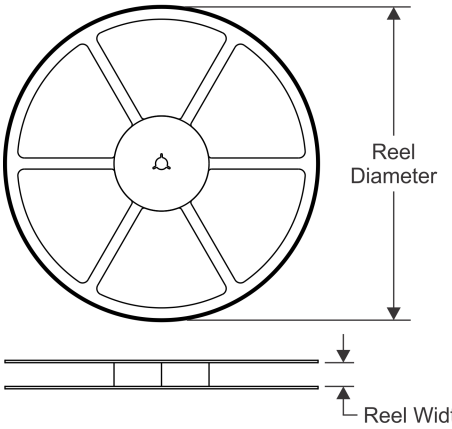
- Catalog: OPA2317, OPA317

NOTE: Qualified Version Definitions:

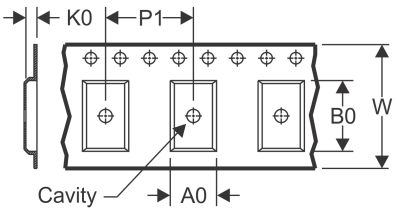
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

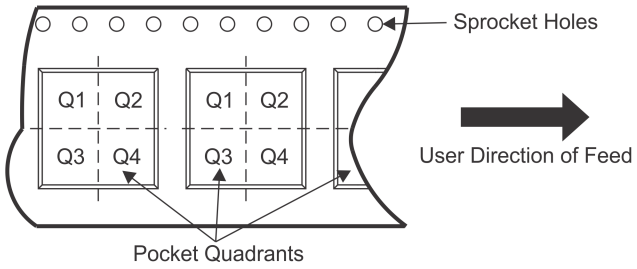


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

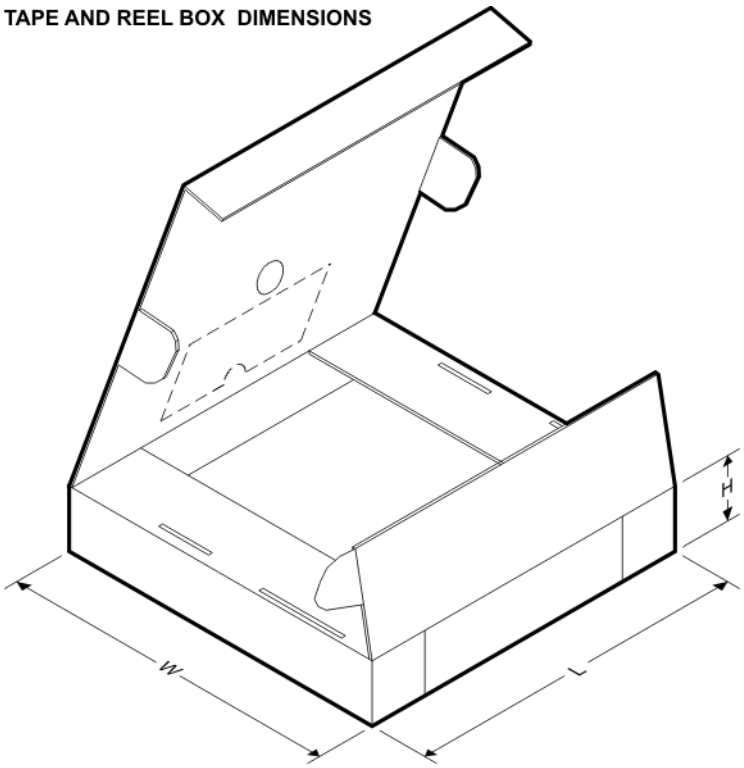
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2317QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA317QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

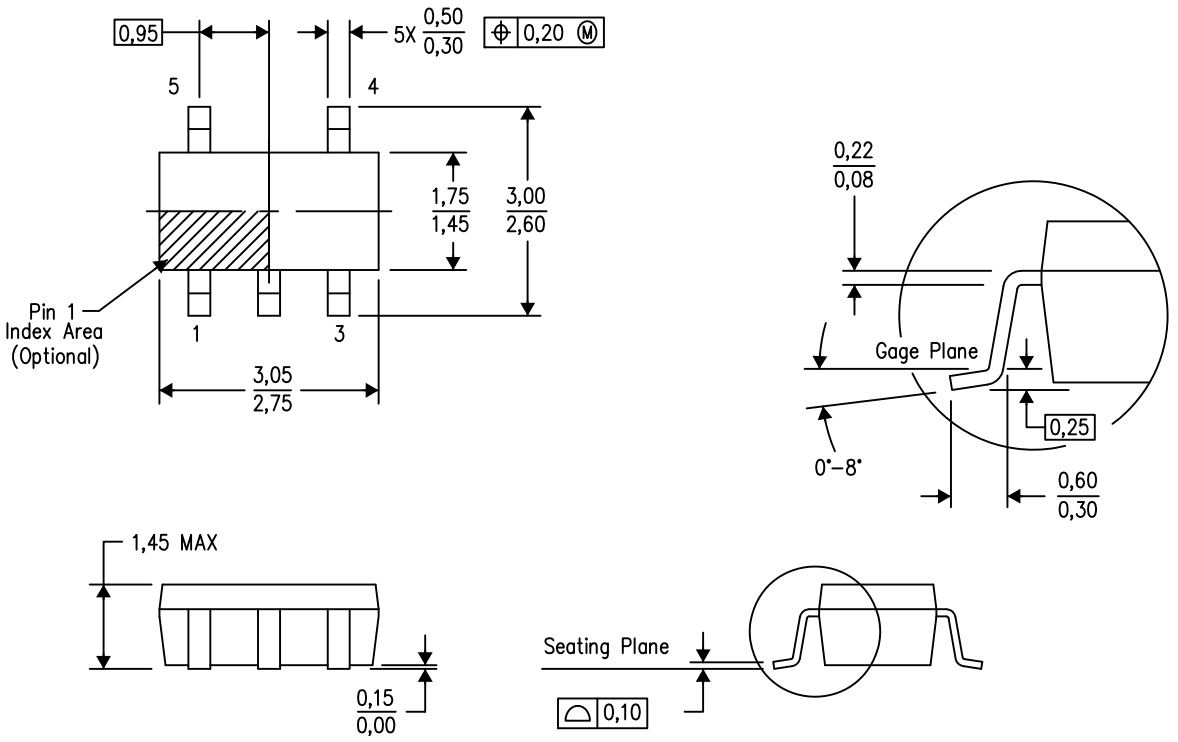
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2317QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA317QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0

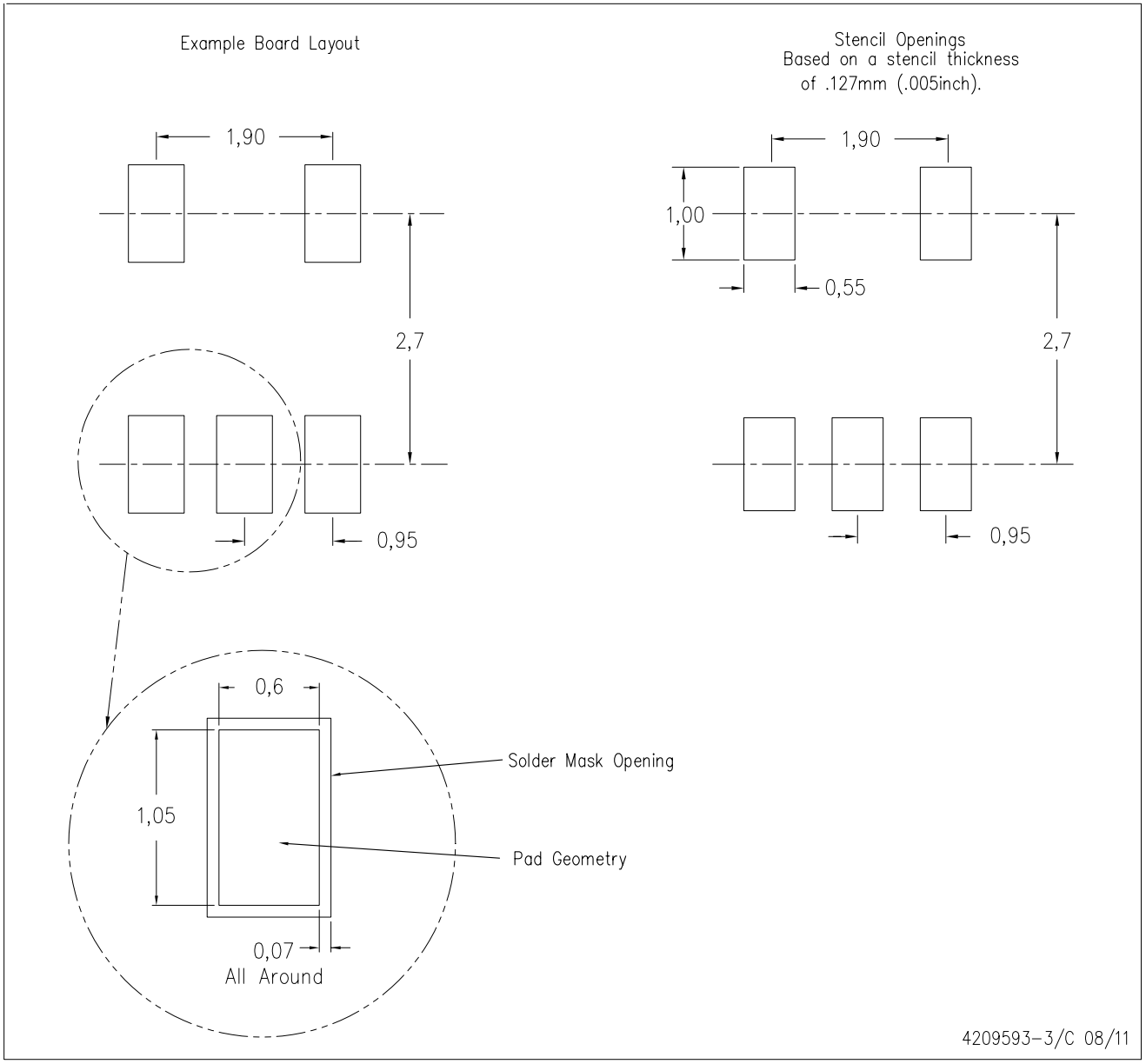
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

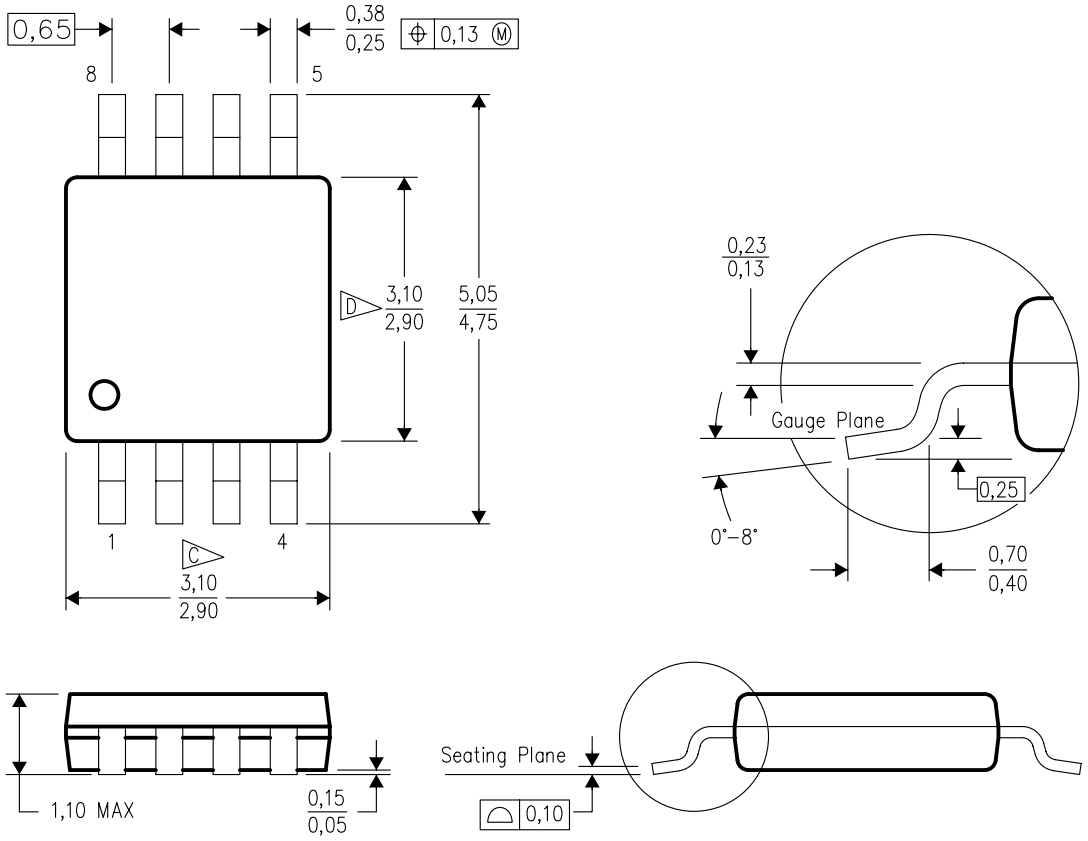
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

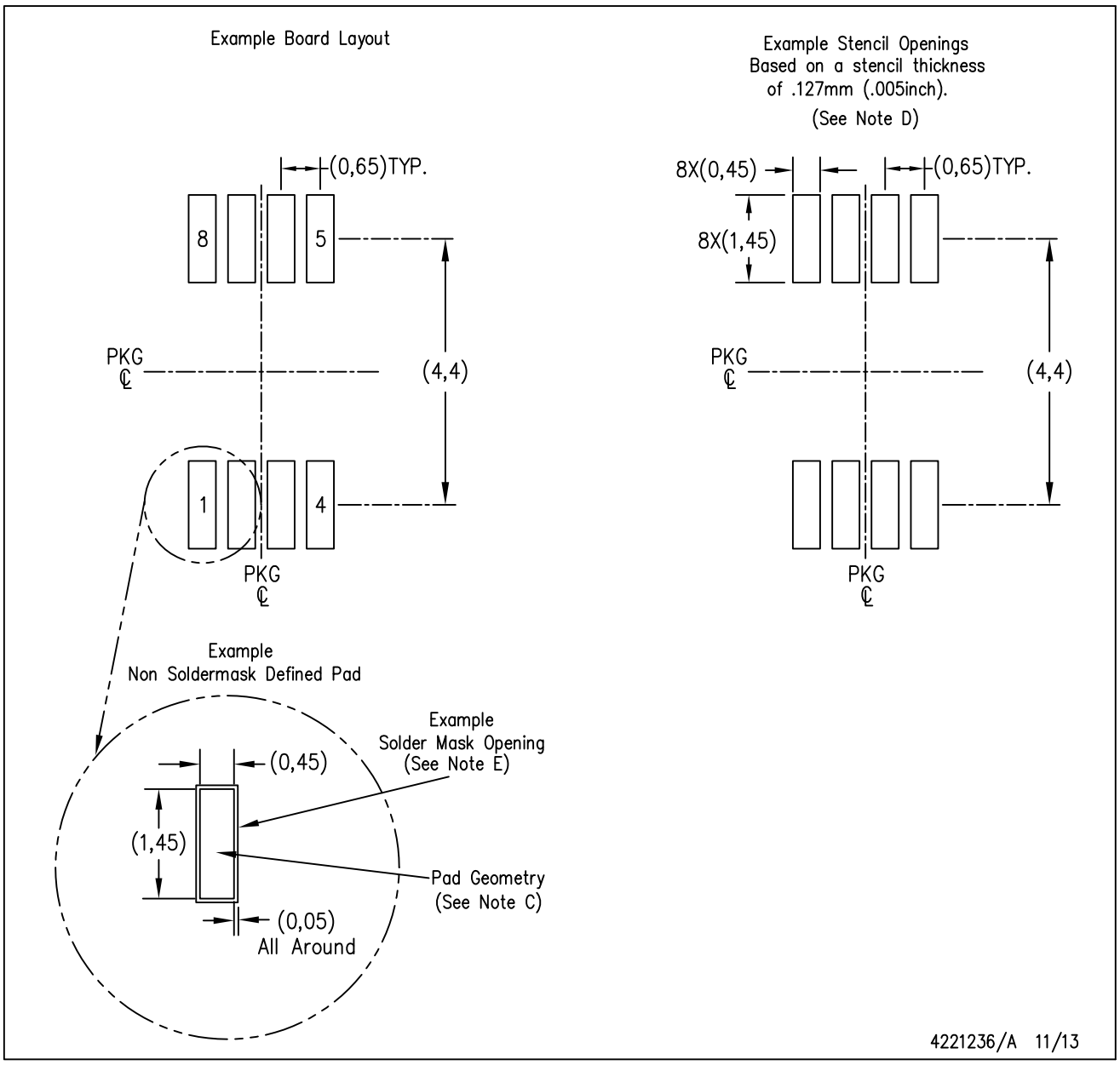
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
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