ICS673-01
PLL Building Block

Description

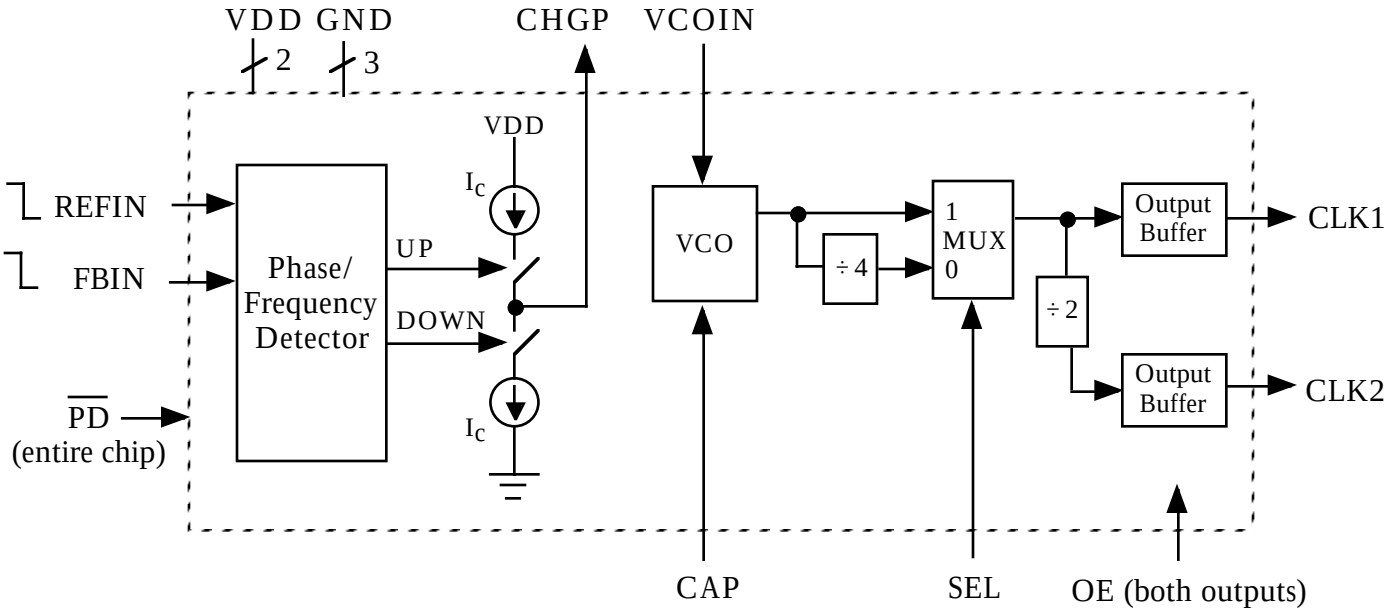
The ICS673-01 is a low cost, high performance Phase Locked Loop (PLL) designed for clock synthesis and synchronization. Included on the chip are the phase detector, charge pump, Voltage Controlled Oscillator (VCO), and two output buffers. One output buffer is a divide by two of the other. Through the use of external reference and VCO dividers (easily implemented with the ICS674-01), the user can easily customize the clock to lock to a wide variety of input frequencies.

Included on the ICS673-01 are an Output Enable function that puts both outputs into a high-impedance state, as well as a Power Down feature that turns off the entire device.

Features

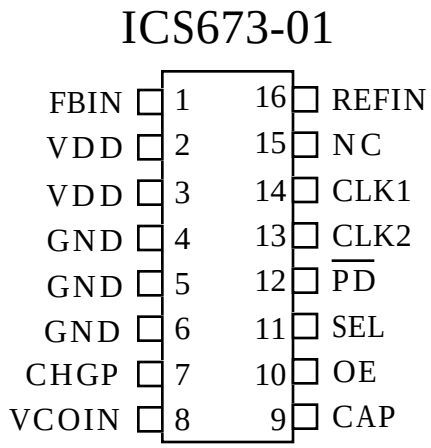
- Packaged in 16 pin narrow SOIC
- Access to VCO input and feedback paths of PLL
- VCO operating range up to 135 MHz (5V)
- Able to lock MHz range outputs to kHz range inputs through use of external dividers
- Output Enable tri-states outputs
- Low skew output clocks
- Power Down turns off chip
- VCO predivide of 1 or 4
- 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- +3.3 V ±5% or +5 V ±10% operating voltage
- Industrial Temperature range available
- With the ICS674-01, forms a complete PLL

Block Diagram



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Pin Assignment



16 pin narrow (150 mil) SOIC

VCO Predivide Select Table

SEL	VCO Predivide
0	4
1	1

0 = connect pin directly to ground
1 = connect pin directly to VDD

Pin Descriptions

Number	Name	Type	Description
1	FBIN	CI	FeedBack INput. Connect feedback clock to this pin. Falling edge triggered.
2	VDD	P	VDD. Connect to +3.3 V or +5 V, and to VDD on pin 3.
3	VDD	P	VDD. Connect to VDD on pin 2.
4	GND	P	Connect to ground.
5	GND	P	Connect to ground.
6	GND	P	Connect to ground.
7	CHGP	O	CHarGe Pump output. Connect to VCOIN under normal operation.
8	VCOIN	I	Input to internal VCO.
9	CAP	I	Loop filter return.
10	OE	I	Output Enable. Active high. Tri-states both outputs when low.
11	SEL	I	SELect pin for VCO pre-divide per table above.
12	$\overline{PD}$	I	Power Down. Turns off entire chip when this pin is low. Outputs stop low.
13	CLK2	O	CLocK output 2. This is a low-skew divide by two version of CLK1.
14	CLK1	O	CLocK output 1.
15	NC	-	No Connect. Nothing is connected internally to this pin.
16	REFIN	CI	REFerence INput. Connect reference clock to this pin. Falling edge triggered.

Key: CI = clock input, I = Input, O = output, P = power supply connection

Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature	ICS673M-01	0		70	°C
	ICS673M-01I	-40		85	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0 V unless noted)					
Operating Voltage, VDD		3.13		5.50	V
Input High Voltage	All except VCOIN	2			V
Input Low Voltage	All except VCOIN			0.8	V
Input High Voltage	VCOIN			VDD	V
Input Low Voltage	VCOIN	0			V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load,CLK1=40MHz		15		mA
Power Down Supply Current, IDDPD	No Load		6		µA
Short Circuit Current	Each output		±100		mA
Input Capacitance	OE, $\overline{PD}$, SEL		5		pF
AC CHARACTERISTICS (VDD = 5.0 V unless noted)					
Output Clock Frequency (4.5 to 5.5 V)	CLK1 with SEL=1	2		135	MHz
Output Clock Frequency (3.13 to 3.46 V)	CLK1 with SEL=1	2		100	MHz
CLK1 and CLK2 skew	Rising edges at VDD/2			500	ps
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	45	50	55	%
VCO Gain, Kv			95		MHz/V
Charge Pump Current, Ic			2.4		µA

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

External Components

The ICS673 requires a minimum number of external components for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD and GND as close to the ICS673 as possible. A series termination resistor of 33 Ω may be used for each clock output. Two ceramic capacitors and a resistor are needed for the external loop filter; calculations to determine the proper values are shown on the following pages. The capacitors must have very low leakage, therefore high quality ceramic capacitors are recommended. DO NOT use any type of polarized or electrolytic capacitor. Ceramic capacitors should have C0G or NP0 dielectric. Avoid high-K dielectrics like Z5U and X7R; these and other ceramics which have piezoelectric properties allow mechanical vibration in the system to increase the output jitter because the mechanical energy is converted directly to voltage noise on the VCO input.

Explanation of Operation

The ICS673 is a PLL building block circuit that includes an integrated VCO with a wide operating range. While it can easily lock MHz frequencies to other MHz frequencies, it is especially designed for starting with a kHz frequency and generating a frequency-locked MHz clock. Refer to Figure 1 below and to the Block Diagram on page 1.

The phase/frequency detector compares the falling edges of the clocks connected to FBIN and REFIN. It then generates an error signal to the charge pump, which produces a charge proportional to this error. The external loop filter integrates this charge, producing a voltage that then controls the frequency of the VCO. This process continues until the edges of FBIN are aligned with the edges of the REFIN clock, at which point the output frequency will be locked to the input frequency.

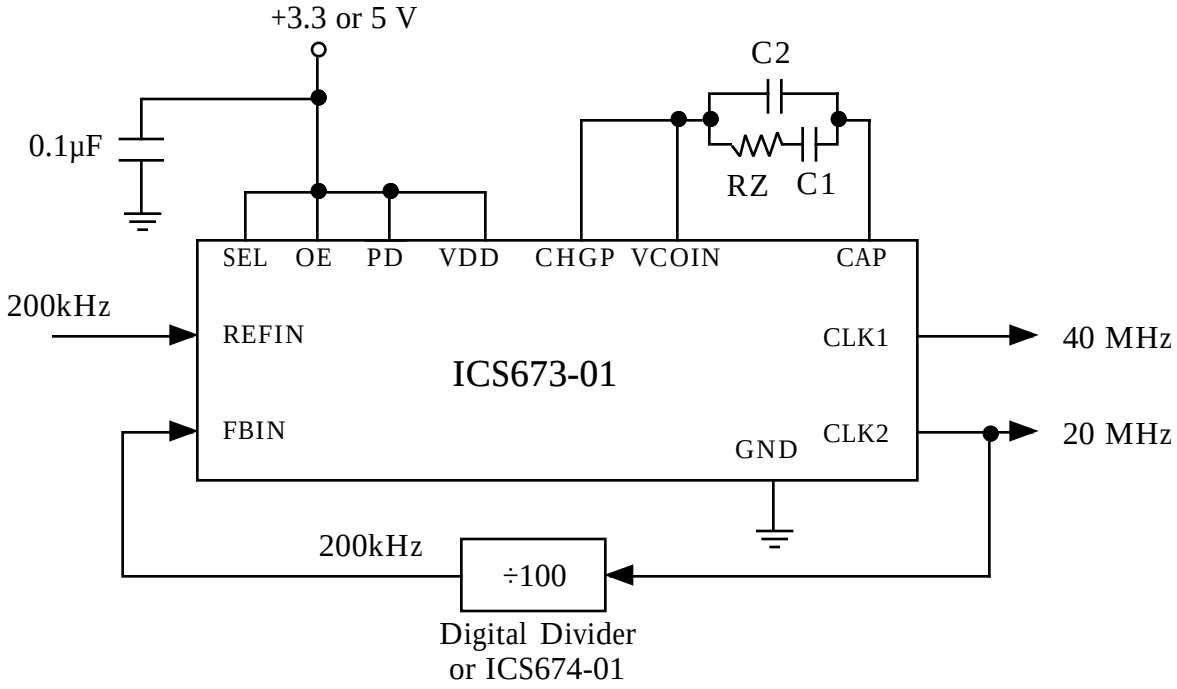


Figure 1. Typical Configuration; Generating 40 MHz from 200 kHz

Determining the Loop Filter Values

The loop filter components consist of C1, C2, and RZ. Calculating these values is best illustrated by an example. Using the example in Figure 1, we can synthesize 40 MHz from a 200 kHz input.

The phase locked loop may be approximately described by the following equations:

Natural frequency, $\omega_n = \sqrt{\frac{Kv \bullet Ic}{N \bullet C1}}$ Equation 1

Damping factor, $\zeta = \frac{Rz}{2}\sqrt{\frac{Kv \bullet Ic \bullet C1}{N}}$ Equation 2

where Kv = VCO gain (MHz/Volt)
Ic = Charge pump current (µA)
N = Total feedback divide
$C1$ = Loop filter capacitor (Farads)
Rz = Loop filter resistor (Ohms)

The natural frequency, ω_n, is approximately equal to the bandwidth (in radians/sec). As a general rule, the bandwidth should be at least 10 times less than the reference frequency, i.e.,

$\omega_n \approx 2\pi \bullet BW \leq REFIN/10$.

In this example, BW = REFIN/20, giving a bandwidth of 10 kHz.

Using the first equation, C1 can be determined since all other variables are known. In the example of Figure 1, N = 200, comprising a divide-by-2 on the chip and the external divide-by-100. Therefore, Equation 1 becomes

$$2\pi \bullet 10{,}000 = \sqrt{\frac{95 \bullet 2.4}{200 \bullet C1}}$$

and $C1$ = 289 pF (270 pF nearest std. value).

Choosing a damping factor of 0.7, Equation 2 becomes

$$0.7 = \frac{Rz}{2}\sqrt{\frac{95 \bullet 2.4 \bullet 270 \bullet 10E-12}{200}}$$

and Rz = 79.8 kΩ (82 kΩ nearest std. value).

The capacitor $C2$ is used to damp transients from the charge pump and should be at least 20 times smaller than $C1$, i.e.,

$C2 \leq C1/20$.

Therefore, $C2$ = 13.5 pF (13 pF nearest std. value).

To summarize, to generate 40 MHz from 200 kHz with standard values, the loop filter components are:

$C1$ = 270 pF
$C2$ = 13 pF
Rz = 82 kΩ

In general, making $C1$ larger may give improved loop performance, since it both lowers the bandwidth and increases the damping factor. However, it also increases the time for the loop to lock since the charge pump current has to charge a larger capacitance.

When choosing either CLK1 or CLK2 to drive the feedback divider, CLK2 should be used whenever possible. See the following section, “Avoiding PLL Lockup”, for additional explanations.

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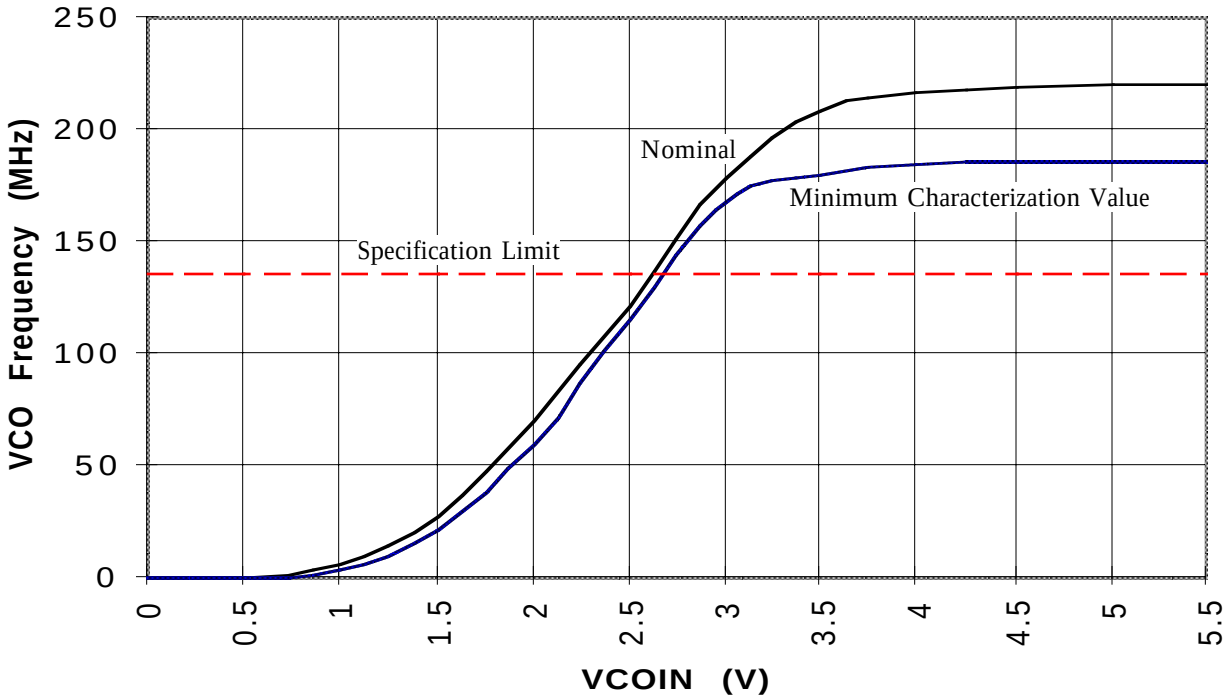


Figure 2. VCO Frequency vs Input Voltage at VDD = 5 V.

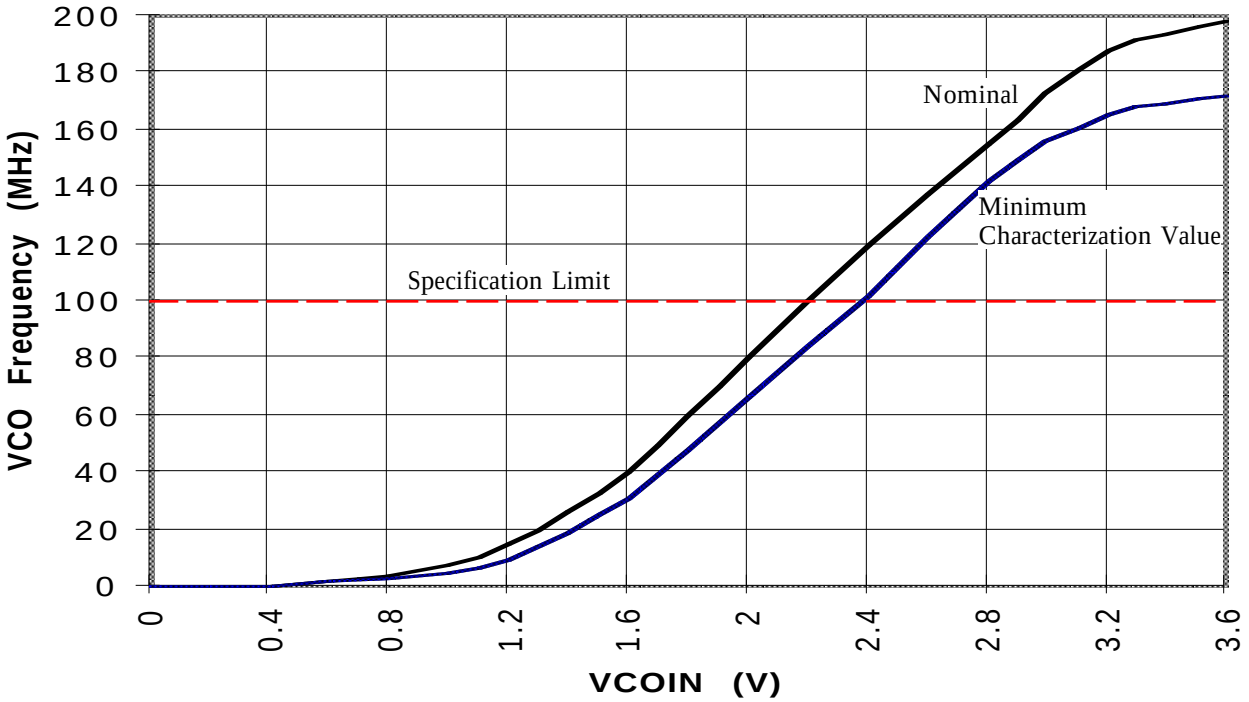


Figure 3. VCO Frequency vs Input Voltage at VDD = 3.3 V.

Avoiding PLL Lockup

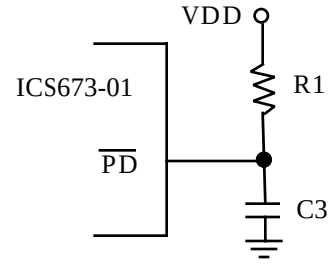
In some applications, the ICS673 can "lock up" at the maximum VCO frequency. This is usually caused by power supply glitches or a very slow power supply ramp. This situation also occurs if the external divider starts to fail at high input frequencies. The usual failure mode of a divider circuit is that the output of the divider begins to miss clock edges. The phase detector interprets this as a too low output frequency and increases the VCO frequency. The feedback divider begins to miss even more clock edges, and the VCO frequency is continually increased until it is running at the maximum. Whether caused by power supply issues or by the external divider, the loop can only recover by powering down the circuit, asserting $\overline{PD}$, or shorting the loop filter to ground.

The simplest way to avoid this problem is to use an external divider that always operates correctly regardless of the VCO speed. Figures 2 and 3 show that the VCO is capable of high speeds. By using the internal divide-by-four and/or the CLK2 output, the maximum VCO frequency can be divided by 2, 4, or 8 and a slower counter can be used. Using the ICS673 internal dividers in this manner does reduce the number of frequencies that can be exactly synthesized by forcing the total VCO divide to change in increments of 2, 4, or 8.

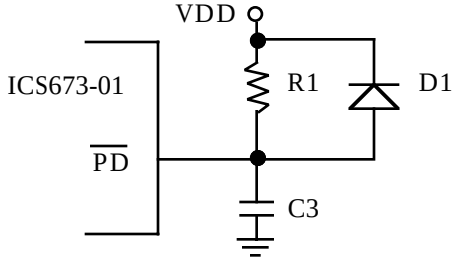
If this lockup problem occurs, there are several solutions, three of which are described below.

1. If the system has a reset or power good signal, this should be applied to the $\overline{PD}$ pin, forcing the ICS673 to stay powered down until the power supply voltage has stabilized.

2. If no power good signal is available, a simple power-on reset circuit can be attached to the $\overline{PD}$ pin, as shown in Figure 4 below. When the power supply ramps up, this circuit holds $\overline{PD}$ asserted (device powered down) until the capacitor charges up.



A. Basic Circuit



B. Faster Discharge

Figure 4. Power-on Reset Circuits.

The circuit of Figure 4A is adequate in most cases, but the discharge rate of capacitor C3 when VDD goes low is limited by R1. As this discharge rate determines the minimum reset time, the circuit of Figure 4B may be used when a faster reset time is desired. The values of R1 and C3 should be selected to ensure that $\overline{PD}$ stays below 1.0 V until the power supply is stable.

3. A comparator circuit may be used to monitor the loop filter voltage, as shown in Figure 5. This circuit will dump the charge off the loop filter by asserting $\overline{PD}$ if the VCO begins to run too fast, and the PLL can recover. A good choice for this comparator is the National Semiconductor LMC7211BIM5X. It is low

Avoiding PLL Lockup (continued)

power, very small (SOT-23), low cost, and has high input impedance.

The trigger voltage of the comparator is set by the voltage divider formed by R2 and R3. The voltage should be set to a value higher than the VCO input is expected to run during normal operation. Typically, this might be 0.5 V below VDD. Hysteresis should be added to the circuit by connecting resistor R4.

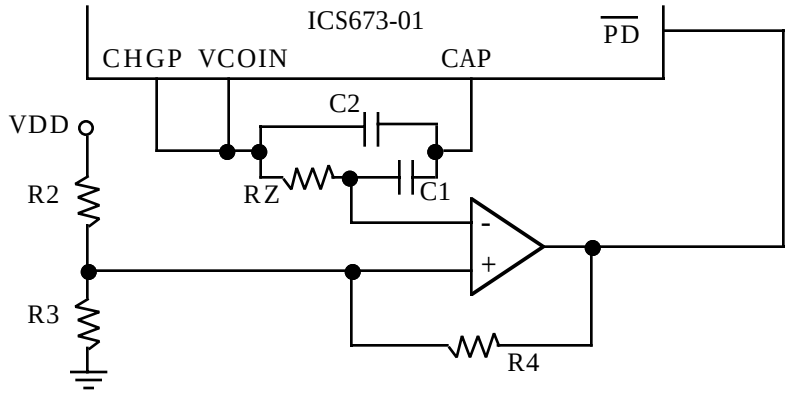
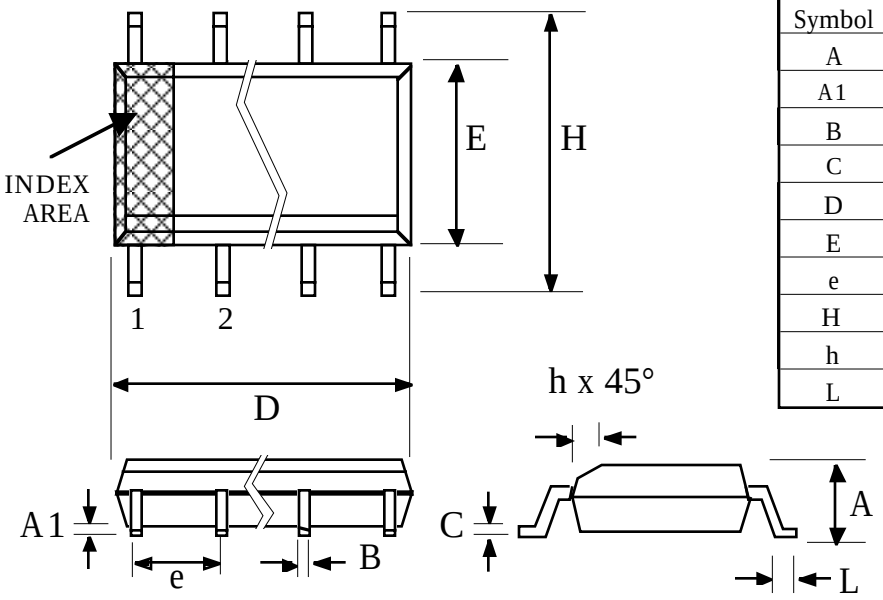


Figure 5. Using an External Comparator to Reset the VCO.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



16 pin SOIC narrow

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
ICS673M-01	ICS673M-01	tubes	16 pin SOIC	0 to 70 °C
ICS673M-01T	ICS673M-01	tape and reel	16 pin SOIC	0 to 70 °C
ICS673M-01I	ICS673M-01I	tubes	16 pin SOIC	-40 to 85 °C
ICS673M-01IT	ICS673M-01I	tape and reel	16 pin SOIC	-40 to 85 °C

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