Low Power Multiclock Generator with VCXO

AK8130A

Features

- 27MHz Crystal Input
- Four Frequency-Selectable Clock Outputs
- One 27MHz-Reference Output
- Selectable Clock out Frequencies:
  - 54.000,74.1758, 74.250MHz
  - 25.000MHz
  - 4.9152, 12.000, 48.000MHz
  - 24.576, 33.333MHz
- Built-in VCXO
  - Pull Range: ±110ppm (Min.)
- Low Jitter Performance
  - Period Jitter:
    150 psec (Typ.) at CLK1-4
  - Long Term Jitter :
    160 psec (Typ.) at REFOUT
- Low Current Consumption:
  16.5mA (Typ.) at 3.3V
- Supply Voltage:
  3.0 – 3.6V
- Operating Temperature Range:
  -20 to +85℃
- Package:
  16-pin TSSOP (Lead free)

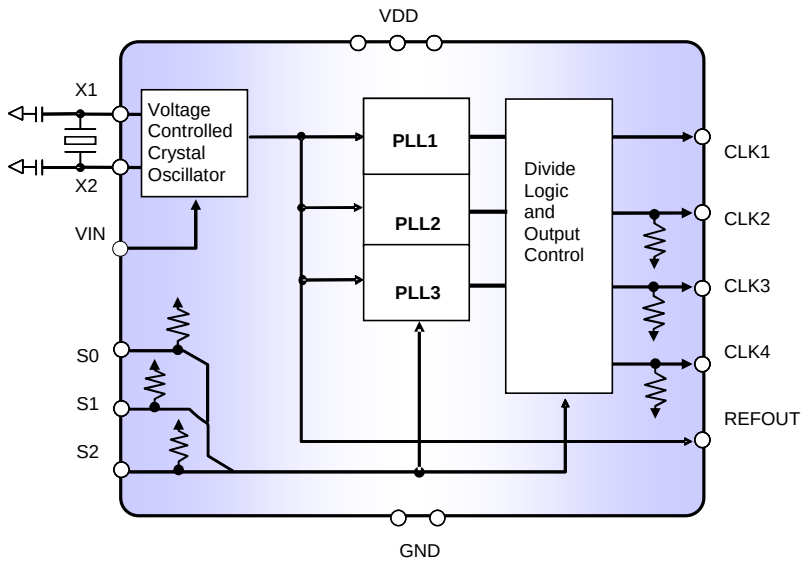
Description

The AK8130A is a member of AKEMD's low power multi clock generator family designed for a feature rich DTV or STB, requiring a range of system clocks with high performance. The AK8130A generates different frequency clocks from a 27MHz crystal oscillator and provides them to up to four outputs configured by pin-setting. The on-chip VCXO accepts a voltage control input to allow the output clocks to vary by ±110 ppm for synchronizing to the external clock system. Both circuitries of VCXO and PLL in AK8130A are derived from AKEMD's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption. The AK8130A is available in a 16-pin SSOP package.

Applications

- Digital TV Sets
- Personal Video Recorders
- Set-Top-Boxes
- Multi Media Receivers

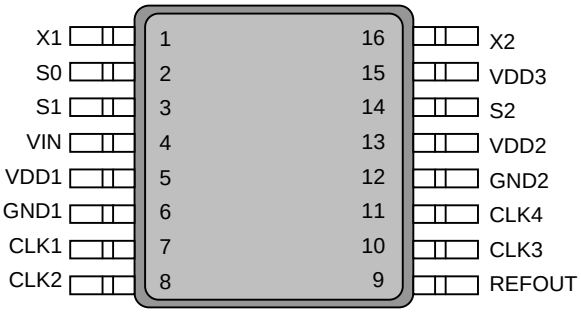
Block Diagram



AK8130A Multi Clock Generator

Pin Descriptions

Package: 16-Pin TSSOP(Top View)



Pin No.	Pin Name	Pin Type	Description
1	X1	XO	Crystal connection, Connect to 27.000MHz crystal
2	S0	IN	Clock Out Frequency Select 0, See Table 1 for the selection (1)
3	S1	IN	Clock Out Frequency select 1, See Table 1 for the selection (1)
4	VIN	IN	VCXO Control Voltage Input
5	VDD1	--	Power Supply 1
6	GND1	--	Ground 1
7	CLK1	OUT	Clock output 1, See Table 1 for its selectable frequency
8	CLK2	OUT	Clock output 2, See Table 1 for its selectable frequency (2)
9	REF OUT	OUT	Reference Clock Output of VCXO based on 27.000MHz Crystal
10	CLK3	OUT	Clock output 3, See Table 1 for its selectable frequency (2)
11	CLK4	OUT	Clock output 4, See Table 1 for its selectable frequency (2)
12	GND2	--	Ground 2
13	VDD2	--	Power Supply 2
14	S2	IN	Clock Out Frequency select 1, See Table 1 for the selection (1)
15	VDD3	--	Power Supply 3
16	X2	XI	Crystal connection, Connect to 27.000MHz crystal

(1) Internal pull up 360kΩ

(2) Internal pull down 510kΩ

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8130A	8130A	Tape and Reel	16-pin TSSOP	-20 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	**VSS-0.3 to VDD+0.3**	V
Input current (any pins except supplies)	I_{IN}	**±**10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.



ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKEMD recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-20		85	°C
Supply voltage (1)	VDD		3.0	3.3	3.6	V
Output Load Capacitance	Cp1	Pin: CLK1-4			15	pF
	Cp2	Pin: REFOUT			25	pF

Note:

(1) Power to VDD1, VDD2 and VDD3 requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be installed close to each VDD pin.

DC Characteristics

All specifications at VDD: over 3.0 to 3.6V, Ta: -20 to +85℃, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: S0,S1,S2	0.7VDD			V
Low Level Input Voltage	V_{IL}	Pin: S0,S1,S2			0.3VDD	V
Input Current 1	I_L1	Pin: S0,S1,S2	-20		+10	µA
Input Current 2	I_L2	PIN: VIN	-3		+3	µA
High Level Output Voltage	V_{OH}	Pin: CLK1-4, REFOUT I_{OH}=-4mA	0.8VDD			V
Low level Output Voltage	V_{OL}	Pin: CLK1-4, REFOUT I_{OL}=+4mA			0.2VDD	V
Current Consumption	I_{DD}	Clock out selection by note (1) No load,Ta=25℃		16.5		mA

(1) Pin setting for output clock selection: [S2:S0] = HLH

AC Characteristics

All specifications at VDD: over 3.0 to 3.6V, Ta: over -20 to +85℃, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Crystal Clock Frequency				27.0000		MHz
VCXO Pullable Range (3)		VIN at over 0 to VDD V	±110			ppm
VCXO Gain	G_{VCXO}	VIN range at 1.5V±1.0V		150		ppm/V
Period Jitter (4)		CLK1-4		150		ps
Long Term Jitter (5)		CLK1 at 54.000MHz 1000 cycle delay		0.5		ns
		CLK1 at 74.250MHz 1000 cycle delay		0.85		ns
		REFOUT at 27.000MHz 1000 cycle delay		160		ps
Output Clock Duty Cycle		Pin: CLK1-4 (1)	45	50	55	%
		Pin: REFOUT (2)	40	50	60	%
Output Clock Rise Time	t_{rise}	Pin: CLK1-4 (1)		1.5		ns
		Pin: REFOUT (2)		2.5		ns
Output Clock Fall Time	t_{fall}	Pin: CLK1-4 (1)		1.5		ns
		Pin: REFOUT (2)		2.5		ns
Power-up Time		Pin: CLK1-4 (1)		1		ms
Output Transition Time (6)		Pin: CLK1 at 74.25 or 74.175MHz		60		µs

(1) Measured with load capacitance of 15pF

(2) Measured with load capacitance of 25pF

(3) Pullable range depends on crystal characteristics, on-chip load capacitance, and stray capacity of PCB. Min. ±110ppm is applied to AKEMD's authorized test condition.

(4) **±3**σ in 1000 sampling or more

(5) **±3**σ in 5000 sampling or more

(6) Time to settle output into **±**20ppm of specified frequency

Output clock frequency selection

The AK8130A generates a range of low-jitter and hi-accuracy clock frequencies with three built-in PLLs and provides to up to four assigned outputs. A frequency selection at assigned output pin is configured by pin-setting of S0 (Pin2), S1 (Pin3), and S2 (Pin14).
The selectable frequency is shown in **Table 1**..

Table 1: Clock output Frequency

Selection Pin			Clock Output Frequency (MHz)			
S2 (Pin 14)	**S1** (Pin 3)	**S0** (Pin 2)	**CLK1** (Pin 7)	**CLK2** (Pin 8)	**CLK3** (Pin 10)	**CLK4** (Pin 11)
L	L	L	74.250	25.000	48.000	33.333
L	L	H	74.250	25.000	12.000	OFF
L	H	L	74.1758	25.000	48.000	33.333
L	H	H	74.1758	25.000	12.000	OFF
H	L	L	74.1758	25.000	OFF	33.333
H	L	H	74.1758	25.000	4.9152	OFF
H	H	L	74.1758	25.000	4.9152	24.576
H	H	H	54.000	OFF	4.9152	24.576

Voltage Control Crystal Oscillator (VCXO)

The AK8130A has a voltage control crystal oscillator (VCXO), featuring fine frequency tuning for 27MHz of primary clock frequency by external DC voltage control. This tuning enables output clock frequency to synchronize the external clock system. VIN (Pin 4) accepts DC voltage control from a processor or a system controller, and pulls the primary frequency of crystal to higher or lower. This pulling range is determined by crystal characteristic, on-chip load capacitor, and stray capacitance of PCB. The AK8130A is designed to range ±110ppm of primary frequency in AKEMD's authorized condition, and the typical pulling profile is shown in **Figure 1**. For details about the condition and other specific crystal application case, refer the AK8130 Family application note.

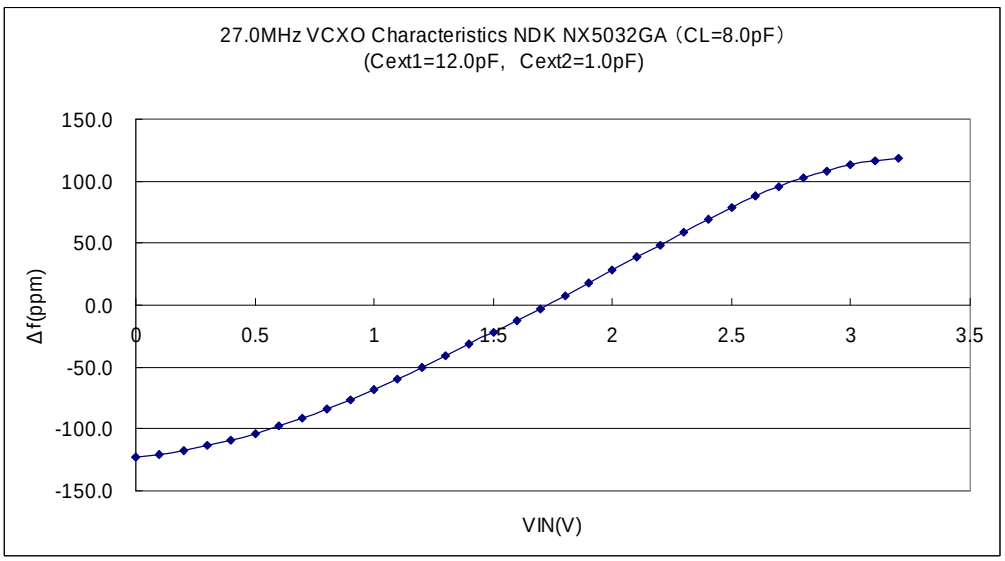


Figure 1: Typical VCXO Pulling Profile

Typical Connection Diagram

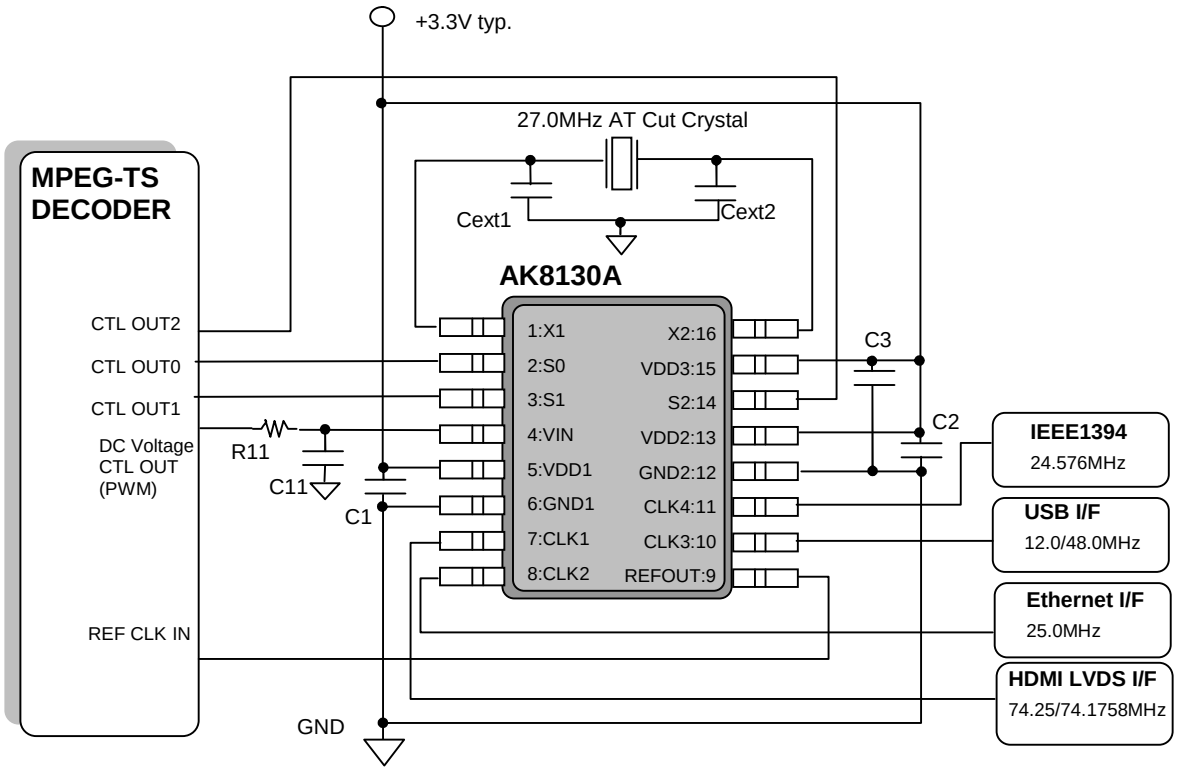


Figure 2: Typical Connection Diagram

C1, C2, C3: 0.1µF
Cext1, Cext2: Depends on crystal characteristics. Refer the specification of the crystal.
R11, C11: In case of interface by PWM. For right configuration, refer the specification of the applied processor.

PCB Layout Consideration

The AK8130A is a high-accuracy and low-jitter multi clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure 2

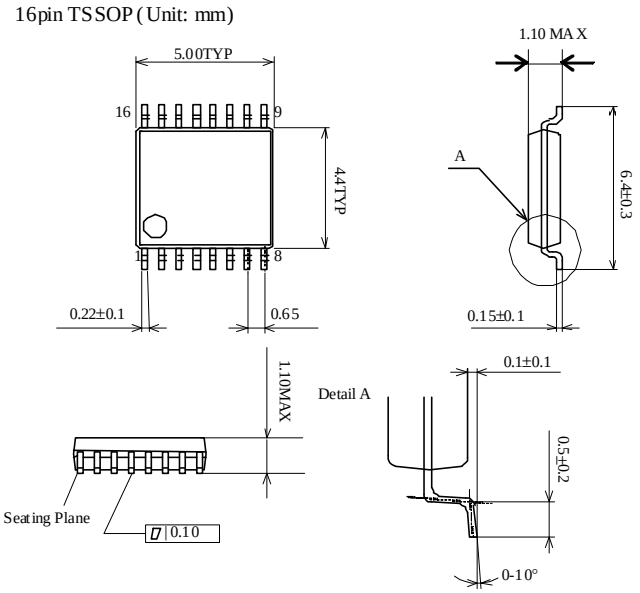
Power supply line – AK8130A has three power supply pins (VDD1-3) which deliver power to internal circuitry segments. A 0.1µF decoupling capacitor should be placed as close to each VDD pin as possible.

Ground pin connection – AK8130A has two ground pins (GND1-2). These pin require connecting to plane ground which will eliminate any common impedance with other critical switching signal return. 0.1µF decoupling capacitors placed at VDD1, VDD2, and VDD3 should be grounded at close to the GND1pin, the GND2 pin, and the GND2, respectively.

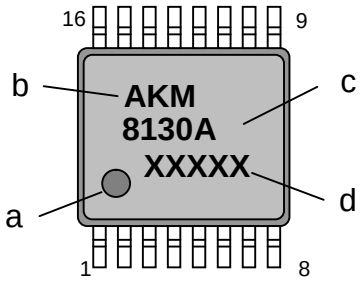
Crystal connection – Proper oscillation performance and pullable range are susceptible to stray or parasitic capacitors around crystal. The wiring traces to a crystal form X1 (Pin 1) and X2 (Pin 14) have equal lengths with no via and as short in length as possible. These traces should be also located away from any traces with switching signal.

Package Information

• Mechanical data



• Marking

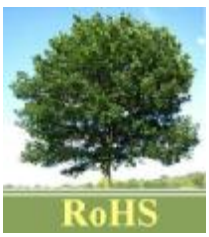


a: #1 Pin Index
b: Product Family Logo (1)
c: Part number
d Date code (5 digits)

(1) **AKM** is the brand name of AKEMD's IC's.

AKM and the logo - - are the brand of AKEMD's IC's and identify that AKEMD continues to offer the best choice for high performance mixed-signal solution under this brand.

• RoHS Compliance



All integrated circuits form Asahi Kasei EMD Corporation (AKEMD) assembled in "lead-free" packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKEMD are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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  - Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
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