



DRV5055 Ratiometric Linear Hall Effect Sensor

1 Features

- Ratiometric Linear Hall Effect Magnetic Sensor
- Operates From 3.3-V and 5-V Power Supplies
- Analog Output With $V_{CC} / 2$ Quiescent Offset
- Magnetic Sensitivity Options (At $V_{CC} = 5\text{ V}$):
 - A1: 100 mV/mT, $\pm 21\text{-mT}$ Range
 - A2: 50 mV/mT, $\pm 42\text{-mT}$ Range
 - A3: 25 mV/mT, $\pm 85\text{-mT}$ Range
 - A4: 12.5 mV/mT, $\pm 169\text{-mT}$ Range
- Fast 20-kHz Sensing Bandwidth
- Low-Noise Output With $\pm 1\text{-mA}$ Drive
- Compensation For Magnet Temperature Drift
- Standard Industry Packages:
 - Surface-Mount SOT-23
 - Through-Hole TO-92

2 Applications

- Precise Position Sensing
- Industrial Automation and Robotics
- Home Appliances
- Gamepads, Pedals, Keyboards, Triggers
- Height Leveling, Tilt and Weight Measurement
- Fluid Flow Rate Measurement
- Medical Devices
- Absolute Angle Encoding
- Current Sensing

3 Description

The DRV5055 device is a linear Hall effect sensor that responds proportionally to magnetic flux density. The device can be used for accurate position sensing in a wide range of applications.

The device operates from 3.3-V or 5-V power supplies. When no magnetic field is present, the analog output drives half of V_{CC} . The output changes linearly with the applied magnetic flux density, and four sensitivity options enable maximal output voltage swing based on the required sensing range. North and south magnetic poles produce unique voltages.

Magnetic flux perpendicular to the top of the package is sensed, and the two package options provide different sensing directions.

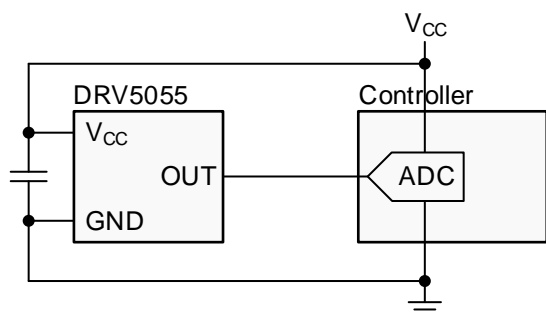
The device uses a ratiometric architecture that can eliminate error from V_{CC} tolerance when the external analog-to-digital converter (ADC) uses the same V_{CC} for its reference. Additionally, the device features magnet temperature compensation to counteract how magnets drift for linear performance across a wide -40°C to 125°C temperature range.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5055	SOT-23 (3)	2.92 mm × 1.30 mm
	TO-92 (3)	4.00 mm × 3.15 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Schematic



Copyright © 2017, Texas Instruments Incorporated

Magnetic Response

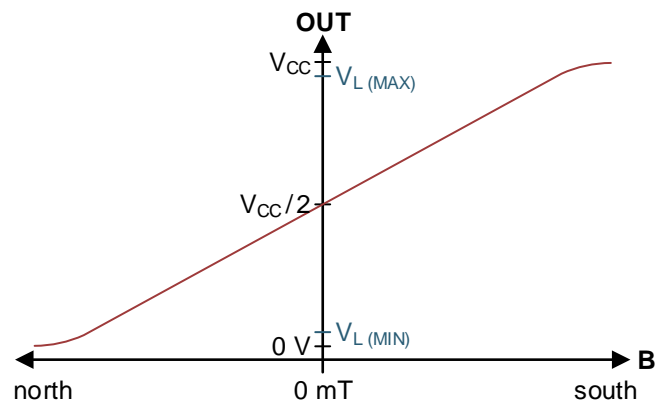


Table of Contents

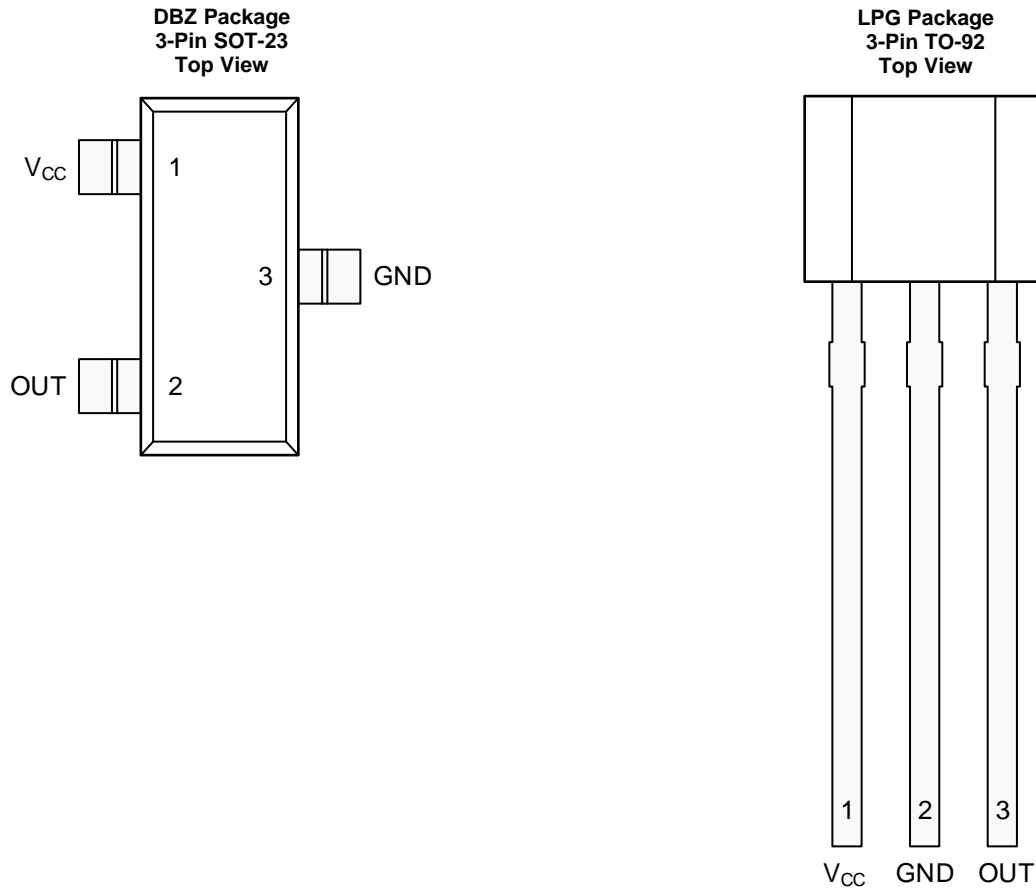
1 Features	1	7.4 Device Functional Modes.....	12
2 Applications	1	8 Application and Implementation	13
3 Description	1	8.1 Application Information.....	13
4 Revision History	2	8.2 Typical Application	14
5 Pin Configuration and Functions	3	8.3 Do's and Don'ts	16
6 Specifications	3	9 Power Supply Recommendations	17
6.1 Absolute Maximum Ratings	3	10 Layout	17
6.2 ESD Ratings.....	4	10.1 Layout Guidelines	17
6.3 Recommended Operating Conditions.....	4	10.2 Layout Examples.....	17
6.4 Thermal Information	4	11 Device and Documentation Support	18
6.5 Electrical Characteristics.....	4	11.1 Documentation Support	18
6.6 Magnetic Characteristics.....	5	11.2 Receiving Notification of Documentation Updates	18
6.7 Typical Characteristics	6	11.3 Community Resources.....	18
7 Detailed Description	8	11.4 Trademarks	18
7.1 Overview	8	11.5 Electrostatic Discharge Caution.....	18
7.2 Functional Block Diagram	8	11.6 Glossary	18
7.3 Feature Description.....	8	12 Mechanical, Packaging, and Orderable Information	18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2018	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	TO-92		
V _{CC}	1	1	—	Power supply. TI recommends connecting this pin to a ceramic capacitor to ground with a value of at least 0.01 μ F.
OUT	2	3	O	Analog output
GND	3	2	—	Ground reference

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Power supply voltage	V _{CC}	–0.3	7	V
Output voltage	OUT	–0.3	V _{CC} + 0.3	V
Magnetic flux density, B _{MAX}		Unlimited		T
Operating junction temperature, T _J		–40	150	°C
Storage temperature, T _{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	
		±2500	
		±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Power supply voltage ⁽¹⁾	3	3.63	V
		4.5	5.5	
I _O	Output continuous current	–1	1	mA
T _A	Operating ambient temperature ⁽²⁾	–40	125	°C

(1) There are two isolated operating V_{CC} ranges. For more information see the [Operating V_{CC} Ranges](#) section.

(2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV5055		UNIT
		SOT-23 (DBZ)	TO-92 (LPG)	
		3 PINS	3 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	170	121	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	66	67	°C/W
R _{θJB}	Junction-to-board thermal resistance	49	97	°C/W
Y _{JT}	Junction-to-top characterization parameter	1.7	7.6	°C/W
Y _{JB}	Junction-to-board characterization parameter	48	97	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

for V_{CC} = 3 V to 3.63 V and 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
I _{CC}	Operating supply current		6	10	mA
t _{ON}	Power-on time (see Figure 11)	B = 0 mT, no load on OUT		175	330
f _{BW}	Sensing bandwidth		20		kHz
t _d	Propagation delay time	From change in B to change in OUT		10	μs
B _{ND}	Input-referred RMS noise density	V _{CC} = 5 V		130	nT/√Hz
		V _{CC} = 3.3 V		215	
B _N	Input-referred noise	B _{ND} × 6.6 × √20 kHz	V _{CC} = 5 V	0.12	mT _{PP}
			V _{CC} = 3.3 V	0.2	
V _N	Output-referred noise ⁽²⁾	B _N × S	DRV5055A1	12	mV _{PP}
			DRV5055A2	6	
			DRV5055A3	3	
			DRV5055A4	1.5	

(1) B is the applied magnetic flux density.

(2) V_N describes voltage noise on the device output. If the full device bandwidth is not needed, noise can be reduced with an RC filter.

6.6 Magnetic Characteristics

for $V_{CC} = 3\text{ V}$ to 3.63 V and 4.5 V to 5.5 V , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
V _Q	Quiescent voltage	B = 0 mT, T _A = 25°C	V _{CC} = 5 V	2.43	2.5	2.57	V
			V _{CC} = 3.3 V	1.59	1.65	1.71	
V _{QAT}	Quiescent voltage temperature drift	B = 0 mT, T _A = -40°C to 125°C versus 25°C		±1% × V _{CC}			V
V _{QRE}	Quiescent voltage ratiometry error ⁽²⁾			±0.2%			
V _{QAL}	Quiescent voltage lifetime drift	High-temperature operating stress for 1000 hours		<0.5%			
S	Sensitivity	V _{CC} = 5 V, T _A = 25°C	DRV5055A1	95	100	105	mV/mT
			DRV5055A2	47.5	50	52.5	
			DRV5055A3	23.8	25	26.2	
			DRV5055A4	11.9	12.5	13.2	
		V _{CC} = 3.3 V, T _A = 25°C	DRV5055A1	57	60	63	
			DRV5055A2	28.5	30	31.5	
			DRV5055A3	14.3	15	15.8	
			DRV5055A4	7.1	7.5	7.9	
B _L	Linear magnetic sensing range ^{(3) (4)}	V _{CC} = 5 V, T _A = 25°C	DRV5055A1	±21			mT
			DRV5055A2	±42			
			DRV5055A3	±85			
			DRV5055A4	±169			
		V _{CC} = 3.3 V, T _A = 25°C	DRV5055A1	±22			
			DRV5055A2	±44			
			DRV5055A3	±88			
			DRV5055A4	±176			
V _L	Linear range of output voltage ⁽⁴⁾			0.2	V _{CC} – 0.2		V
S _{TC}	Sensitivity temperature compensation for magnets ⁽⁵⁾			0.12			%/°C
S _{LE}	Sensitivity linearity error ⁽⁴⁾	V _{OUT} is within V _L		±1%			
S _{SE}	Sensitivity symmetry error ⁽⁴⁾	V _{OUT} is within V _L		±1%			
S _{RE}	Sensitivity ratiometry error ⁽²⁾	T _A = 25°C, with respect to V _{CC} = 3.3 V or 5 V		–2.5% 2.5%			
S _{ΔL}	Sensitivity lifetime drift	High-temperature operating stress for 1000 hours		<0.5%			%

(1) B is the applied magnetic flux density.

(2) See the [Ratiometric Architecture](#) section.

(3) B_L describes the minimum linear sensing range at 25°C taking into account the maximum V_Q and Sensitivity tolerances.

(4) See the [Sensitivity Linearity](#) section.

(5) S_{TC} describes the rate the device increases Sensitivity with temperature. For more information, see the [Sensitivity Temperature Compensation For Magnets](#) section.

6.7 Typical Characteristics

for $T_A = 25^\circ\text{C}$ (unless otherwise noted)

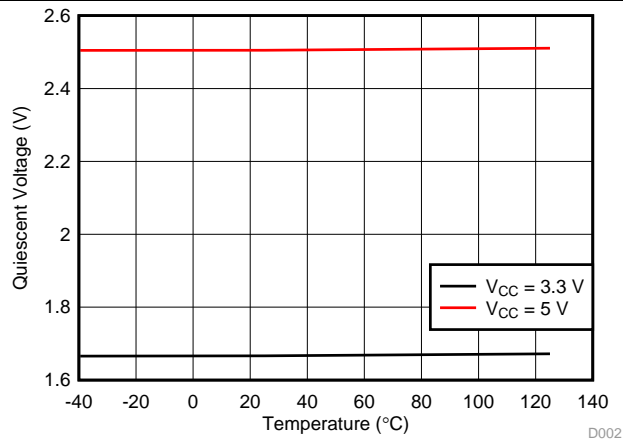


Figure 1. Quiescent Voltage vs Temperature

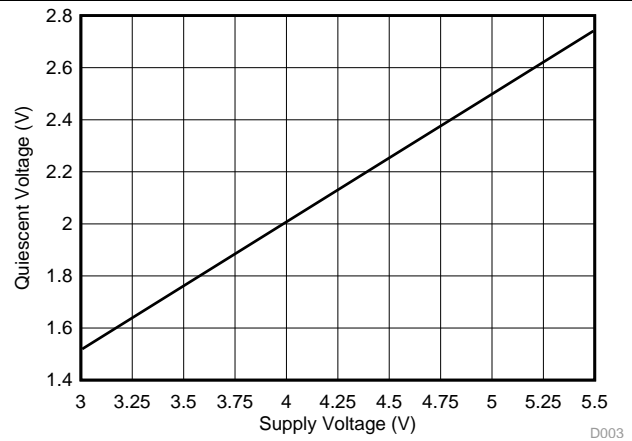


Figure 2. Quiescent Voltage vs Supply Voltage

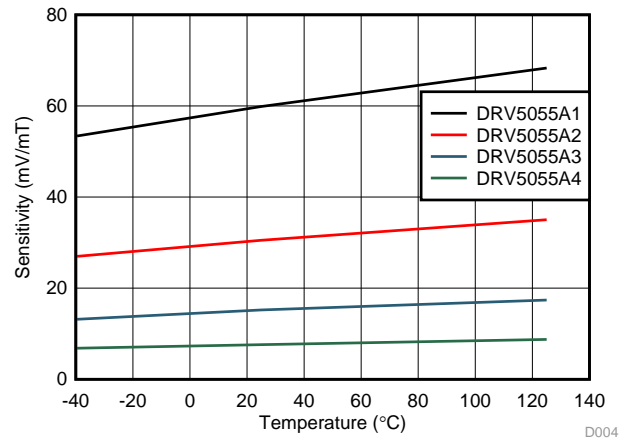


Figure 3. Sensitivity vs Temperature, $V_{CC} = 3.3\text{ V}$

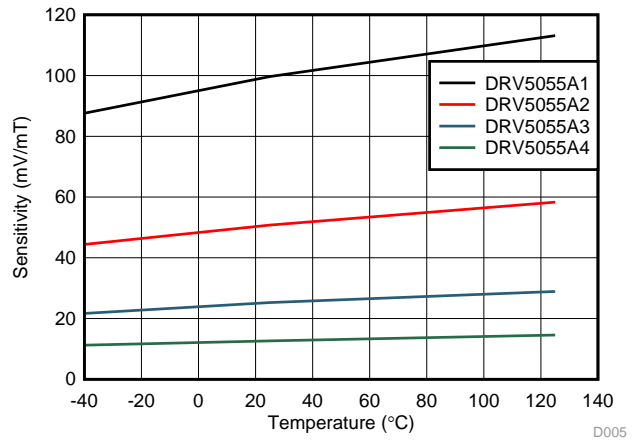


Figure 4. Sensitivity vs Temperature, $V_{CC} = 5\text{ V}$

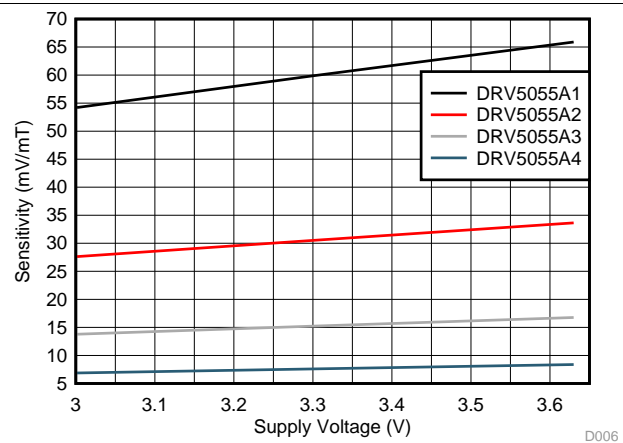


Figure 5. Sensitivity vs Supply Voltage, $V_{CC} = 3.3\text{ V} \pm 10\%$

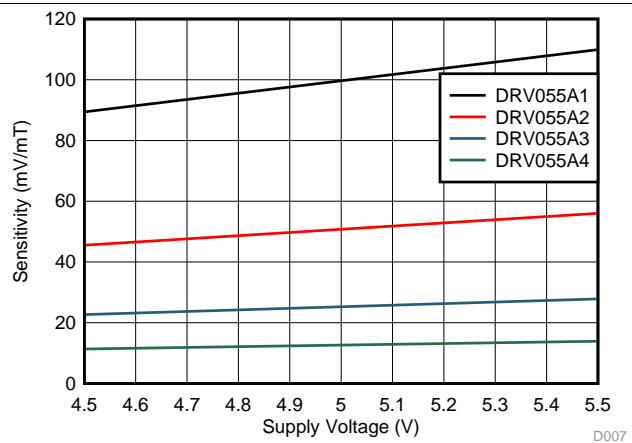


Figure 6. Sensitivity vs Supply Voltage, $V_{CC} = 5\text{ V} \pm 10\%$

Typical Characteristics (continued)

for $T_A = 25^\circ\text{C}$ (unless otherwise noted)

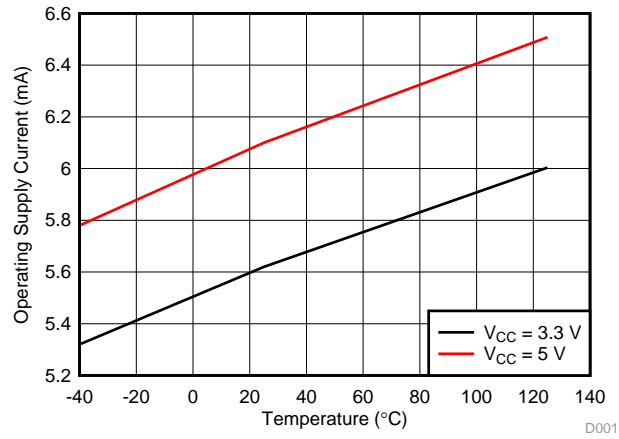


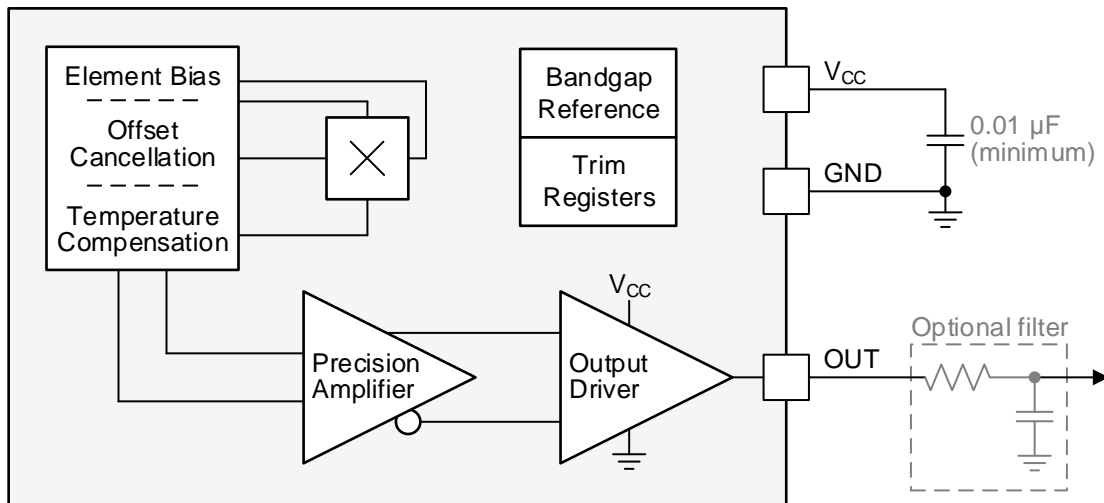
Figure 7. Operating Supply Current vs Temperature

7 Detailed Description

7.1 Overview

The DRV5055 is a 3-pin linear Hall effect sensor with fully integrated signal conditioning, temperature compensation circuits, mechanical stress cancellation, and amplifiers. The device operates from 3.3-V and 5-V ($\pm 10\%$) power supplies, measures magnetic flux density, and outputs a proportional analog voltage that is referenced to V_{CC} .

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Magnetic Flux Direction

As shown in Figure 8, the DRV5055 is sensitive to the magnetic field component that is perpendicular to the top of the package.

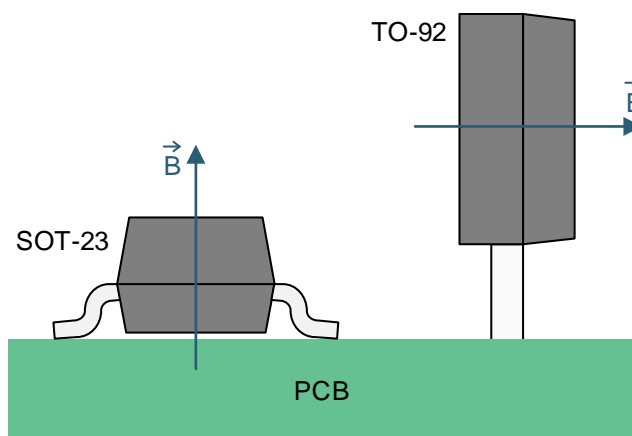


Figure 8. Direction of Sensitivity

Feature Description (continued)

Magnetic flux that travels from the bottom to the top of the package is considered positive in this document. This condition exists when a south magnetic pole is near the top (marked-side) of the package. Magnetic flux that travels from the top to the bottom of the package results in negative millitesla values.

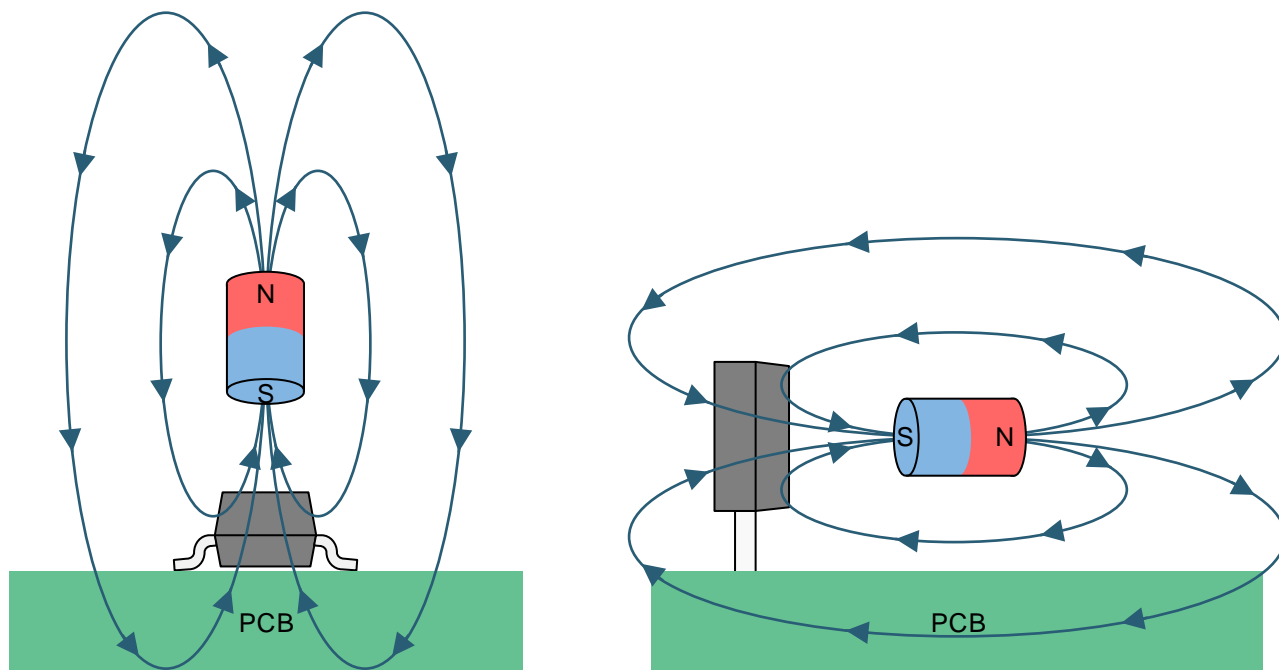


Figure 9. The Flux Direction for Positive B

7.3.2 Magnetic Response

When the DRV5055 is powered, the DRV5055 outputs an analog voltage according to Equation 1:

$$V_{OUT} = V_Q + B \times (\text{Sensitivity}_{(25^\circ\text{C})} \times (1 + S_{TC} \times (T_A - 25^\circ\text{C})))$$

where

- V_Q is typically half of V_{CC}
- B is the applied magnetic flux density
- $\text{Sensitivity}_{(25^\circ\text{C})}$ depends on the device option and V_{CC}
- S_{TC} is typically 0.12%/°C
- T_A is the ambient temperature
- V_{OUT} is within the V_L range

(1)

As an example, consider the DRV5055A3 with $V_{CC} = 3.3\text{ V}$, a temperature of 50°C , and 67 mT applied. Excluding tolerances, $V_{OUT} = 1650\text{ mV} + 67\text{ mT} \times (15\text{ mV/mT} \times (1 + 0.0012/^\circ\text{C} \times (50^\circ\text{C} - 25^\circ\text{C}))) = 2685\text{ mV}$.

7.3.3 Sensitivity Linearity

The device produces a linear response when the output voltage is within the specified V_L range. Outside this range, sensitivity is reduced and nonlinear. Figure 10 graphs the magnetic response.

Feature Description (continued)

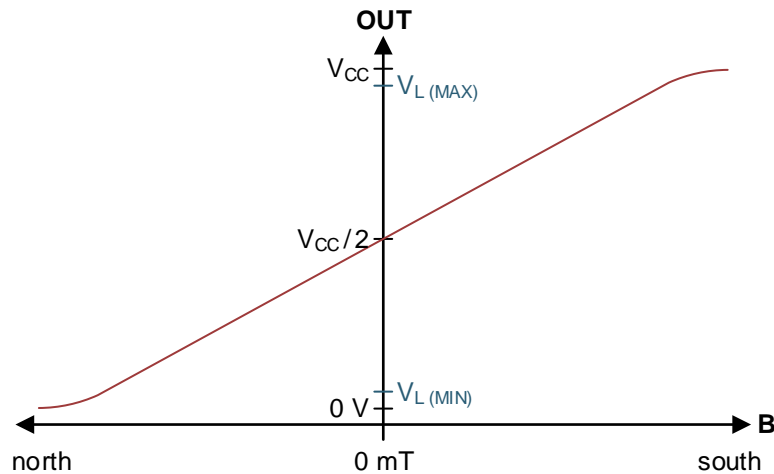


Figure 10. Magnetic Response

Equation 2 calculates parameter B_L , the minimum linear sensing range at 25°C taking into account the maximum quiescent voltage and sensitivity tolerances.

$$B_{L(MIN)} = \frac{V_{L(MAX)} - V_{Q(MAX)}}{S_{(MAX)}} \quad (2)$$

The parameter S_{LE} defines linearity error as the difference in sensitivity between any two positive B values, and any two negative B values, while the output is within the V_L range.

The parameter S_{SE} defines symmetry error as the difference in sensitivity between any positive B value and the negative B value of the same magnitude, while the output voltage is within the V_L range.

7.3.4 Ratiometric Architecture

The DRV5055 has a ratiometric analog architecture that scales the quiescent voltage and sensitivity linearly with the power-supply voltage. For example, the quiescent voltage and sensitivity are 5% higher when $V_{CC} = 5.25$ V compared to $V_{CC} = 5$ V. This behavior enables external ADCs to digitize a consistent value regardless of the power-supply voltage tolerance, when the ADC uses V_{CC} as its reference.

Equation 3 calculates sensitivity ratiometry error:

$$S_{RE} = 1 - \frac{S_{(VCC)} / S_{(5V)}}{V_{CC} / 5V} \text{ for } V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, \quad S_{RE} = 1 - \frac{S_{(VCC)} / S_{(3.3V)}}{V_{CC} / 3.3V} \text{ for } V_{CC} = 3 \text{ V to } 3.63 \text{ V}$$

where

- $S_{(VCC)}$ is the sensitivity at the current V_{CC} voltage
- $S_{(5V)}$ or $S_{(3.3V)}$ is the sensitivity when $V_{CC} = 5$ V or 3.3 V
- V_{CC} is the current V_{CC} voltage

Equation 4 calculates quiescent voltage ratiometry error:

$$V_{QRE} = 1 - \frac{V_{Q(VCC)} / V_{Q(5V)}}{V_{CC} / 5V} \text{ for } V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, \quad V_{QRE} = 1 - \frac{V_{Q(VCC)} / V_{Q(3.3V)}}{V_{CC} / 3.3V} \text{ for } V_{CC} = 3 \text{ V to } 3.63 \text{ V}$$

where

- $V_{Q(VCC)}$ is the quiescent voltage at the current V_{CC} voltage
- $V_{Q(5V)}$ or $V_{Q(3.3V)}$ is the quiescent voltage when $V_{CC} = 5$ V or 3.3 V
- V_{CC} is the current V_{CC} voltage

Feature Description (continued)

7.3.5 Operating V_{CC} Ranges

The DRV5055 has two recommended operating V_{CC} ranges: 3 V to 3.63 V and 4.5 V to 5.5 V. When V_{CC} is in the middle region between 3.63 V to 4.5 V, the device continues to function, but sensitivity is less known because there is a crossover threshold near 4 V that adjusts device characteristics.

7.3.6 Sensitivity Temperature Compensation For Magnets

Magnets generally produce weaker fields as temperature increases. The DRV5055 compensates by increasing sensitivity with temperature, as defined by the parameter S_{TC} . The sensitivity at $T_A = 125^\circ\text{C}$ is typically 12% higher than at $T_A = 25^\circ\text{C}$.

7.3.7 Power-On Time

After the V_{CC} voltage is applied, the DRV5055 requires a short initialization time before the output is set. The parameter t_{ON} describes the time from when V_{CC} crosses 3 V until OUT is within 5% of V_Q , with 0 mT applied and no load attached to OUT. Figure 11 shows this timing diagram.

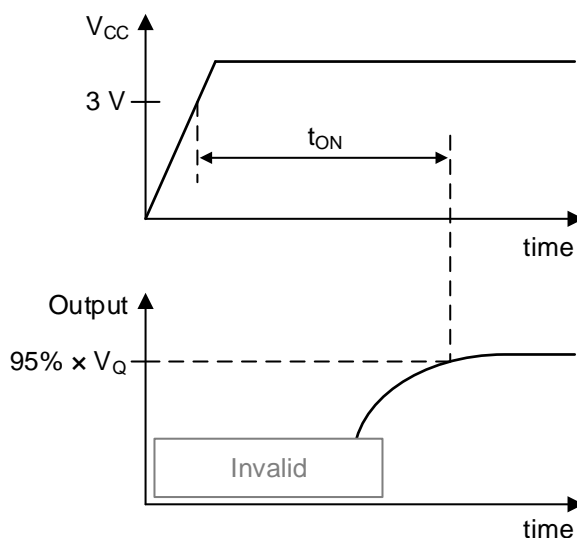


Figure 11. t_{ON} Definition

Feature Description (continued)

7.3.8 Hall Element Location

Figure 12 shows the location of the sensing element inside each package option.

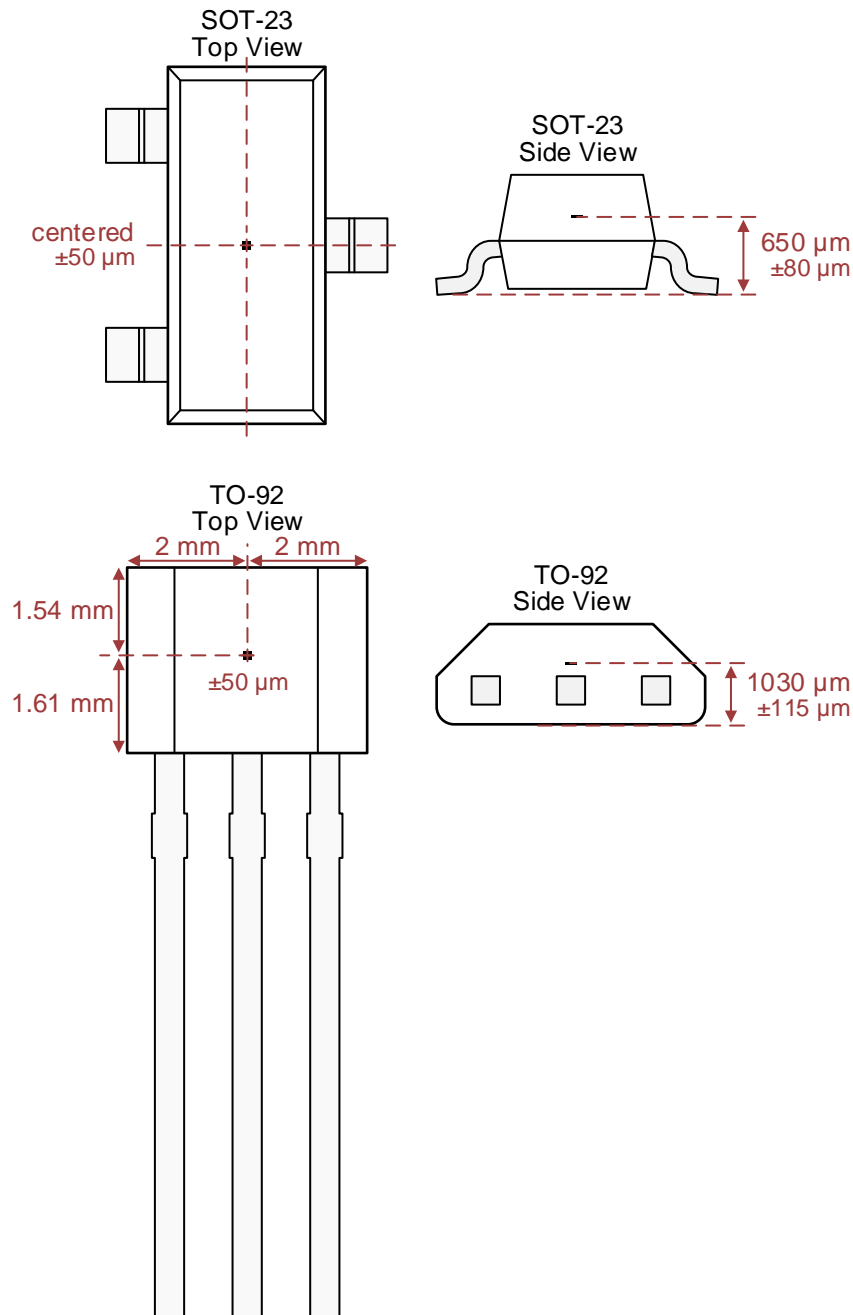


Figure 12. Hall Element Location

7.4 Device Functional Modes

The DRV5055 has one mode of operation that applies when the *Recommended Operating Conditions* are met.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Selecting the Sensitivity Option

Select the highest DRV5055 sensitivity option that can measure the required range of magnetic flux density, so that the output voltage swing is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations at <http://www.ti.com/product/drv5013>.

8.1.2 Temperature Compensation for Magnets

The DRV5055 temperature compensation is designed to directly compensate the average drift of neodymium (NdFeB) magnets and partially compensate ferrite magnets. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite. When the operating temperature of a system is reduced, temperature drift errors are also reduced.

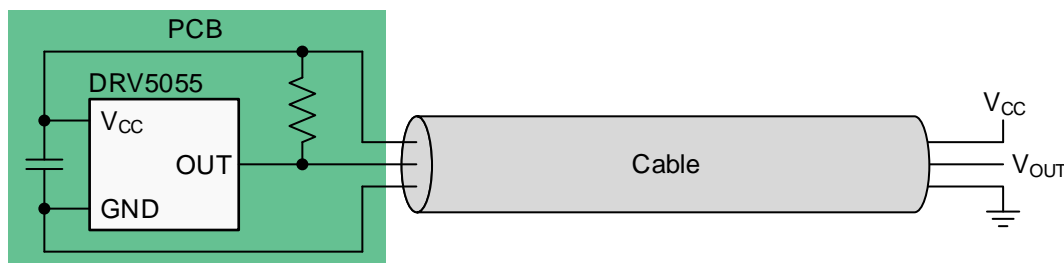
8.1.3 Adding a Low-Pass Filter

As shown in the [Functional Block Diagram](#), an RC low-pass filter can be added to the device output for the purpose of minimizing voltage noise when the full 20-kHz bandwidth is not needed. This filter can improve the signal-to-noise ratio (SNR) and overall accuracy. Do not connect a capacitor directly to the device output without a resistor in between because doing so can make the output unstable.

8.1.4 Designing for Wire Break Detection

Some systems must detect if interconnect wires become open or shorted. The DRV5055 can support this function.

First, select a sensitivity option that causes the output voltage to stay within the V_L range during normal operation. Second, add a pullup resistor between OUT and V_{CC} . TI recommends a value between 20 k Ω to 100 k Ω , and the current through OUT must not exceed the I_O specification, including current going into an external ADC. Then, if the output voltage is ever measured to be within 150 mV of V_{CC} or GND, a fault condition exists. [Figure 13](#) shows the circuit, and [Table 1](#) describes fault scenarios.



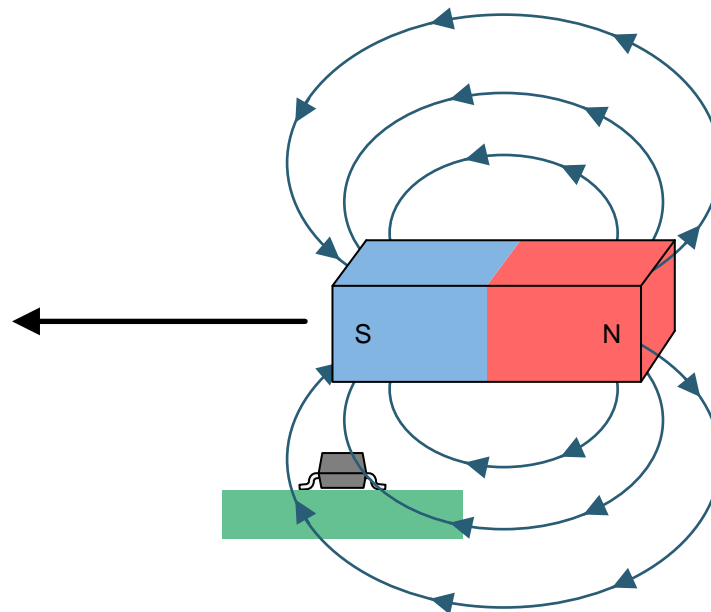
Copyright © 2017, Texas Instruments Incorporated

Figure 13. Wire Fault Detection Circuit

Table 1. Fault Scenarios and the Resulting V_{OUT}

FAULT SCENARIO	V_{OUT}
V_{CC} disconnects	Close to GND
GND disconnects	Close to V_{CC}
V_{CC} shorts to OUT	Close to V_{CC}
GND shorts to OUT	Close to GND

8.2 Typical Application


Figure 14. Common Magnet Orientation

8.2.1 Design Requirements

Use the parameters listed in [Table 2](#) for this design example.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC}	5 V
Magnet	15 × 5 × 5 mm NdFeB
Travel distance	12 mm
Maximum B at the sensor at 25°C	±75 mT
Device option	DRV5055A3

8.2.2 Detailed Design Procedure

Linear Hall effect sensors provide flexibility in mechanical design, because many possible magnet orientations and movements produce a usable response from the sensor. [Figure 14](#) shows one of the most common orientations, which uses the full north to south range of the sensor and causes a close-to-linear change in magnetic flux density as the magnet moves across.

When designing a linear magnetic sensing system, always consider these three variables: the magnet, sensing distance, and the range of the sensor. Select the DRV5055 with the highest sensitivity that has a B_L (linear magnetic sensing range) that is larger than the maximum magnetic flux density in the application. To determine the magnetic flux density the sensor receives, TI recommends using magnetic field simulation software, referring to magnet specifications, and testing.

8.2.3 Application Curve

Figure 15 shows the simulated magnetic flux from a NdFeB magnet.

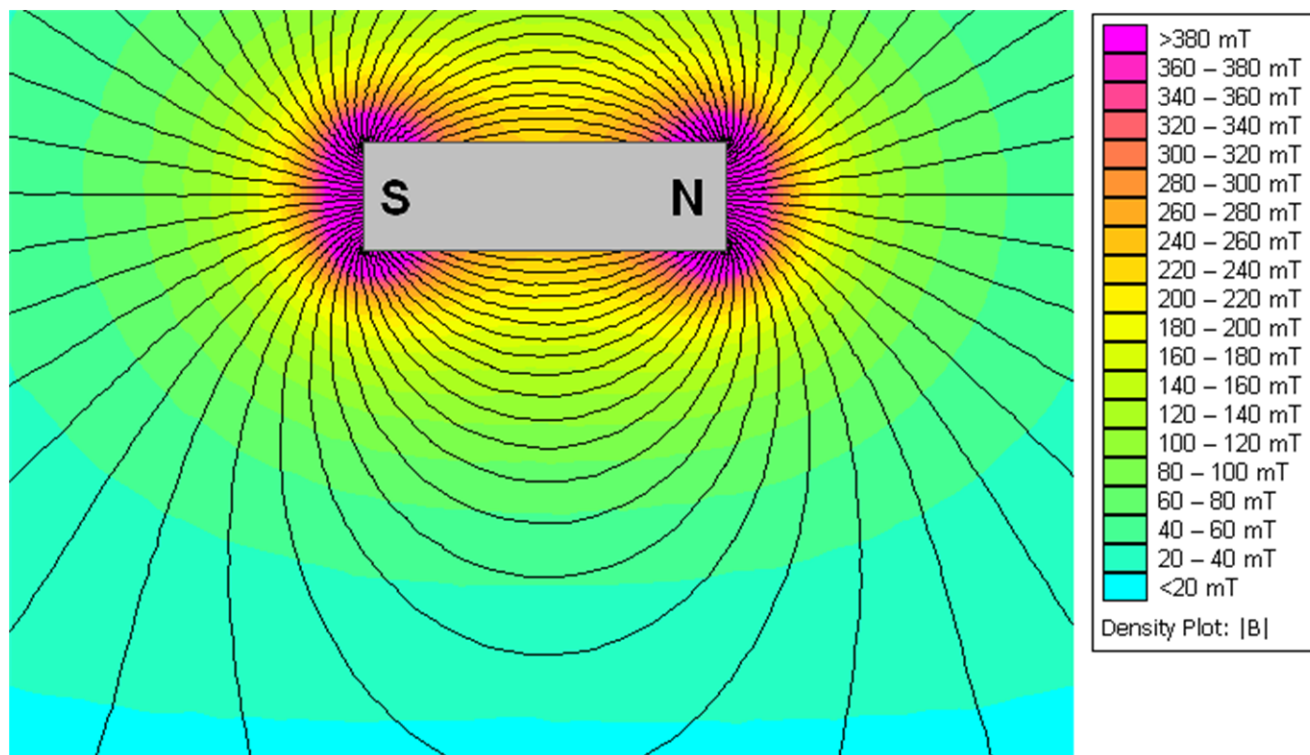


Figure 15. Simulated Magnetic Flux

8.3 Do's and Don'ts

Because the Hall element is sensitive to magnetic fields that are perpendicular to the top of the package, a correct magnet approach must be used for the sensor to detect the field. Figure 16 shows correct and incorrect approaches.

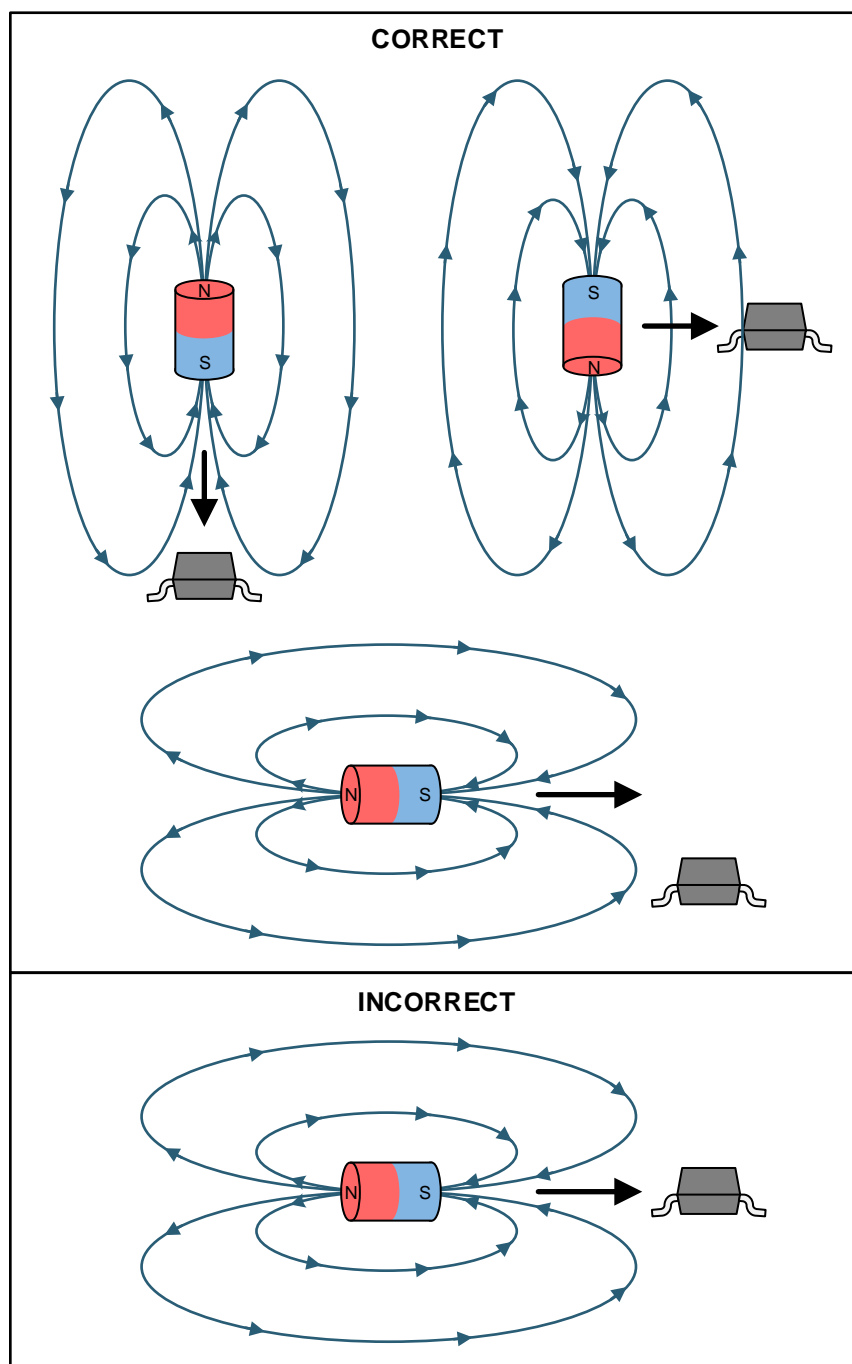


Figure 16. Correct and Incorrect Magnet Approaches

9 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 μF .

10 Layout

10.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed-circuit boards, which makes placing the magnet on the opposite side possible.

10.2 Layout Examples

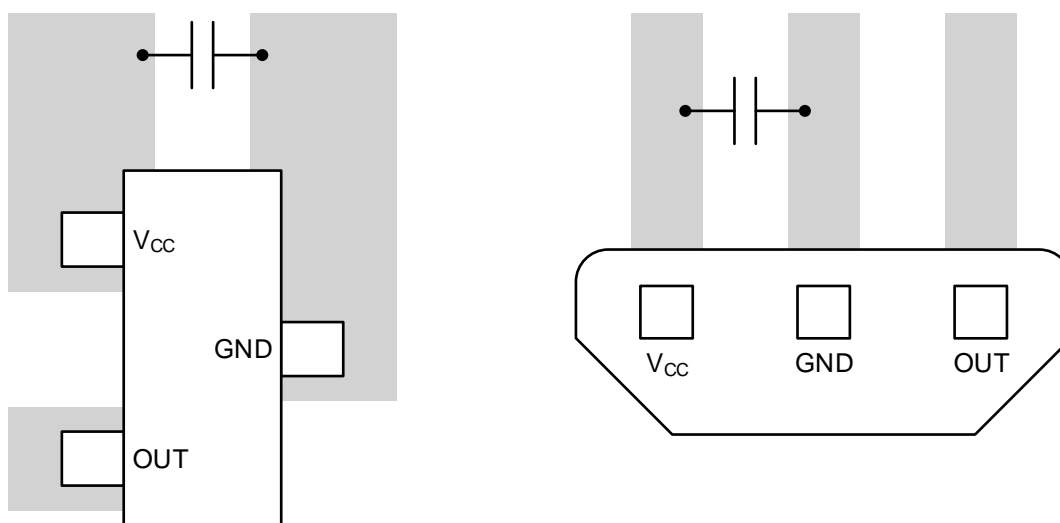


Figure 17. Layout Examples

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- [Using Linear Hall Effect Sensors to Measure Angle](#)
- [Incremental Rotary Encoder Design Considerations](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5055A1QDBZR	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	55A1	
DRV5055A1QDBZT	PREVIEW	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	55A1	
DRV5055A1QLPG	PREVIEW	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	55A1	
DRV5055A1QLPGM	PREVIEW	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	55A1	
DRV5055A2QDBZR	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	55A2	
DRV5055A2QDBZT	PREVIEW	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	55A2	
DRV5055A2QLPG	PREVIEW	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	55A2	
DRV5055A2QLPGM	PREVIEW	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	55A2	
DRV5055A3QDBZR	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	55A3	
DRV5055A3QDBZT	PREVIEW	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	55A3	
DRV5055A3QLPG	PREVIEW	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	55A3	
DRV5055A3QLPGM	PREVIEW	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	55A3	
DRV5055A4QDBZR	PREVIEW	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125	55A4	
DRV5055A4QDBZT	PREVIEW	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	55A4	
DRV5055A4QLPG	PREVIEW	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	55A4	
DRV5055A4QLPGM	PREVIEW	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	55A4	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV5055 :

- Automotive: [DRV5055-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

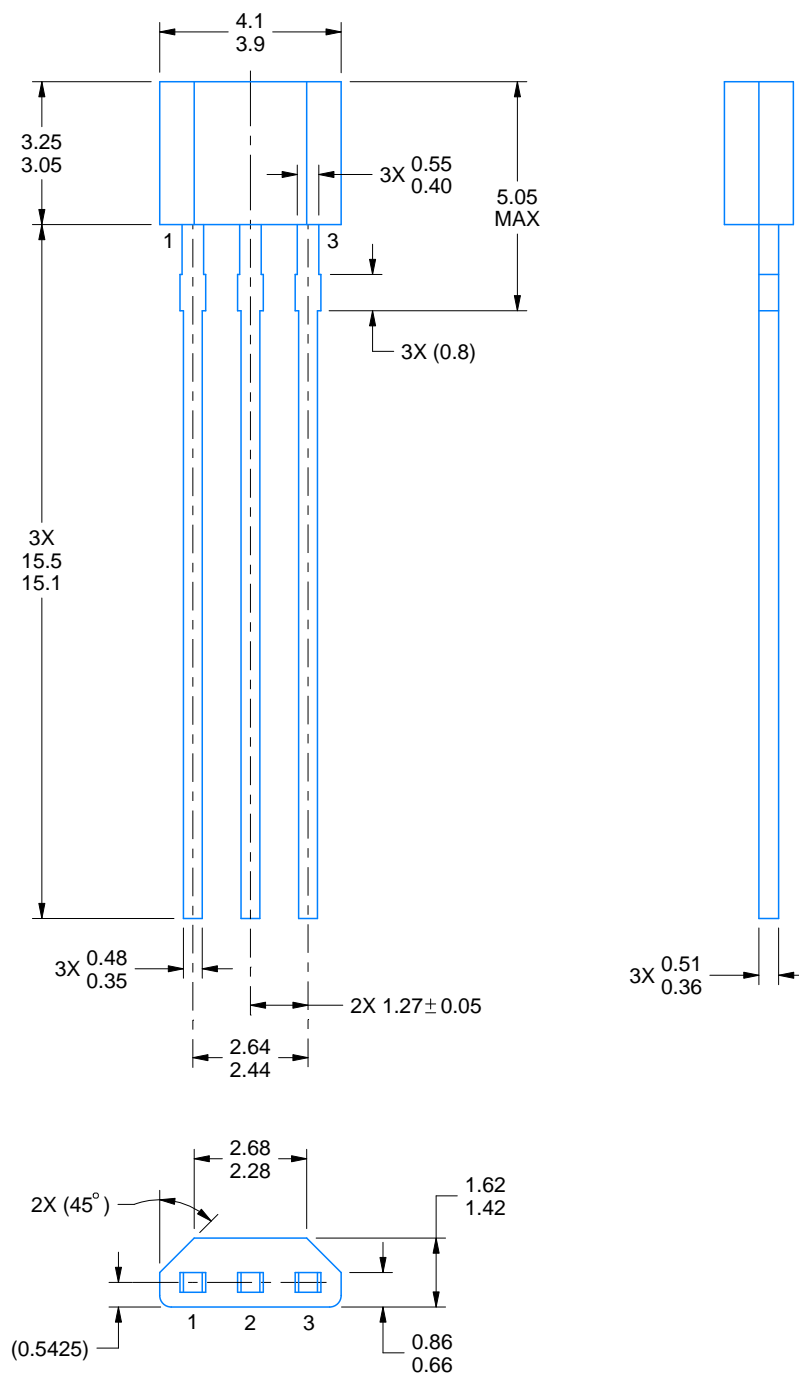
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5055A1QDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A1QDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A2QDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A2QDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A3QDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A3QDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A4QDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5055A1QDBZR	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A1QDBZT	SOT-23	DBZ	3	250	213.0	191.0	35.0
DRV5055A2QDBZR	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A2QDBZT	SOT-23	DBZ	3	250	213.0	191.0	35.0
DRV5055A3QDBZR	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A3QDBZT	SOT-23	DBZ	3	250	213.0	191.0	35.0
DRV5055A4QDBZT	SOT-23	DBZ	3	250	213.0	191.0	35.0



4221343/C 01/2018

NOTES:

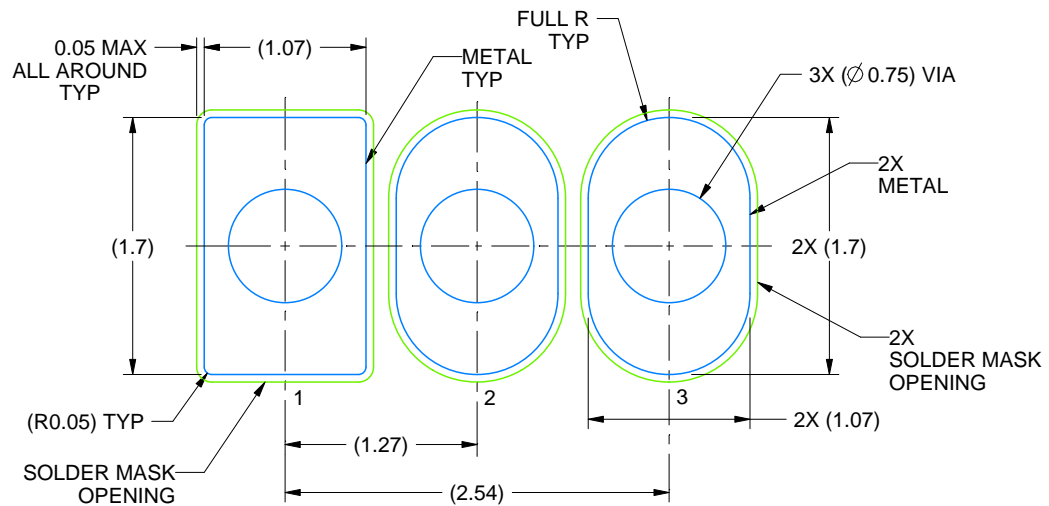
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

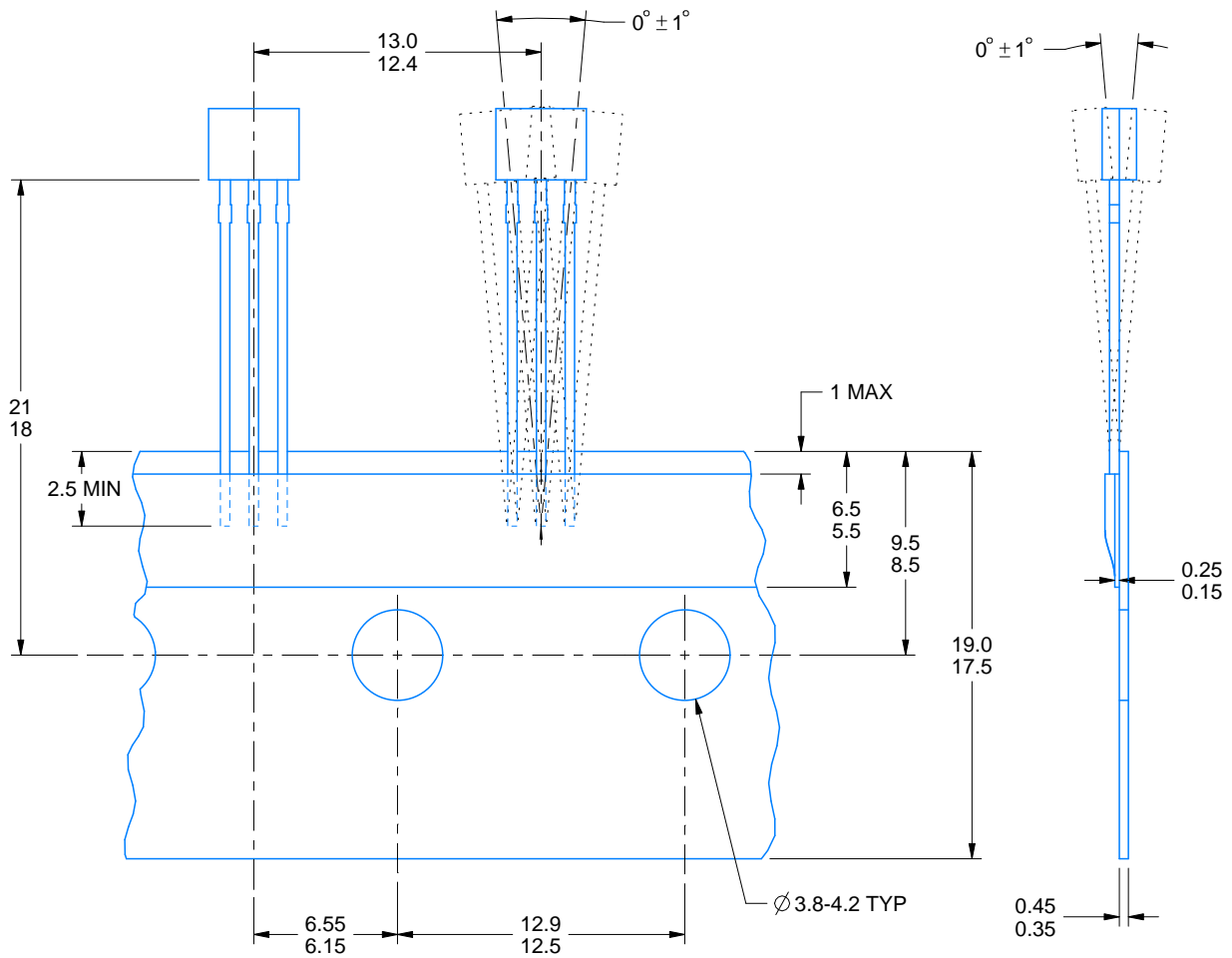
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



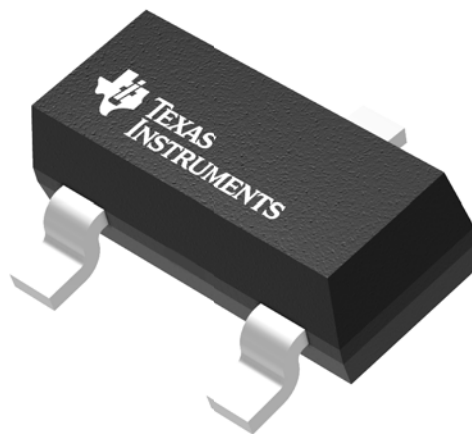
4221343/C 01/2018

GENERIC PACKAGE VIEW

DBZ 3

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203227/C

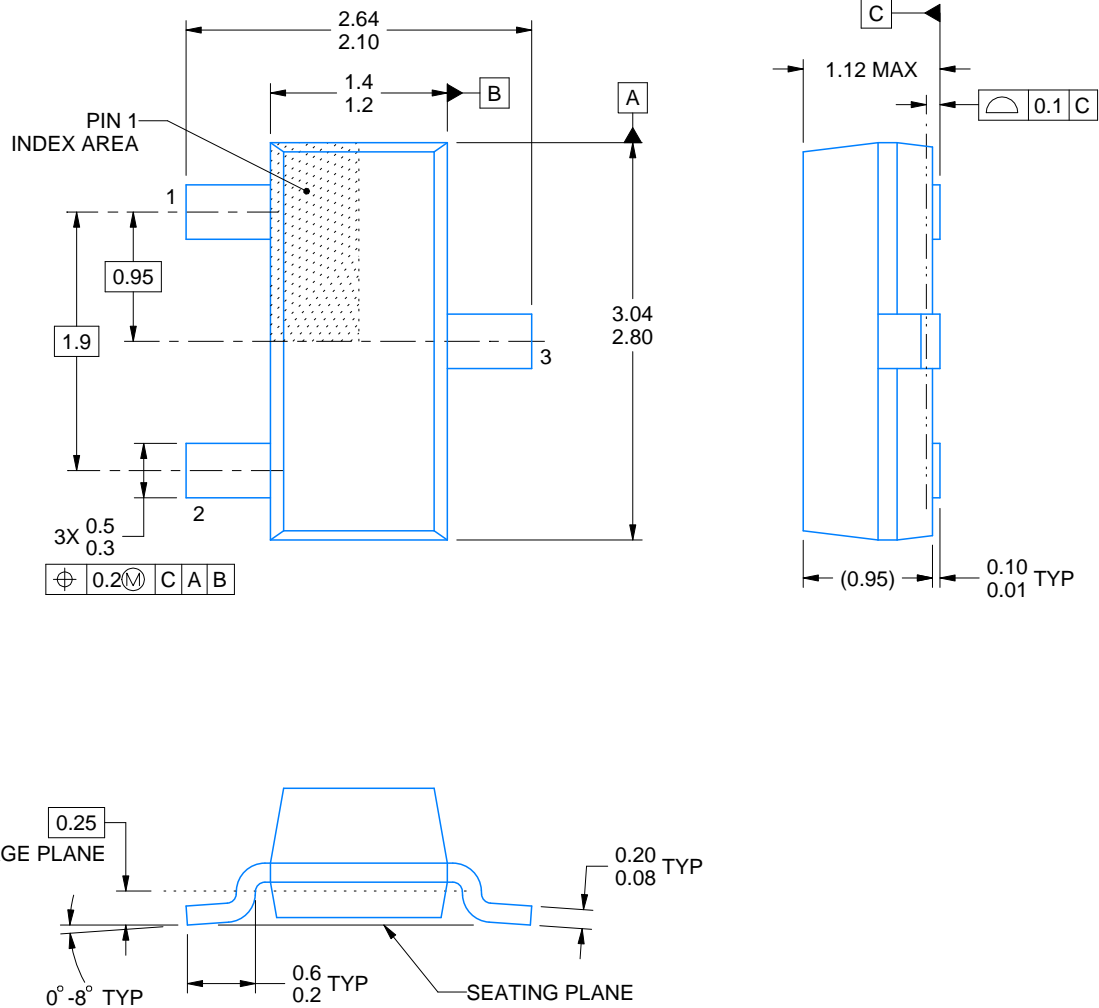
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

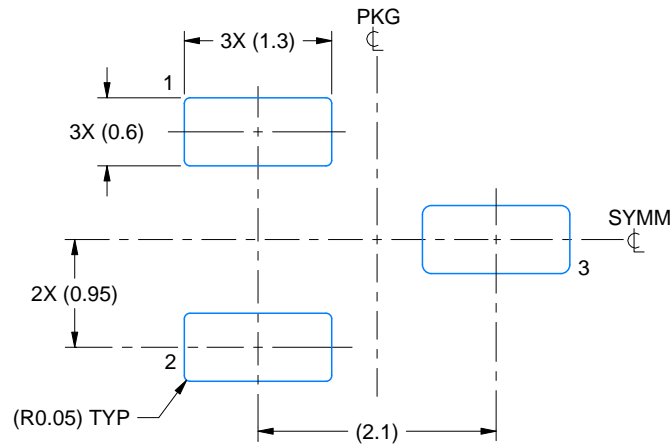
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

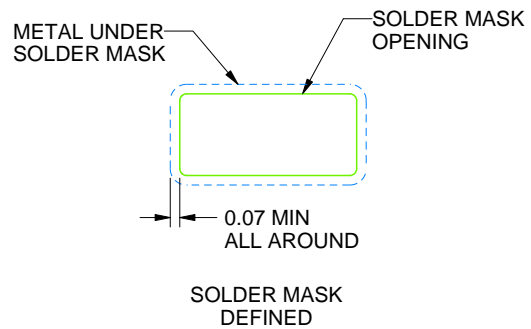
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

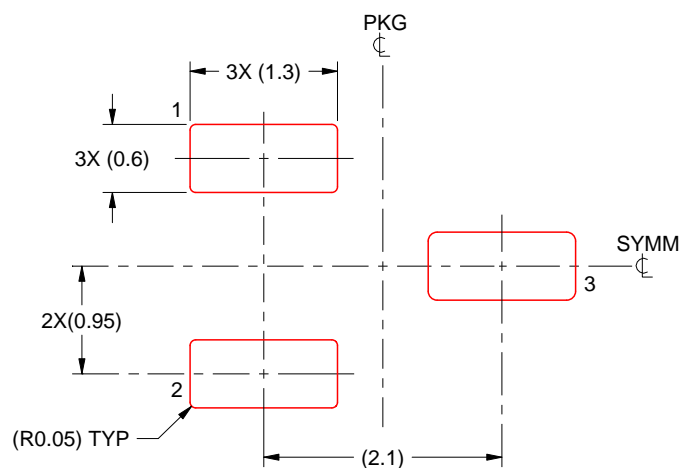
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.