UCC24610 GREEN Rectifier™ Controller Device

1 Features

- Secondary-Side Controller Optimized for 5-V Systems
- Up to 600-kHz Operating Frequency
- V_{DS} MOSFET-Sensing
- 1.6-Ω Sink, 2.0-Ω Source Gate-Drive Impedances
- Micro-Power Sleep Current for 90+ Designs
- Automatic Light-Load Management
- Synchronous Wake-Up From Sleep and Light-Load Modes
- Protection Features on Programming Inputs
- SYNC Input for CCM Operation
- 20-ns Typical Turnoff Propagation Delay
- Improved Efficiency and Design Flexibility Over Traditional Diode Solution
- May Be Biased Directly From 5-V Output
- Minimal Component Count

2 Applications

- AC-to-DC 5-V Adapters
- 5-V Bias Supplies
- Low Voltage Rectification Circuits
- Flyback and LLC Converters

3 Description

This GREEN Rectifier™ controller is a high-performance controller and driver for standard and logic-level N-channel MOSFET power devices used for low-voltage secondary-side synchronous rectification.

The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also indirectly reduces primary-side losses as well, due to compounding of efficiency gains.

Using drain-to-source voltage sensing, the UCC24610 is ideal for Flyback and LLC-resonant power supplies but can also be used with other power architectures. The UCC24610 is optimized for output voltages from 4.5 V to 5.5 V, and is suitable for use with lower and higher output voltages as well.

The UCC24610 offers a programmable false-triggering filter, a programmable timer to automatically switch to light-load mode at light load, and a SYNC input for optional use in continuous conduction mode (CCM) systems. Protection features on TON and EN/TOFF pins prevent run-away on-time due to open-circuit or short-circuit fault conditions.

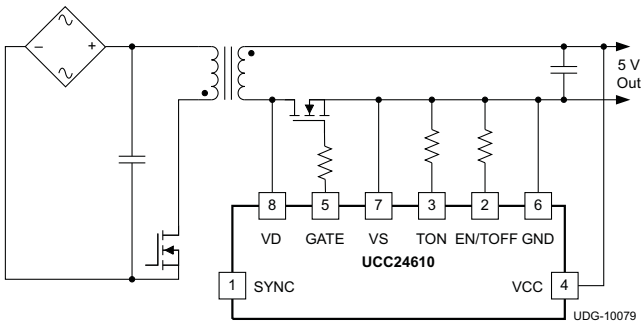
This device is available in an 8-pin SOIC package and an 8-pin, 3.0-mm × 3.0-mm SON package with an exposed thermal pad.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC24610DRB	SON (8)	3.00 mm × 3.00 mm
UCC24610D	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Flyback Topology



LLC-Resonant Half Bridge

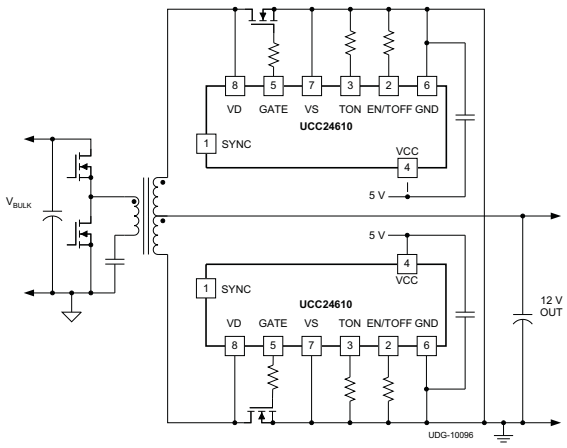


Table of Contents

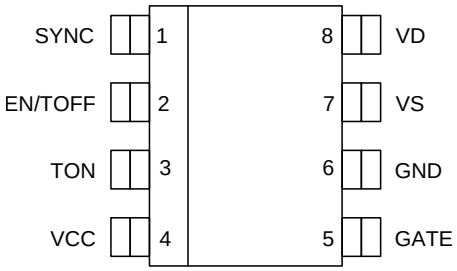
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

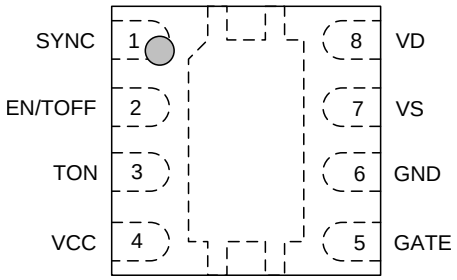
Changes from Revision B (September 2010) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



DRB Package
8-Pin SON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN/TOFF	2	I	EN/TOFF (combined enable function and programmable off-time timer), when VCC falls below the $V_{CC(off)}$ threshold, the UCC24610 is in UVLO mode, the EN/TOFF input is internally connected to GND through a 10-kΩ resistance and the internal current source is turned off. When VCC exceeds the $V_{CC(on)}$ threshold, the 10-kΩ resistance is removed and the current source is turned on. Thereafter, when EN/TOFF exceeds $V_{EN(on)}$, the UCC24610 is in run mode and when EN/TOFF falls below $V_{EN(off)}$, the UCC24610 is in sleep mode. The voltage level on EN/TOFF also programs the minimum off-time (T_{OFF}) for the controlled MOSFET. EN/TOFF is internally driven by a two-level current source, so the voltage level on EN/TOFF can be set by connecting a resistor from EN/TOFF to GND. The EN/TOFF current source initially drives twice as much current ($I_{EN-START}$) to achieve the enable threshold voltage $V_{EN(on)}$, and then drops to the normal run mode level (I_{EN-ON}) to program the T_{OFF} time. Alternatively, the desired EN/TOFF voltage may be forced using an external source. The T_{OFF} time is programmed to suppress GATE output for a desired duration to avoid possible false retriggering from resonant ringing or noise after turnoff. The T_{OFF} timer is triggered when VD voltage exceeds 1.5 V after GATE transitions from high to low.
GATE	5	O	GATE (controlled MOSFET gate drive), connect GATE to the gate of the controlled MOSFET through a small series resistor using short PC board tracks to achieve optimal switching performance. The GATE output can achieve >1-A peak source current when High and >2-A peak sink current when Low into a large N-channel power MOSFET. In sleep mode and UVLO, GATE impedance to GND is about 1.6 Ω. GATE impedance to GND crests about 80 Ω, when VCC ≈ 1.1 V.
GND	6	–	GND (combined analog and power ground), this ground input is the reference potential for the GATE driver, the UVLO comparator, the EN/TOFF comparator, the EN/TOFF timer, and the TON timer. Connect a 0.1-µF or larger ceramic bypass capacitor from the VCC pin to the GND pin through very short PC-board tracks.
SYNC	1	I	SYNC (gate turnoff synchronization), a falling edge on SYNC immediately forces GATE low, turning off the controlled MOSFET asynchronous to the voltage on the drain and source, and regardless of the state of the TON timer. When a power converter is operated in continuous conduction mode (CCM), it is necessary to turn off the controlled MOSFET under command of the switching converter. Connect SYNC to a control signal on the primary side of the converter using a high-voltage isolation capacitor or transformer, or other suitable coupling means. A continuous low level on the SYNC input causes GATE to be driven low for the same duration.
TON	3	I	TON (programmable on-time timer), program the minimum on time with a resistor from TON to GND. When the controlled MOSFET gate is turned on, some ringing noise is generated. The minimum on-time timer blanks the VD-VS comparator, keeping the controlled MOSFET on for at least the programmed minimum time. This time also determines the light-load shut-down point. If VD-VS falls below the –5-mV threshold before TON time expires, the controller transitions into light-load mode on the next switching cycle. When VD-VS falls below the –5-mV threshold after TON expires, the device resumes run-mode operation on the next switching cycle.
VCC	4	I	VCC (positive power input), connect a DC power voltage to VCC. Bypass VCC to GND with a 0.1-µF or larger ceramic capacitor using short PC board tracks. VCC supplies power to all circuits in the UCC24610. Under-Voltage Lockout (UVLO) comparators prevent operation until VCC rises above $V_{CC(on)}$. VCC can be used to safely turn off the UCC24610 by pulling VCC below $V_{CC(off)}$. In the event that VCC drops below $V_{CC(off)}$, GATE immediately falls Low and EN/TOFF is internally connected to GND with a 10-kΩ resistance.
VD	8	I	VD (drain-sense voltage), connect this pin as close as possible to the controlled MOSFET drain pad through a short PC board track, to minimize the effects of trace inductance on VD. VD must be >1.5 V and the TOFF timer must be expired before the device may be armed to allow the controlled MOSFET to be turned on the next switching cycle. Once armed, the controlled MOSFET is turned on (GATE goes High) when VD falls more than –150 mV below VS. At that threshold, the GATE output goes High and the TON timer is triggered. GATE remains High at least as long as the programmed TON time has not expired, unless a pulse at the SYNC input is detected. After TON has expired, the GATE output is turned off when VD-VS voltage decreases to –5 mV. If VD-VS decreases to –5 mV before TON expires, the controller enters light-load mode and the GATE pulse for the next switching cycle is suppressed. When the VD voltage increases to 1.5 V, the TOFF timer is triggered and the GATE output is prevented from turning on during the TOFF interval.
VS	7	I	VS (source-sense voltage), connect this pin as close as possible to the controlled MOSFET source pad through a short PC-board track, to minimize the effects of trace inductance on VS.
Thermal Pad		–	Thermal Pad on SON package only, the exposed thermal pad on the bottom of the SON package enhances the thermal performance of the device, and is intended to be soldered to a heat-dissipating pad on the PCB. This pad should be connected to the GND pin, or may be left floating (unconnected to any network). It is internally connected to GND through an indeterminate impedance and so may not be used to carry current.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage (2)	VCC	–0.3	6.5	V
	EN/TOFF (3)	–0.3	VCC	V
	TON (4)	–0.3	VCC	V
	VD for I_{VD} ≤ –10 mA	–1.0	50	V
	VS for I_{VS} ≤ –10 mA	–1.0	0.5	V
Input current, peak	SYNC (5) pulsed, t_{PULSE} ≤ 4 ms, duty cycle ≤ 1%		±100	mA
Output current, peak	GATE (6) pulsed, t_{PULSE} ≤ 4 ms, duty cycle ≤ 1%		±3	A
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltages more negative than indicated may exist on any listed pin without excess stress or damage to the device if the pin's input current magnitude is limited to less than -10mA. See separate ratings for SYNC and GATE pins.
(3) EN/TOFF can be driven by a voltage within the specified absolute maximum range or connected to a resistor to ground. Either method will program maximum off-time. When programmed by a resistor to GND, the voltage at the EN/TOFF terminal is internally limited to <VCC regardless of resistor value, so no absolute maximum input voltage considerations are required.
(4) In normal use, TON is connected to a resistor to GND. TON is normally not connected to a voltage source. When TON is connected to ground through a resistor, no absolute maximum input voltage considerations are required.
(5) In normal use, SYNC is connected with a capacitor to a high-speed voltage-transition source. The capacitor value shall be selected in conjunction with the worst-case voltage slew-rate to insure that the current into or out of SYNC is not in excess of the SYNC absolute maximum input current rating, or a current-limiting series resistor may also be necessary. In this use, if the input current is limited to less than the absolute maximum, no absolute maximum input voltage considerations are required. The capacitor breakdown voltage shall be selected to insure that dangerous voltage is not applied to the UCC24610. Continuous SYNC current is subject to the maximum operating junction temperature limitation.
(6) In normal use, GATE is connected to the gate of a power MOSFET through a small resistor. When used this way, GATE current is limited by the UCC24610 and no absolute maximum output current considerations are required. The series resistor shall be selected to minimize overshoot and ringing due to series inductance of the GATE output and power-MOSFET gate-drive loop. Continuous GATE current is subject to the maximum operating junction temperature limitation.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2,000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	VCC input voltage	4.5		5.5	V
C_{VCC}	VCC bypass capacitor	0.1			µF
T_J	Junction temperature	–40		125	°C
f_S	Switching frequency	20		600	kHz
R_{TON}	TON-to-GND resistor	10		261	kΩ
$R_{EN/TOFF}$	EN/TOFF-to-GND resistor	93		280	kΩ
t_{MIN}	SYNC minimum pulse width at V_{THSYNC} – 0.1 V	20			ns

6.4 Thermal Information

THERMAL METRIC(1)		UCC24610		UNIT
		DRB (SON)	D (SOIC)	
		9 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.3	115.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	59.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.5	54.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	13.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.7	53.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *the Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At VCC = 5 V_{DC}, C_{GATE} = 0 pF, R_{TON} = 200 kΩ, $R_{EN/TOFF}$ = 100 kΩ, −40°C ≤ T_J = T_A ≤ +125°C, all voltages are with respect to GND, and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY						
ICC_{START}	VCC current, undervoltage	VCC = 4.05 V		70	100	µA
ICC_{STBY}	VCC current, disabled	VCC = 5.5 V, $R_{EN/TOFF}$ = 0 Ω		130	200	µA
ICC_{ON}	VCC current, enabled	VCC = 5.5 V, $R_{EN/TOFF}$ = 100 kΩ	1.40	2.15	2.80	mA
VEN_{ON}	EN/TOFF turnon threshold, rising	EN/TOFF driven, ICC > 1 mA	1.31	1.40	1.49	V
VEN_{OFF}	EN/TOFF turnoff threshold, falling	EN/TOFF driven, ICC < 200 µA	0.74	0.80	0.86	V
$I_{EN-START}$	EN/TOFF input current, disabled	EN/TOFF = 1.3 V, rising from zero	–21.5	–20.0	–18.5	µA
I_{EN-ON}	EN/TOFF input current, enabled	EN/TOFF = 2 V	–10.7	–10.0	–9.3	µA
UNDERVOLTAGE LOCKOUT (UVLO)						
VCC_{ON}	VCC turnon threshold	Turnon detected by V_{EN} > 1.0 V	4.15	4.40	4.65	V
VCC_{OFF}	VCC turnoff threshold	Turnoff detected by V_{EN} < 0.5 V	3.96	4.20	4.44	V
VCC_{HYST}	UVLO hysteresis	VCC_{HYST} = VCC_{ON} – VCC_{OFF}	0.15	0.20	0.25	V
MOSFET VOLTAGE SENSING						
V_{THARM}	GATE rearming threshold	VD to GND, rising	1.3	1.5	1.7	V
V_{THON}	GATE turnon threshold	(VD – VS) falling, VS = 0 V	–220	–150	–80	mV
V_{THOFF}	GATE turnoff threshold	(VD – VS) rising, VS = 0 V	–8	–5	–2	mV
I_{DH}	VD input bias current, high	VD = 50 V, VS = 0 V		0.05	2.00	µA
I_{DL}	VD input bias current, low	VD = -0.15 V, VS = 0 V	–250	–150	–50	µA
I_S	VS input bias current	VD = 0 V, VS = 0 V	–250	–150	–50	µA
GATE DRIVER						
r_{GUP}	GATE pullup resistance, enabled	I_{GATE} = –100 mA		2.0	3.6	Ω
r_{GDN}	GATE pulldown resistance, enabled	I_{GATE} = 100 mA		1.6	2.5	Ω
V_{OHG}	GATE output high voltage	I_{GATE} = –100 mA	4.64	4.80		V
V_{OLG}	GATE output low voltage	I_{GATE} = 100 mA		0.16	0.25	V
V_{OLGUV}	GATE output low voltage, UV	I_{GATE} = 25 mA, VCC = 0 V		0.70	0.90	V
V_{OLGOFF}	GATE output low voltage, disabled	I_{GATE} = 25 mA, V_{EN} = 0 V		0.04	0.10	V
SYNCHRONIZATION						
V_{THSYNC}	SYNC falling threshold	GATE output transitions from high to low	VCC – 2.4	VCC – 2.0	VCC – 1.6	V
r_{SYNC}	SYNC pullup resistance	Internal resistance from SYNC to VCC	1.6	2.0	2.4	kΩ

6.6 Timing Requirements

At VCC = 5 V_{DC}, C_{GATE} = 0 pF, R_{TON} = 200 kΩ, $R_{EN/TOFF}$ = 100 kΩ, −40°C ≤ T_J = T_A ≤ +125°C, all voltages are with respect to GND, and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = +25°C.

		MIN	NOM	MAX	UNIT
MOSFET VOLTAGE SENSING					
t_{DON}	GATE turnon propagation delay, from V_{THON} to GATE > 1 V		44	70	ns
t_{DOFF}	GATE turnoff propagation delay, from V_{THOFF} to GATE < 4 V		16	35	ns
MINIMUM ON-TIME SETTING					
t_{ONLR}	Minimum on-time, low resistance, R_{TON} = 16.5 kΩ	0.17	0.25	0.33	µs
t_{ONHR}	Minimum on-time, high resistance, R_{TON} = 200 kΩ	2.2	3.0	3.8	µs
MINIMUM OFF-TIME SETTING					
t_{OFFLR}	Minimum off-time, low resistance, $R_{EN/TOFF}$ = 100 kΩ	4.94	7.80	9.86	µs
t_{OFFHR}	Minimum off-time, high resistance, $R_{EN/TOFF}$ = 261 kΩ	0.55	1.37	2.30	µs
t_{OFFLV}	Minimum off-time, low voltage, EN/TOFF = 1.0 V	4.94	7.80	9.86	µs
t_{OFFHV}	Minimum off-time, high voltage, EN/TOFF = 2.61 V	0.85	1.37	2.10	µs
t_{OFFOV}	Minimum off-time, over voltage, 3 V < V_{EN} < VCC	0.48	0.65	0.82	µs
GATE DRIVER					
t_{fGATE}	GATE rise time, from 1 V to 4 V, C_{GATE} = 3300 pF		14	30	ns
t_{rGATE}	GATE fall time, from 4 V to 1 V, C_{GATE} = 3300 pF		9	25	ns
t_{DIS}	Disable delay, from EN falling to GATE falling	50	100	150	ns
SYNCHRONIZATION					
t_{SDLY}	SYNC propagation delay, from SYNC falling to GATE falling 10%		20	60	ns

6.7 Typical Characteristics

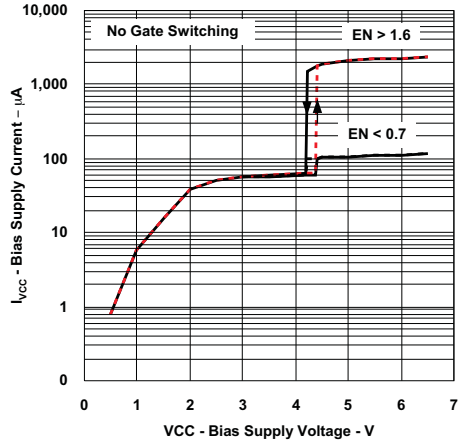


Figure 1. Bias Supply Current vs. Bias Supply Voltage

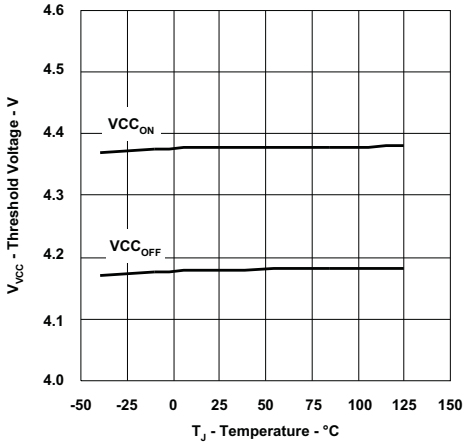


Figure 2. UVLO Threshold Voltage vs. Temperature

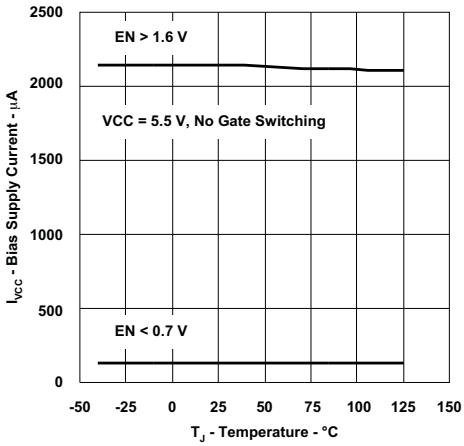


Figure 3. Bias Supply Current vs. Temperature

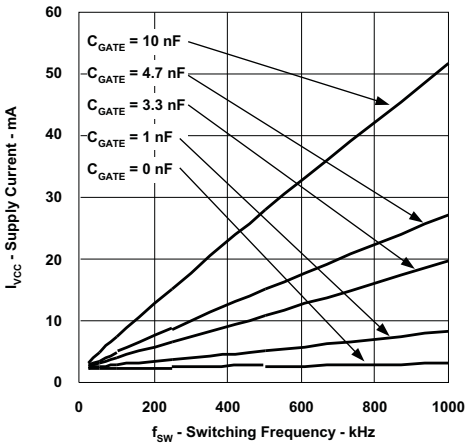


Figure 4. Supply Current vs. Switching Frequency

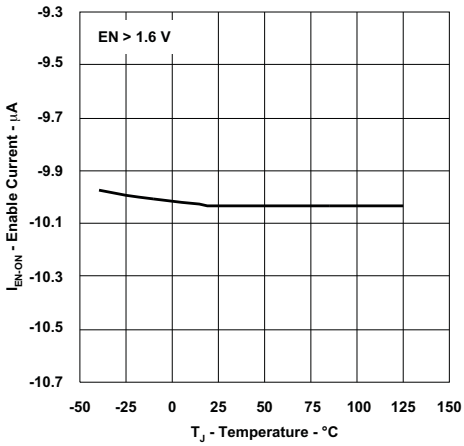


Figure 5. Enable Current vs. Temperature

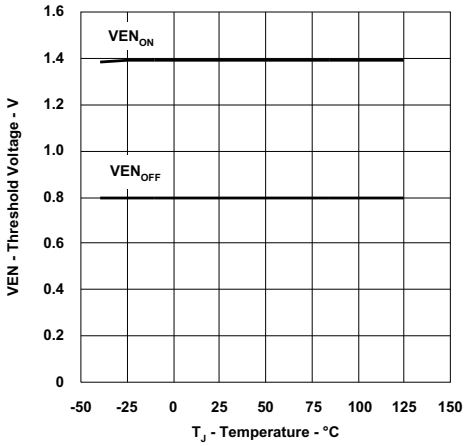


Figure 6. Enable Threshold Voltage vs. Temperature

Typical Characteristics (continued)

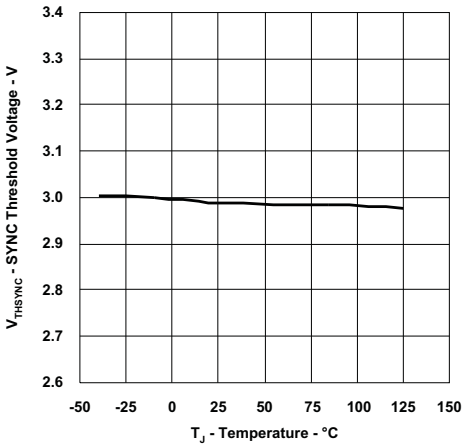


Figure 7. SYNC Threshold Voltage vs. Temperature

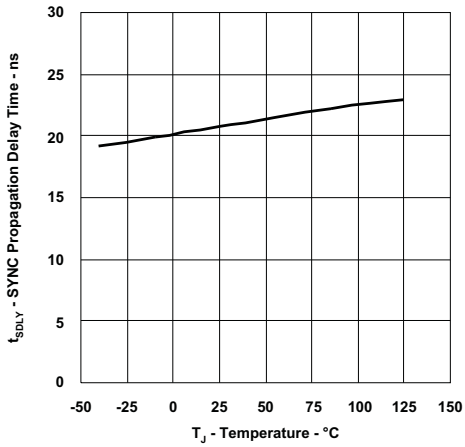


Figure 8. SYNC Propagation Delay Time vs. Temperature

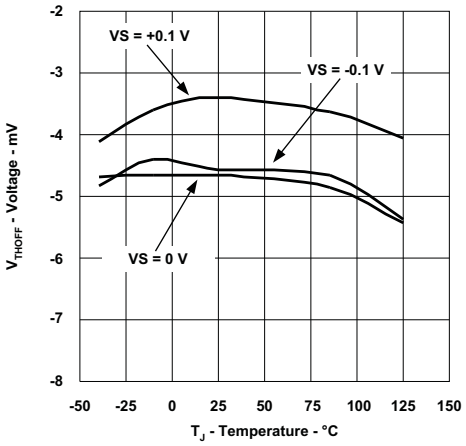


Figure 9. V_{DS} Gate-Off Threshold Voltages vs. Temperature

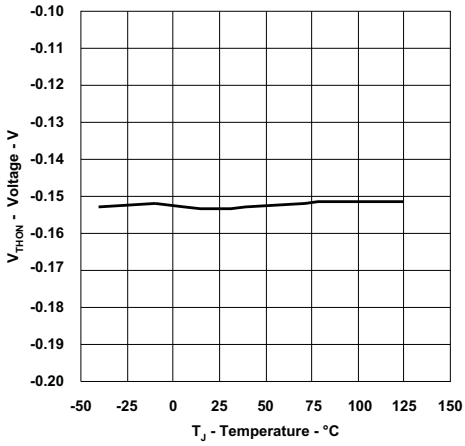


Figure 10. V_{DS} Gate-On Threshold Voltage vs. Temperature

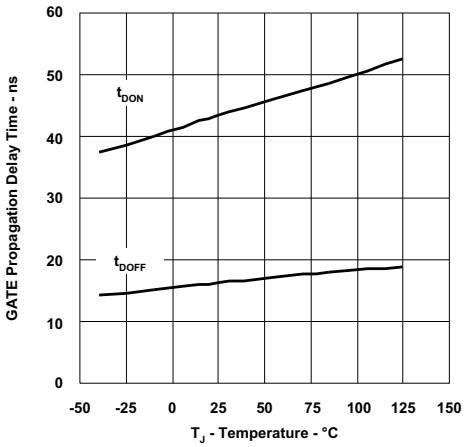


Figure 11. Gate Propagation Delay Time vs. Temperature

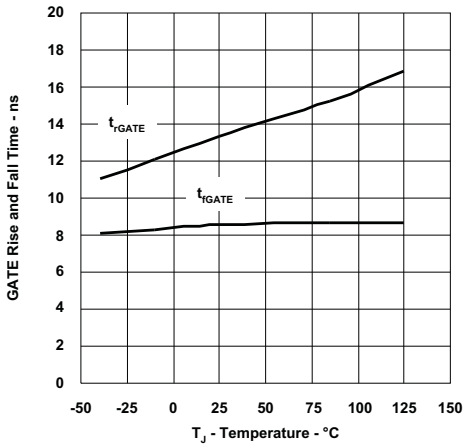


Figure 12. Gate Rise And Fall Time vs. Temperature

Typical Characteristics (continued)

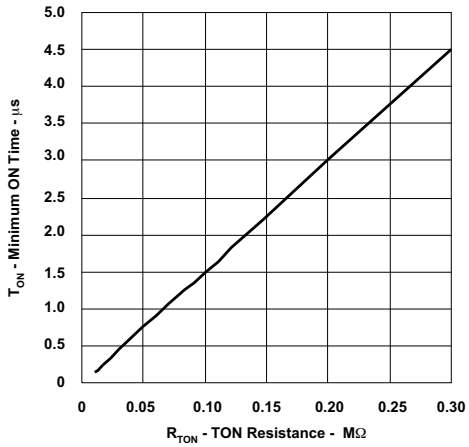


Figure 13. Minimum On Time vs. t_{ON} Resistance

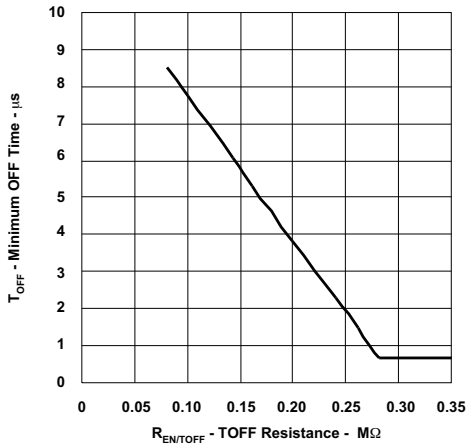


Figure 14. Minimum Off Time vs. t_{OFF} Resistance

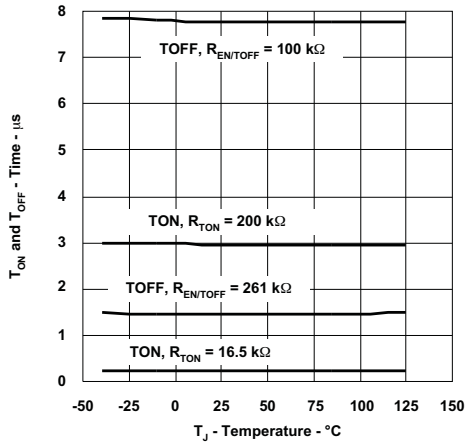


Figure 15. t_{ON} and t_{OFF} Time vs. Temperature

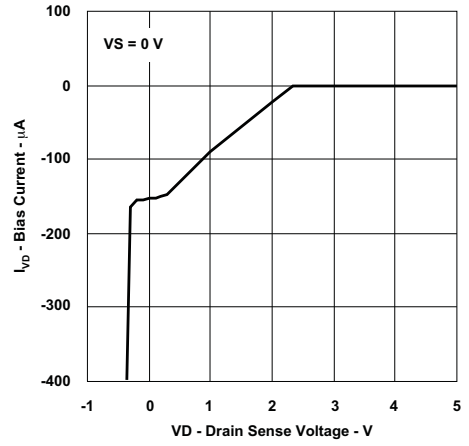


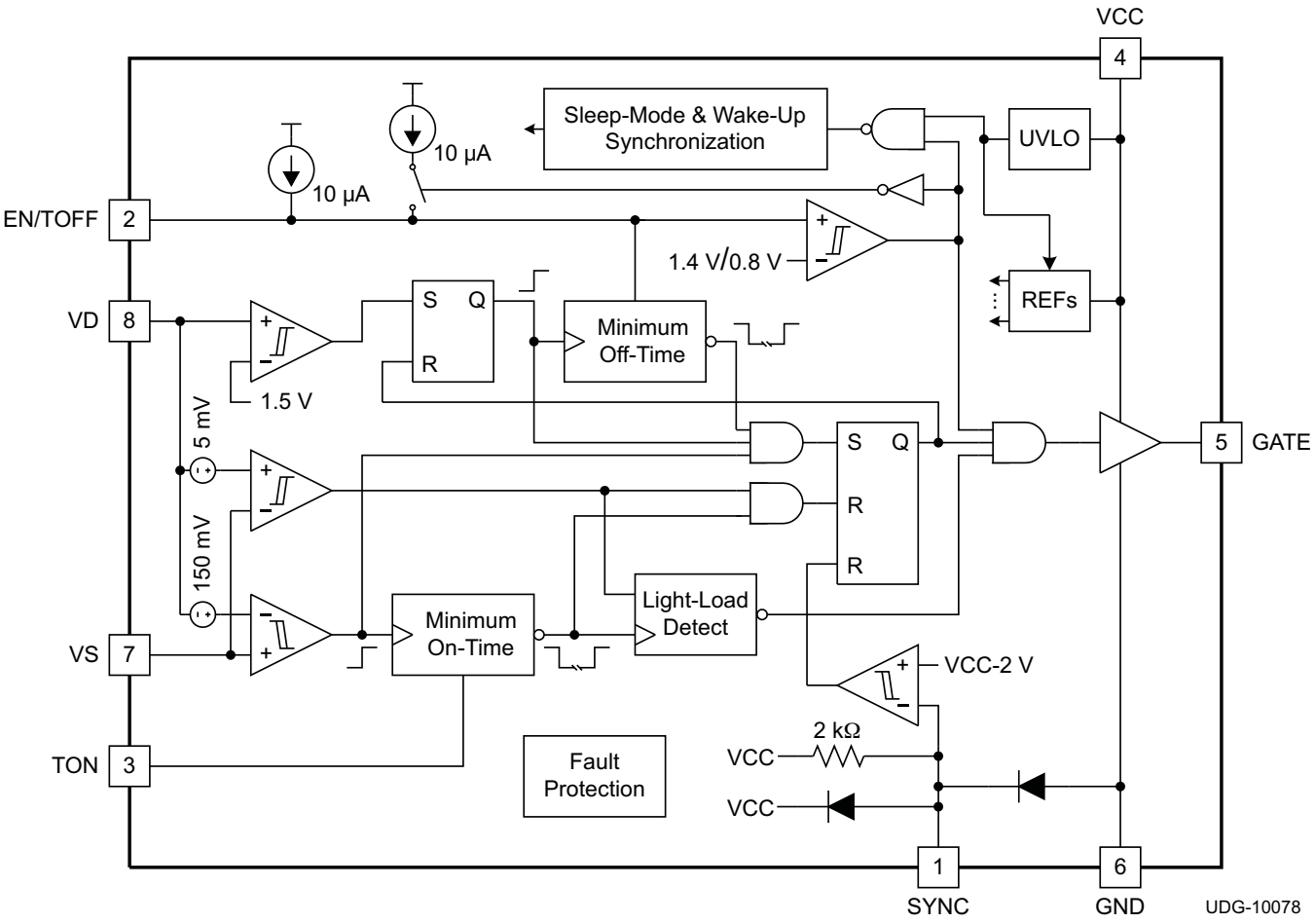
Figure 16. VD Bias Current vs. Drain Sense Voltage

7 Detailed Description

7.1 Overview

The UCC24610 synchronous rectifier (SR) controller uses drain-to-source voltage sensing to determine the SR MOSFET conduction interval. The SR MOSFET is turned on when V_{DS} exceeds –150 mV, and is turned off when V_{DS} diminishes to –5 mV or the SYNC input is triggered for CCM operation. Programmable minimum on-time and off-time helps avoid false turnon and turnoff responses to switch voltage ringing and noise. To reduce light-load switching losses, automatic light-load mode disables the GATE pulses when the actual on-time based on V_{DS} becomes less than the programmed minimum on-time. When the load increases such that the conduction time exceeds the programmed minimum on-time, the controller resumes normal SR operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Normal Operation

The UCC24610 GREEN rectifier synchronous-rectifier (SR) controller powers up into UVLO mode as VCC increases from 0 V. Enable current (I_{EN}) from the EN/TOFF pin is inhibited until VCC exceeds the $V_{CC(on)}$ threshold, and remains active as long as VCC exceeds the $V_{CC(off)}$ threshold. The voltage on the EN/TOFF pin determines whether the controller is enabled or not. The controller operates in the normal run mode when the enable voltage (VEN) exceeds the enable threshold $V_{EN(on)}$ and remains enabled as long as V_{EN} exceeds the $V_{EN(off)}$ threshold.

After the controller is enabled, V_{EN} programs the minimum off time inversely proportional to the voltage (see *Enabling and TOFF Programming*). The two-state enable current allows a lower-value resistance for $R_{EN(off)}$ (necessary to program longer off time) to still generate sufficient voltage to exceed $V_{EN(on)}$ at start-up. A simple resistor from EN/TOFF to GND generates V_{EN} based on the level of I_{EN} current flowing through it (see Figure 17). Alternatively, V_{EN} may be driven by an external voltage source provided this voltage exceeds $V_{EN(on)}$ for at least 100 ns before settling to its final programming level.

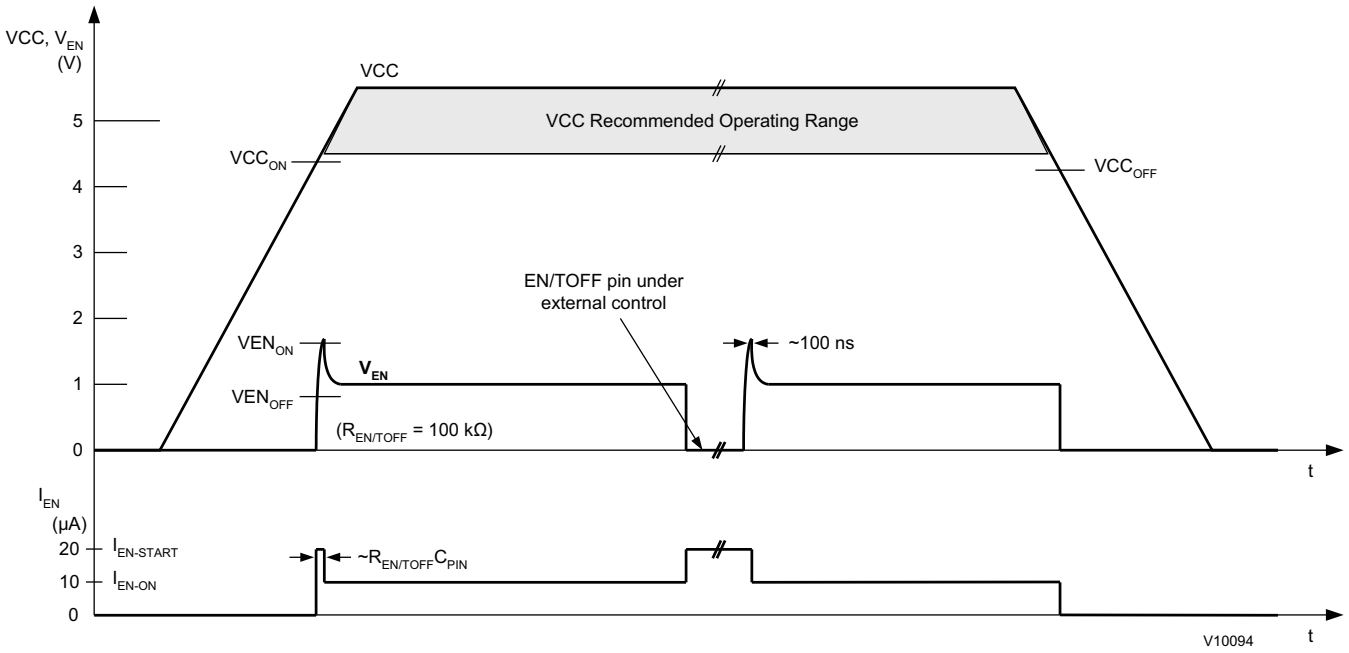


Figure 17. Behavior of I_{EN} and V_{EN} as VCC Varies ($R_{EN/TOFF}$ = 100 kΩ)

Feature Description (continued)

The UCC24610 SR controller determines the conduction time of the SR-MOSFET by comparing the drain-to-source voltage of the MOSFET against a turnon threshold and a turnoff threshold. The GATE output is driven high when V_{DS} of the MOSFET exceeds $V_{TH(on)}$ and is driven low when V_{DS} decreases below $V_{TH(off)}$ as illustrated in Figure 18.

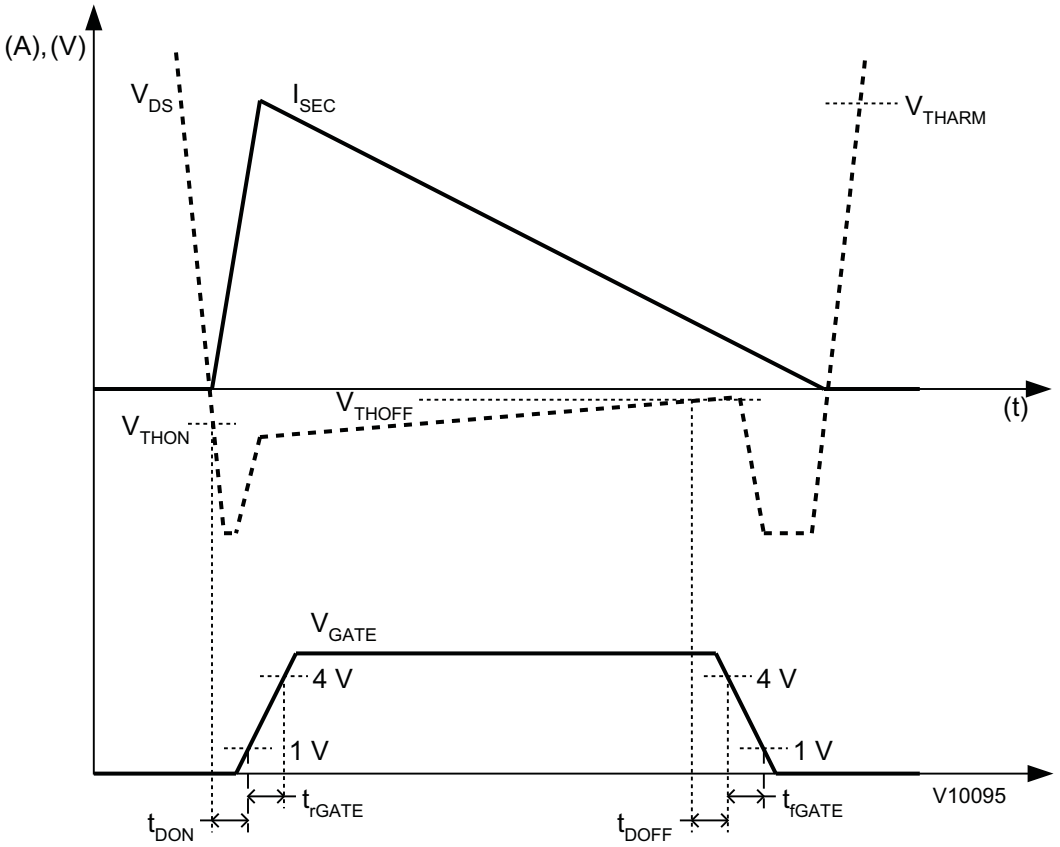


Figure 18. GATE Output With Respect to V_{DS}

NOTE

Because of finite propagation and rise times, the body diode of the SR-MOSFET may conduct briefly after $V_{TH(on)}$ has been exceeded. Also, the body-diode conducts the residual secondary current after $V_{TH(off)}$ has been crossed. A waveform similar to that of V_{DS} depicted in Figure 18 can be observed during SR operation in a simple flyback circuit.

Feature Description (continued)

However, actual in-circuit waveforms are rarely as clean as shown in Figure 18. Instead, parasitic inductances and capacitances set up resonant ringing at various inflection points in the waveforms. The UCC24610 has control timing and programming options that help avoid interference from such ringing with proper operation. Figure 19 shows more realistic waveforms and the internal control timing which accommodates them. The waveforms affecting the SR-MOSFET in a typical flyback circuit are shown.

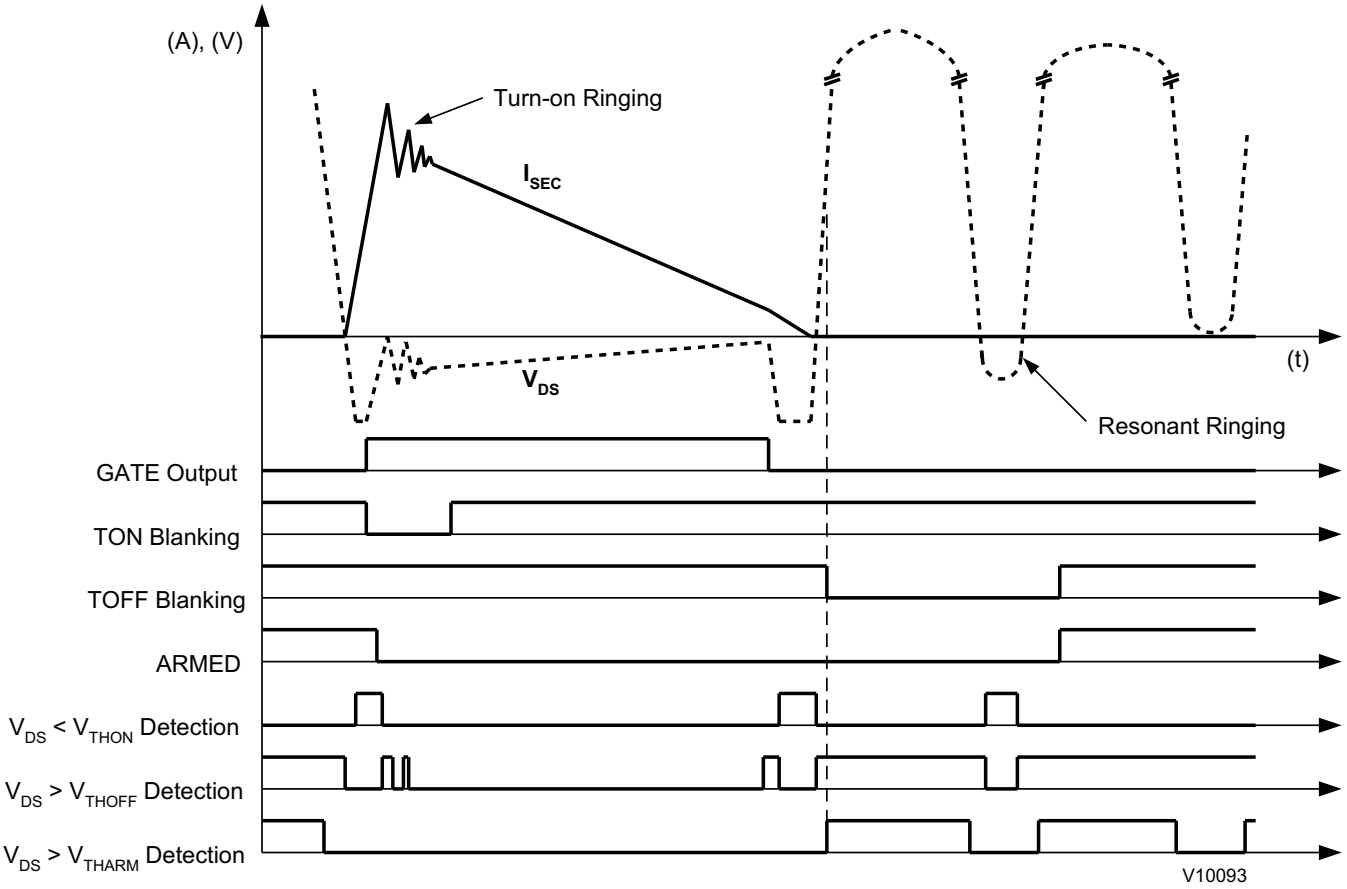


Figure 19. Internal Signal Timing With Respect to Realistic DCM Waveforms

Minimum on-time TON is programmed with a resistor from TON, (pin 3) to GND to blank the response of the turnoff detection circuit to prevent GATE from being turned off from spurious crossings of $V_{TH(off)}$ due to noise and ringing. TON is triggered by the GATE turning on. Refer to *TON Programming* for details.

Minimum off-time T_{OFF} is programmed with a resistor from pin 2 to GND to blank the response of the turnon detection circuit to prevent GATE from being turned-on again from spurious crossings of $V_{TH(on)}$ due to excessive C_{OSS} resonant ringing. TOFF is triggered by V_{DS} crossing V_{THARM} after the GATE turns off. Refer to the *Enabling and TOFF Programming* for details

The GATE output may only turn on when the controller has been *armed* for the switching cycle. The controller is armed for each successive SR cycle only after TOFF expires. In high-frequency applications, an excessively long TOFF may interfere with timely turn-on of GATE in the next switching cycle. GATE turn on will be delayed if TOFF from the previous cycle has not yet expired.

Feature Description (continued)

7.3.2 Light-Load Operation

During normal operation, the synchronous rectifier conduction time is longer than the programmed minimum on-time. If load current decreases enough that the SR conduction time becomes shorter than the programmed minimum on-time, a light-load condition is detected. The light-load latch is set and the next GATE output pulse is blanked, so only the body diode of the controlled MOSFET conducts. This comparison between SR conduction time and minimum on time occurs every switching cycle, regardless of whether the GATE output pulse is enabled or blanked. When load current increases enough that the body-diode conduction time becomes longer than the programmed minimum on time, the light-load latch is cleared and the next GATE output pulse is enabled and the controlled MOSFET resumes SR operation.

Figure 20 depicts the progression into light-load mode for a DCM flyback application as the load decreases, while Figure 21 depicts the reverse progression back to run mode.

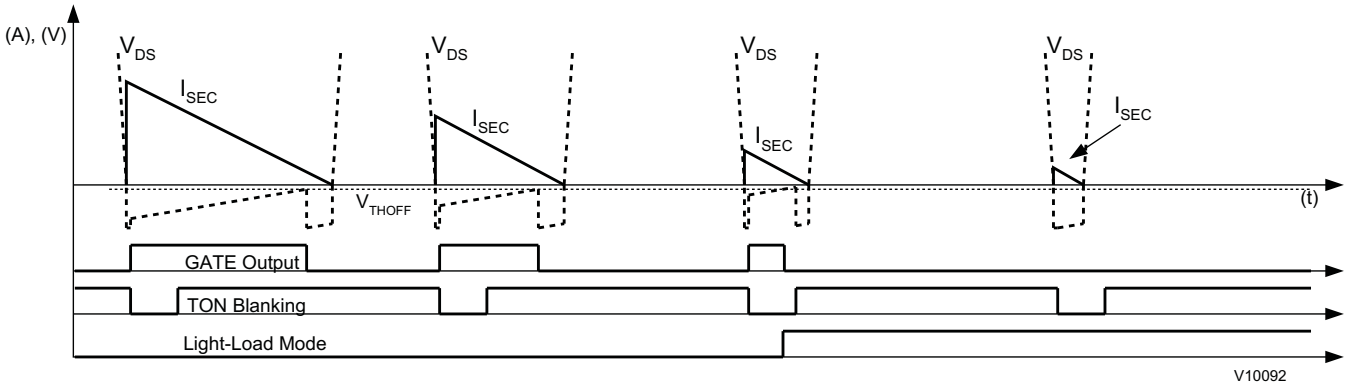


Figure 20. Decreasing Load Current Progression Leads to Light-Load-Mode Operation

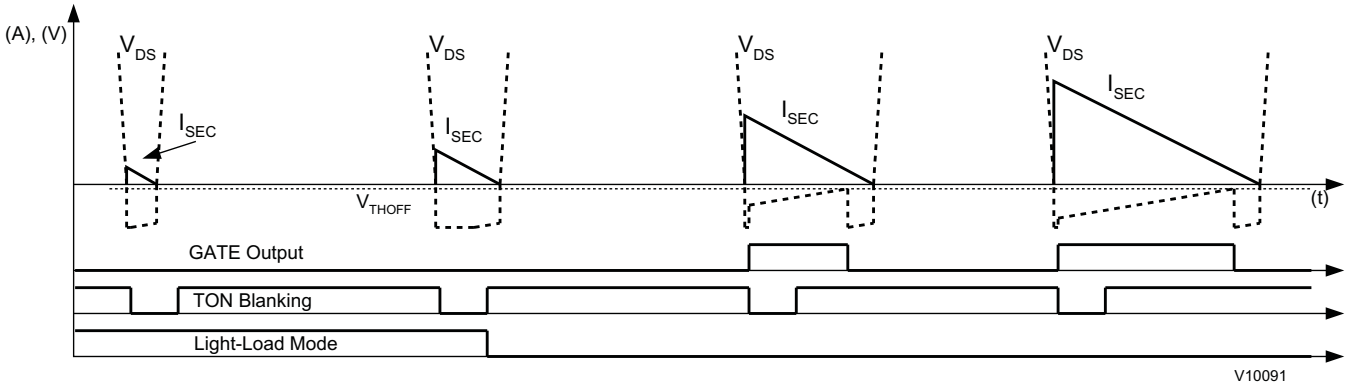


Figure 21. Increasing Load Current Progression Returns to Run-Mode Operation

7.4 Device Functional Modes

7.4.1 UVLO Mode

When the VCC voltage to the device has not yet reached the $V_{CC(on)}$ threshold, or has fallen below the UVLO threshold $V_{CC(off)}$, the device operates in the low-power UVLO mode. In this mode, most internal functions are disabled and ICC current is typically much less than 100 µA. While in this mode, the EN current source is shut off, an internal 10-kΩ resistance is applied from the EN/TOFF pin to GND, the voltage on EN/TOFF is irrelevant, and the GATE output is driven low continuously for all VCC > 1.2 V. The device passes out of UVLO mode when VCC increases above the $V_{CC(on)}$ threshold. UVLO mode is very similar to Sleep mode, except VCC current is at $I_{CC(start)}$ level.

7.4.2 Sleep Mode

Sleep mode is a low-power operating mode similar to UVLO mode, except that this mode is entered under external control by forcing V_{EN} below the $V_{EN(off)}$ threshold. Sleep mode may be used to reduce device operating losses to less than 1 mW. VCC current reduces to $I_{CC(stby)}$ level. External control overrides any internal timing conditions, and immediately forces the GATE output low and enters Sleep mode. Many internal circuits are turned off to reduce power consumption. When V_{EN} is restored to above the $V_{EN(on)}$ threshold, the device exits Sleep mode synchronously into Light-load mode after a delay of approximately 25 µs to allow re-powered internal circuits to settle.

7.4.3 Run Mode

Run mode is the normal operating mode of the controller when not in UVLO mode, sleep mode, or light-load mode. In this mode, VCC current is higher because all internal control and timing functions are operating and the GATE output is driving the controlled MOSFET for synchronous rectification. VCC current is the sum of $I_{CC(on)}$ plus the average current necessary to drive the load on the GATE output. GATE output duty-cycle is dependent upon system line and load conditions, programmed TON and TOFF times, and SYNC-pulse timing (if applicable).

7.4.4 Light-Load Mode

Light-load mode is a low-power operating mode similar to sleep mode, except that this mode is entered automatically based on internal timing conditions. Light-load mode automatically reduces switching losses under light-load conditions by suppressing GATE output pulses whenever the detected synchronous conduction time is less than the programmed minimum on-time (TON). VCC current reduces to $I_{CC(on)}$ level. While in light-load mode, the MOSFET body-diode conduction time is still continuously monitored. When this time is detected to once again exceed TON, the device resumes run mode on the next switching cycle.

7.4.5 Fault Mode and Other Protections

Fault mode is a self-protection operating mode of the controller when certain types of single-fault conditions are detected on certain pins. In this mode, the device enters a shut-down state (not sleep mode) and drives the GATE output low. Specifically, Fault mode is entered if R_{TON} > 301 kΩ or if R_{TON} < 8.7 kΩ. Fault mode prevents the conditions of excessive or indefinite on-time (such as from an open-pin) and of excessive TON current (such as from a shorted-pin).

Similar protection is provided for the EN/TOFF pin. While not specifically detected as faults, if this pin becomes open-circuited TOFF defaults to a minimum value of ≈0.65 µs, and if shorted-to-GND the device enters sleep mode. Additionally, if the SYNC input is continuously held below its trigger threshold voltage, the GATE output is held low for the entire duration that SYNC remains in that condition.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC24610 synchronous rectifier controller is optimized for 5-V only applications, but may be used for other applications (such as LLC converters) where device stresses (such as VD voltage) are not exceeded, and a 5-V VCC source is available.

The effects of lead inductance on the V_{DS}-sensing turnoff threshold varies with the SR MOSFET package. Compact packages such as SON, QFN, and similar packages have virtually no significant lead inductance in the drain connection, very little in the source, and nominal bond-wire inductance in the gate path. Slightly larger SOIC-derived packages may have 2-nH to 3-nH inductance in the source path. TO-220 and larger packages have significant lead inductances, which can adversely affect the turnoff point of the SR MOSFET unless the sensing is compensated for inductance. The falling dI/dt of the current through the SR lead inductance reduces the sensed V_{DS} voltage and prematurely triggers turnoff. Resistors in the VD and VS sense paths can be used to compensate for this effect.

8.2 Typical Application

The following application information is applied to the UCC24610 Evaluation Module (EVM), which delivers 5 A at 5 V using an SR MOSFET in a TO-220 package. In this DCM flyback-topology application example, the SYNC signal is not used. Performance data relevant to the operation of the UCC24610 SR controller are included in this section for application reference. Refer to *Using the UCC24610EVM-563* User's Guide (SLUU434) for additional details on the overall performance of the EVM. The schematic diagram for the EVM, Figure 22, is provided as an example of a typical application for the UCC24610.

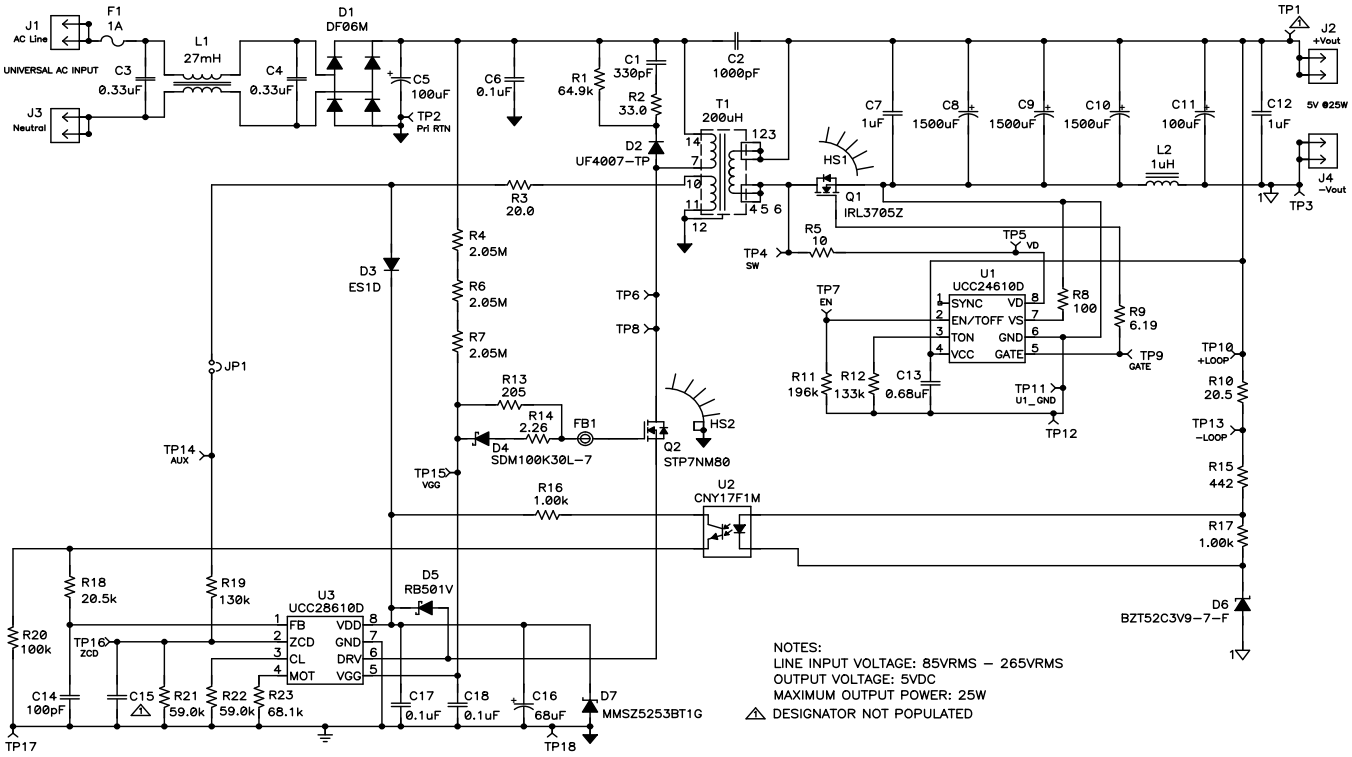


Figure 22. UCC24610 Typical Application Example

Typical Application (continued)

8.2.1 Design Requirements

Table 1. UCC24610 EVM Design Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		85		265	V_{RMS}
I_{IN}	Input current	V_{IN} = 115 V_{RMS}, I_{OUT} = 5 A		0.6		A_{RMS}
		V_{IN} = 115 V_{RMS}, I_{OUT} = 0 A		0.03		A_{RMS}
V_{UVLO}	Brown out	I_{OUT} = 5 A		69		V_{RMS}
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage, average	V_{IN} = 85 V_{RMS} to 265 V_{RMS}, I_{OUT} = 0 A to 5 A	4.5	5	5.6	V
V_{RIPPLE}	Output voltage, ripple	V_{IN} = 115 V_{RMS}, I_{OUT} = 5 A		200		mVpp
I_{OUT}	Output current	V_{IN} = 85 V_{RMS} to 265 V_{RMS}	0		5	A
I_{OCP}	Output overcurrent inception point	V_{IN} = 115 V_{RMS}		7		A
V_{OVP}	Output overvoltage protection point	I_{OUT} = 0 A to 5 A		6.5		V
	Transient response voltage over-shoot	V_{IN} = 115 V_{RMS}, I_{OUT} = 0 A to 5 A		600		mV
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency		26.3		140.4	kHz
η_{PEAK}	Peak efficiency	V_{IN} = 115 V_{RMS}, I_{OUT} = 1.75 A		82.7%		
η_{AVG}	Average efficiency	V_{IN} = 115 V_{RMS}, I_{OUT} = 25%, 50%, 75%, 100% of rated output current		82.3%		
		V_{IN} = 230 V_{RMS}, I_{OUT} = 25%, 50%, 75%, 100% of rated output current		82.3%		
	No-load power consumption	V_{IN} = 115 V_{RMS}, I_{OUT} = 0 A		181		mW
		V_{IN} = 230 V_{RMS}, I_{OUT} = 0 A		368		mW
	Operating temperature range	V_{IN} = 85 V_{RMS} to 265 V_{RMS}, I_{OUT} = 0 A to 5 A		25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 VD and VS Detection

VD and VS are differential inputs used to sense the voltage across the SR-MOSFET to determine when to turn on and off the GATE output. When the GATE is off, the controller will not drive the GATE on until VD has exceeded 1.5 V at least once and TOFF has expired. Once these two conditions are met, the controller is *armed* to allow the GATE to turn on the next time the drain voltage falls 150 mV below the source voltage (VD – VS = –150 mV). While the GATE is off, the SR-MOSFET may be blocking reverse current, or forward current may be building up in the MOSFET body diode. Normally this body-diode current would generate about 700 mV forward voltage drop (–700 mV_{DS}), but when –150 mV is detected the GATE is turned on to enhance the MOSFET into a synchronous rectifier. The GATE stays on for at least the minimum on time TON or longer until the SR-MOSFET current diminishes to near zero. When the current reduces sufficiently such that the V_{DS} voltage drop is only –5 mV, the GATE output is turned off. (It can be seen that the MOSFET $R_{DS(on)}$ determines the current level at which the GATE is turned off, which then further factors into determining the light-load mode inception point.) At the same time, the controller is *disarmed* to prevent spurious GATE output. Because the MOSFET current is not yet zero at GATE turn off, the V_{DS} will briefly increase back up to the body-diode drop, however the additional power loss is very small. The *disarmed* state of the controller prevents repeated turn on of the GATE (even though V_{DS} ≤150 mV again). Once the current does decrease to zero, the drain voltage climbs past the 1.5-V threshold, at which point the minimum off-time interval TOFF is triggered. Once V_{DS} has exceeded 1.5 V and TOFF has expired, the GATE circuit is *rearmed* to respond to the next turnon condition.

Because the VD and VS inputs are connected across the SR-MOSFET body diode by way of its package leads, the high secondary-side dI/dt through the lead inductances can impress excessive negative voltage on the VD pin. This negative voltage can disrupt normal controller operation and prevent the device from switching. This problem can be avoided by limiting the current drawn out of the VD pin to less than 100 mA. A resistor placed in series between VD and the SR-MOSFET drain can be sized to provide the proper current limiting.

This resistor value is calculated by Equation 1.

$$R_{VD} \geq \frac{\left(L_{PKG} \frac{dI_{SEC}}{dt} - 0.3\,V \right)}{0.1A} \quad (1)$$

where

- L_{PKG} is the total package inductance between the drain and source pads of the SR-MOSFET when mounted on the PCB,
- dI_{SEC}/dt is the rate of rise of the secondary current after the primary-side switch turns off.

Include any stray trace inductance if the device GND pin is not connected directly to the SR-MOSFET source pad.

The bias current of the VD pin through R_{VD} (if any) generates a small offset voltage that can cause an apparent shift in the SR-MOSFET turnoff threshold, leading to earlier turn off than desired, depending on the value of R_{VD}. To counter this offset voltage, a resistor of equal value can be placed in series with the VS pin to balance the VD–VS comparator inputs ($R_{VS} = R_{VD}$).

Larger MOSFET packages such as TO-220 and TO-247 generally have significant internal inductances (on the order of 10 nH ≈ 20 nH), and are used in higher-power applications where dI/dt can be quite high. On the other hand, low-power applications using smaller packages such as QFN style and even DPAK style or equivalent MOSFETs can have a sufficiently low L × dI/dt product such that R_{VD} and R_{VS} may not be necessary. Refer to the MOSFET datasheet or consult with the manufacturer to determine the total inductance for the specific MOSFET being considered for a synchronous-rectifier application.

8.2.2.2 Enabling and TOFF Programming

The controller must be out of UVLO mode, or the internal current source on EN/TOFF pin is shut off and the pin is pulled low with an internal 10-kΩ resistor. Before the device is in the Enabled state, the current source on EN/TOFF delivers 20 µA. Prudent design practice indicates that a minimum $R_{EN/TOFF}$ value of 93 kΩ is necessary to ensure the pin voltage exceeds the disable threshold. After being Enabled, the Enabled state is latched and the source current reduces to 10 µA. This current level establishes the voltage that determines the TOFF time, as shown in Equation 2 through Equation 5.

When both the VCC and EN/TOFF conditions are met to enable the device, an internal power-up sequence ensures that the controller starts the SR-MOSFET synchronously with the system conduction conditions. This avoids turnon of the SR-MOSFET into an inappropriate system state. After a ≈25-µs delay to allow internal references to stabilize, SR operation commences in light-load mode and the load condition is monitored at the first complete switching cycle after the delay to determine the next operating mode.

Because V_{DS} of the SR-MOSFET may ring above 1.5 V and back below –150 mV one or more times (due to circuit parasitic elements), TOFF time should be programmed to block GATE re-arming for the duration of this ringing. In a system, the duration of this ringing may be unknown until actual prototypes are operational and observable, so a longer TOFF time may be initially programmed and the final value adjusted after system evaluation and optimization.

Nominal TOFF off time is programmed by Equation 2 through Equation 5, where TOFF is in µs and $R_{EN/TOFF}$ is in MΩ.

$$TOFF(\mu s) = \left(11(\mu s) - 39\left(\frac{\mu s}{M\Omega}\right) R_{EN/TOFF}(M\Omega) \right) + 0.65(\mu s)(min) \quad (2)$$

valid for:

$$0.1 \le R_{EN/TOFF}(M\Omega) \le 0.282 \quad (3)$$

Conversely,

$$R_{EN/TOFF}(M\Omega) = \frac{\left(11(\mu s) + 0.65(\mu s)(min) - TOFF(\mu s)\right)}{39\left(\frac{\mu s}{M\Omega}\right)} \quad (4)$$

valid for:

$$0.65 \le TOFF(\mu s) \le 7.75 \quad (5)$$

For any $R_{EN/TOFF}$ > 282 kΩ, TOFF = 0.65 µs.

For any 70 kΩ < $R_{EN/TOFF}$ < 80 kΩ, V_{EN} toggles rapidly between 1.4 V and 0.8 V and the device remains disabled. In this situation, average I_{CC} is approximately half of the normal run-mode current, $I_{CC(on)}$.

For any $R_{EN/TOFF}$ < 70 kΩ, VEN is < 1.4 V and the device is disabled, operating in sleep mode.

8.2.2.3 TON Programming

The voltage on this pin is internally regulated to 2 V, and an external resistor to GND sets a current which programs the minimum on time TON. If a noise-filter capacitor is deemed to be necessary on this pin, do not exceed 100 pF to avoid instability of the 2-V regulator.

Because V_{DS} of the SR-MOSFET may ring above –5 mV one or more times immediately after turn on (due to circuit parasitic elements) TON time should be programmed to block GATE turn off for the duration of this spurious ringing. In a system, the duration of this ringing may be unknown until actual prototypes are operational and observable, so a longer TON time may be initially programmed and the final value adjusted after system evaluation and optimization.

Nominal TON minimum on time is programmed by Equation 6 through Equation 9, where TON is in µs and R_{TON} is in MΩ.

$$TON(\mu s) = 15\left(\frac{\mu s}{M\Omega}\right)R_{TON}(M\Omega) \tag{6}$$

Valid for:

$$0.010 \le R_{TON}(M\Omega) \le 0.301 \tag{7}$$

Conversely,

$$R_{TON}(M\Omega) = \frac{TON(\mu s)}{15\left(\frac{\mu s}{M\Omega}\right)} \tag{8}$$

Valid for:

$$0.15 \le TON(\mu s) \le 4.5 \tag{9}$$

For resistance values of R_{TON} outside of the previous range given, the device may enter a fault-protection mode as described in *Fault Mode and Other Protections*.

8.2.2.4 GATE Drive and R_{GATE} Considerations

The GATE output driver is capable of sourcing >1-A peak current into the SR-MOSFET gate, and sinking >2 A out of it. Standard low-inductance, low-loop-area design techniques should be employed to minimize stray inductance, which slows the MOSFET turn on and increases gate-drive ringing.

A series resistance R_{GATE} from the GATE output to the MOSFET gate is used to damp this ringing, and its value is chosen based on the standard critical damping formula for a series-LCR resonant tank, see Equation 10.

$$R_{GATE} \ge 2\sqrt{\frac{L_g}{C_{iss}}} - r_g \tag{10}$$

where

- L_g is the total series gate-loop inductance,
- C_{iss} is the total effective input capacitance of the MOSFET,
- r_g is the internal gate resistance of the MOSFET.

NOTE

The total series resistance in the gate-drive path may also limit the peak GATE currents obtainable below the rated capabilities of the device's GATE output driver stage.

8.2.2.5 VCC Range and Bypassing Considerations

With a normal operating range of 4.5 V to 5.5 V, the device is well suited for 5-V nominal output applications and can easily accommodate ±10% transient VCC excursions due to system line and load disturbances. When the average VCC voltage approaches the $V_{CC(off)}$ threshold (UVLO), system ripple and noise on VCC may cross that threshold and shut down the controller unless adequate decoupling is provided from VCC to GND at the controller pins.

High peak gate-drive currents during the GATE turnon transition also require sufficient local capacitive bypassing of the VCC pin to GND. For smaller SR-MOSFETs a minimum value of 0.1 µF may be sufficient, but larger MOSFETs may require additional bypass capacitance to avoid excess ripple on the VCC voltage.

Suggested VCC bypass capacitance is 0.1 µF for each 2.2 nF of C_{iss}.

8.2.2.6 SYNC Input Considerations

In applications where the synchronous rectifier is used in continuous conduction mode (CCM) such as CCM-Flyback and LLC converters, it is imperative that the SR-MOSFET be turned off as soon as the primary-side switch turns on, to prevent reverse conduction of the SR-MOSFET. In these applications, a Y-type isolating capacitor C_{SYNC} can be used to convey a primary-side signal to the SR controller by coupling a negative-going trigger voltage into the SYNC pin. Alternatively, an isolating pulse transformer may be used in situations where a coupling capacitor is not practicable. When the SYNC voltage falls 2 V below VCC (the SYNC detection threshold V_{THSYNC}), the GATE output is immediately turned off, regardless of the state of the TON timer. An internal 2-kΩ pullup resistance (r_{SYNC}) provides current to recharge the SYNC coupling capacitor. In the event that the SYNC input voltage is continuously held below V_{THSYNC}, the GATE output is driven low for the same duration.

The SYNC input has a maximum pulse current rating of ±100 mA, and a high-reliability design should reduce the peak current further. This also reduces noise and signal losses in the system. A series resistor helps limit the pulse current by reducing the effective dV/dt across C_{SYNC}. Figure 23 illustrates a simple implementation of the SYNC signal derived from the falling drain-source voltage of the primary-side MOSFET. In this example, a synchronous-rectifier MOSFET is used in place of the free-wheeling diode in a single-transistor forward-mode application. Note that primary-to-secondary common-mode capacitance CCM forms the return path for the SYNC current.

Nominally, only –1 mA is required to develop –2 V across the internal 2-kΩ resistance and trigger the SYNC function. This current is generated by a rapidly changing voltage across the SYNC coupling capacitor C_{SYNC}. But variations of this resistor, of C_{SYNC}, and of the dV/dt across C_{SYNC} require that worst-case tolerances be taken into account when determining the minimum value of C_{SYNC}. In addition, V_{SYNC} must exceed the V_{THSYNC} threshold for a minimum duration of 20 ns to ensure that the internal controller logic has reliably triggered.

Although the TON minimum on-time gate-drive function is overridden by the SYNC signal, the timer continues to function otherwise. Light-load mode is entered if the proper conditions are met, as usual. The TOFF timer is triggered when the SR-MOSFET V_{DS} exceeds 1.5 V, as usual.

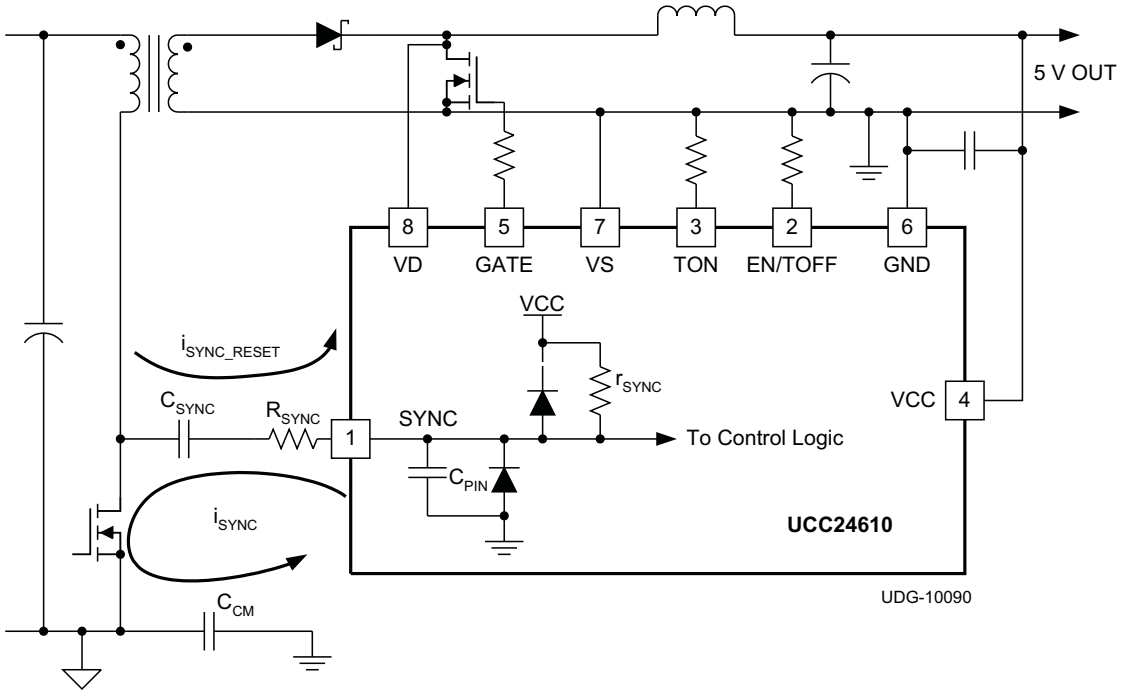


Figure 23. Driving the SYNC Input from the Primary-Side MOSFET Drain

C_{SYNC} is the synchronization signal coupling capacitor, rated to cross the primary-to-secondary isolation boundary. It is used to couple a negative-going voltage into the UCC24610 SYNC input (pin 1) to turn off the GATE output to the SR-MOSFET when the primary-side MOSFET is turned on.

R_{SYNC} is an optional external current-limiting resistor used to reduce the peak current into the SYNC input. It also serves to reduce overall power loss, and reduce the common-mode noise current.

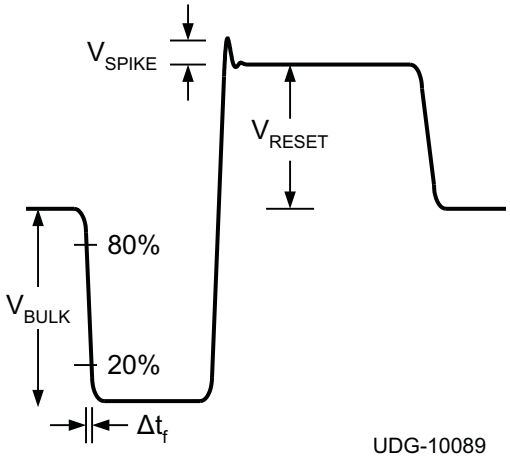
C_{CM} is the main common-mode capacitance between the primary and the secondary sides of the system. This is usually a discrete component, whose value ranges from 100 pF ≈2200 pF. Aside from any EMI-control purposes, it also serves as the return path for the SYNC signal charging and discharging current pulses across the isolation boundary.

Within the UCC24610 controller device is a 2-kΩ pullup resistor (r_{SYNC}) to VCC. To trigger the SYNC function, a negative-going signal must pull the SYNC input below the V_{THSYNC} threshold (nominally 2 V below VCC) for a minimum duration of 20 ns. This requires a minimum 1-mA current to achieve, but prudent design will target a higher current to allow for parameter variations.

Internal clamp diodes to VCC and GND also form parts of the charging and discharging current paths of the SYNC signal. Finally, C_{PIN} comprises stray internal and external pin and pad capacitances on the SYNC input, and is modeled as ≈10 pF to GND. Although C_{PIN} is physically unavoidable, it is wise to minimize any external stray capacitance to keep its effect of additional delay on the SYNC function to a minimum.

8.2.2.6.1 Determine the Minimum Change

Determine the minimum change in voltage $\Delta V_{SYNC\text{-}pri}$ expected from the SYNC signal source. In this example, the primary-side MOSFET drain-to-source voltage V_{DS_PRI} is the signal source, and its minimum change is $V_{BULK(min)}$ at low input line.



$\Delta V_{DS\_PRI} = V_{BULK}$ at low-line

Δt_f = fall time for ΔV_{DS_PRI} between the 80% and 20% points

$V_{SYNC\text{-}pri} = \Delta V_{DS\_PRI}$

Figure 24. Primary MOSFET Drain Voltage

To allow for parameter and environmental variations, set the minimum peak SYNC current to 2 mA. With 2-mA peak flowing through the internal 2-kΩ resistor, the SYNC voltage falls to 4-V below VCC. The maximum value for current limiting resistor R_{SYNC} is determined by Equation 11 and Equation 12.

$$R_{SYNC} \le \frac{\Delta V_{SYNC-pri}}{i_{SYNC}(min)} - r_{SYNC} \tag{11}$$

so in this case,

$$R_{SYNC} \le \frac{V_{BULK}(min)}{2mA} - 2k\Omega \tag{12}$$

8.2.2.6.2 After the ΔV_{DS_PRI} Transition

After the ΔV_{DS_PRI} transition, the SYNC signal will begin to reset back to VCC by charging exponentially. This allows the value of the SYNC coupling capacitor C_{SYNC} to be determined by Equation 13.

$$C_{SYNC} = \frac{1.5 \times t_{MIN}}{R_{SYNC} + r_{SYNC}} \tag{13}$$

The value of C_{SYNC} is chosen to ensure that the SYNC signal stays below the SYNC threshold for at least 20 ns. Choose the minimum dwell time t_{MIN} to be 40 ns to allow for parametric variations, shown in Equation 14.

$$C_{SYNC} = \frac{1.5 \times 40\,ns}{R_{SYNC} + 2k\Omega} \tag{14}$$

8.2.2.6.3 The Value of C_{CM}

The value of C_{CM} should be much higher than that of C_{SYNC}. If necessary, increase the value of C_{CM} to ensure that C_{CM} >> C_{SYNC}; do not decrease C_{SYNC}.

8.2.2.6.4 Conservative Power-Loss Estimates

Conservative power-loss estimates for the internal and external SYNC resistances are:

$$P_{r_{SYNC}} \le \left[\frac{(VCC + 0.7\,V)^2}{r_{SYNC}}\right] \times \left[\ln\left(\frac{\Delta V_{SYNC-pri-max}}{\Delta V_{SYNC-pri-min}}\right) + 1\right] \times \left[(R_{SYNC} + r_{SYNC}) \times C_{SYNC} \times f_{SW}\right] \tag{15}$$

and

$$P_{R_{SYNC}} \le 2 \times \left[\frac{1}{2} \times C_{SYNC} \times (V_{BULK} + V_{RESET} + V_{SPIKE})^2 \times f_{SW}\right]$$

where

- f_{SW} is the converter switching frequency. (16)

These calculations can be used to predict the maximum thermal impact of the SYNC current on the device junction temperature and to determine the external SYNC resistor power rating. Actual SYNC-related losses generally are lower than these calculations predict and observations of actual circuit operation should be used to determine true losses if more accuracy is required.

8.2.2.6.5 The Device Internal SYNC-to-GATE Delay Time

The device internal SYNC-to-GATE delay time t_{SDLY} is a measure of how quickly the GATE output will turn off after the SYNC signal has crossed the V_{THSYNC} threshold. However, stray pin capacitance C_{PIN} introduces an additional delay to the SYNC function by slowing the SYNC voltage falling 2-V below VCC. If C_{PIN} is small, this delay is relatively short and the SYNC current can be approximated as a constant current, allowing this calculation to simplify to a simple linear equation given by:

$$t_{PIN\_DLY} = \frac{2\,V \times C_{PIN}}{i_{SYNC}} \tag{17}$$

Also, additional delay comes from the finite dV/dt of the signal source, in this case V_{DS_PRI}, due to the finite transition time from V_{BULK} level to 0 V. This delay can be approximated by:

$$t_{dV\_DLY} = \frac{\Delta t_f \times R_{SYNC}}{R_{SYNC} + r_{SYNC}} \tag{18}$$

These delay times should be added to the internal SYNC-to-GATE delay to determine the total delay time expected between the falling of the primary-side MOSFET drain voltage and the turn off of the SR-FET gate drive.

$$t_{OFF\_DLY} = t_{SDLY} + t_{PIN\_DLY} + t_{dV\_DLY} \tag{19}$$

8.2.2.6.6 The C_{SYNC} Capacitor Resets

The C_{SYNC} capacitor resets during the off-time of the primary-side MOSFET, while the SR-FET is conducting. The reset current i_{SYNC_RESET} is similar to i_{SYNC}. However, this reset current flows through the internal diode between SYNC and VCC pins of the device.

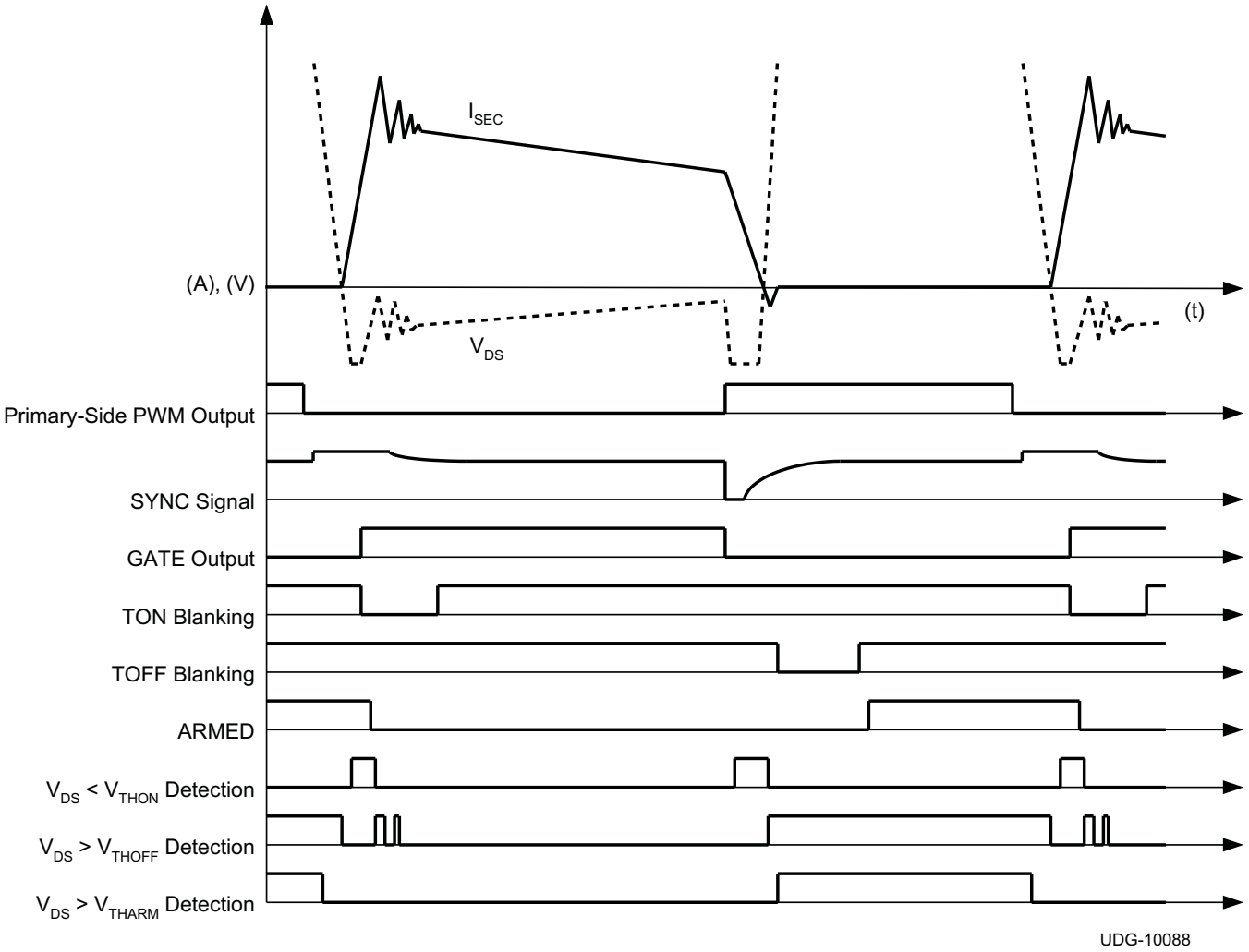


Figure 25. External and Internal Signal Timing Relationships with Respect to Realistic CCM Waveforms

8.2.2.7 Single-Fault Self-Protection Features

If R_{TON} is less than 8.7 kΩ, the device may detect excess current and interpret this as a short-cir cuit and disable the GATE output.

If R_{TON} is greater than 301 kΩ, the device may detect insufficient current and interpret this as an open-circuit and disable the GATE output, to avoid indefinite on-time.

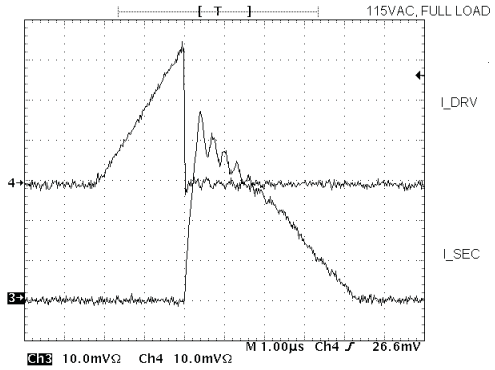
Noise pick-up on excessive trace length may destabilize the internal 2-V source causing either insufficient or excess current to R_{TON} and triggering premature GATE shut off. This could cause GATE output to be less than TON and lead to light-load mode even at heavy loads. Minimize R_{TON} trace lengths.

If $R_{EN/TOFF}$ is less than 93 kΩ, the device may detect insufficient voltage for Enable threshold and disable the GATE output.

If $R_{EN/TOFF}$ is greater than 284 kΩ, the device will internally clamp the programming voltage to deliver a minimum T_{OFF} of ≈0.65 µs, regardless of $R_{EN/TOFF}$ value.

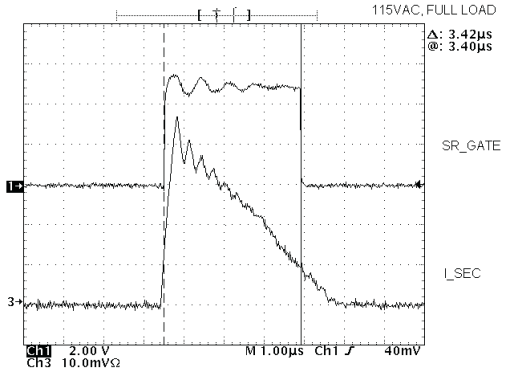
8.2.3 Application Curves

The following oscilloscope screen-captures and performance data illustrate the operation of the UCC24610 SR controller as applied in the UCC24610EVM-563 evaluation module, using, in part, the design method and equations found in *Detailed Design Procedure*. These select figures are reproduced from *Using the UCC24610EVM-563* User's Guide (SLUU434).



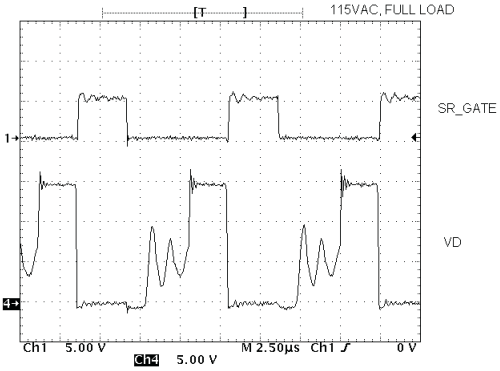
115-V_{AC} input 5-A load

Figure 26. Primary and Secondary MOSFET Currents



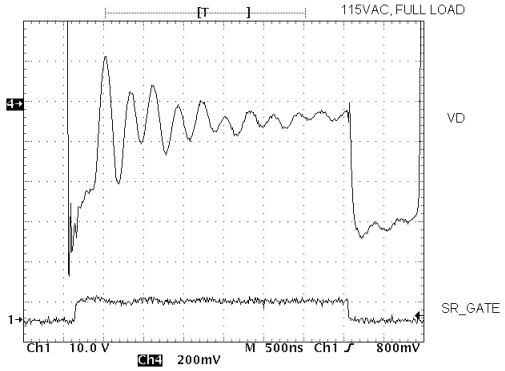
115-V_{AC} input 5-A load

Figure 27. SR MOSFET Drain Current and SR GATE Signal



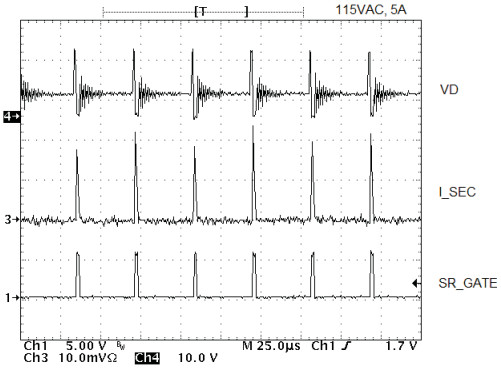
115-V_{AC} input 5-A load

Figure 28. SR MOSFET Gate and Drain Waveforms



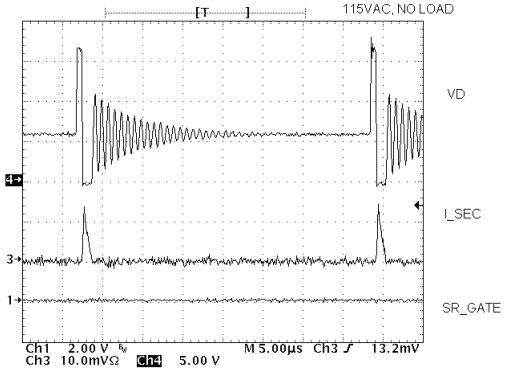
115-V_{AC} input 5-A load

Figure 29. Close-Up View of VD and SR GATE



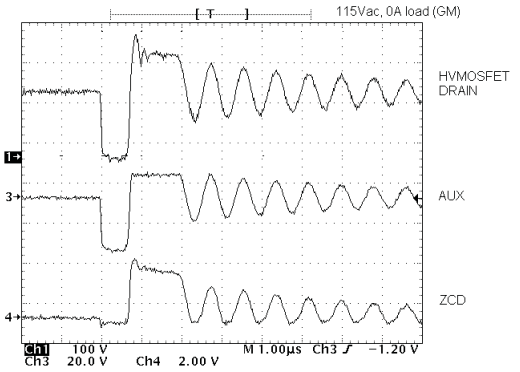
115-V_{AC} input 5-A load

Figure 30. Secondary-Side Waveforms



115-V_{AC} Input 0-A load green mode

Figure 31. Secondary-Side Waveforms



115-V_{AC} Input 0-A load green mode

Figure 32. Primary-Side Waveforms

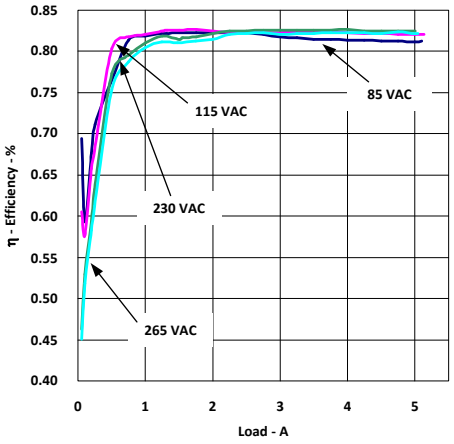


Figure 33. Overall EVM Efficiency as a Function of Load Current and Input Voltage

9 Power Supply Recommendations

The UCC24610 in nominally a 5-V only controller as regards to the VCC bias supply rating. Although the absolute maximum rating for VCC is 6.5 V, it is recommended to operate the device with VCC < 5.5 V to allow margin for voltage-rail transients and surges. Although the device may typically function with VCC down to 4.2 V, it is recommended to operate the device at VCC ≥ 4.5 V to provide adequate gate-drive to the SR MOSFET. Use a ceramic bypass capacitor from VCC to GND of suitable value to provide the total gate charge each switching cycle.

10 Layout

10.1 Layout Guidelines

The printed circuit board (PCB) requires conscientious layout to minimize current loop areas and track lengths, especially when using single-sided PCBs.

- Place a ceramic MLCC bypass capacitor as close as possible to VCC and GND.
- Avoid connecting VD and VS sense points at locations where stray inductance is added to the SR MOSFET package inductance, as this will tend to turn off the SR prematurely.
- Run a track from the VD pin directly to the MOSFET drain pad to avoid sensing voltage across the stray inductance in the SR drain current path. Include an R_{VD} component option in series with the VD pin unless previous testing has shown that it is not necessary.
- Run a track from the VS pin directly to the MOSFET source pad to avoid sensing voltage across the stray inductance in the SR source current path. Do not simply connect VS to the controller GND pin. Include an R_{VS} component option in series with the VS pin unless previous testing has shown that it is not necessary.
- Run parallel tracks from GATE and GND to the SR MOSFET. Include a series gate resistance to dampen ringing.

10.2 Layout Example

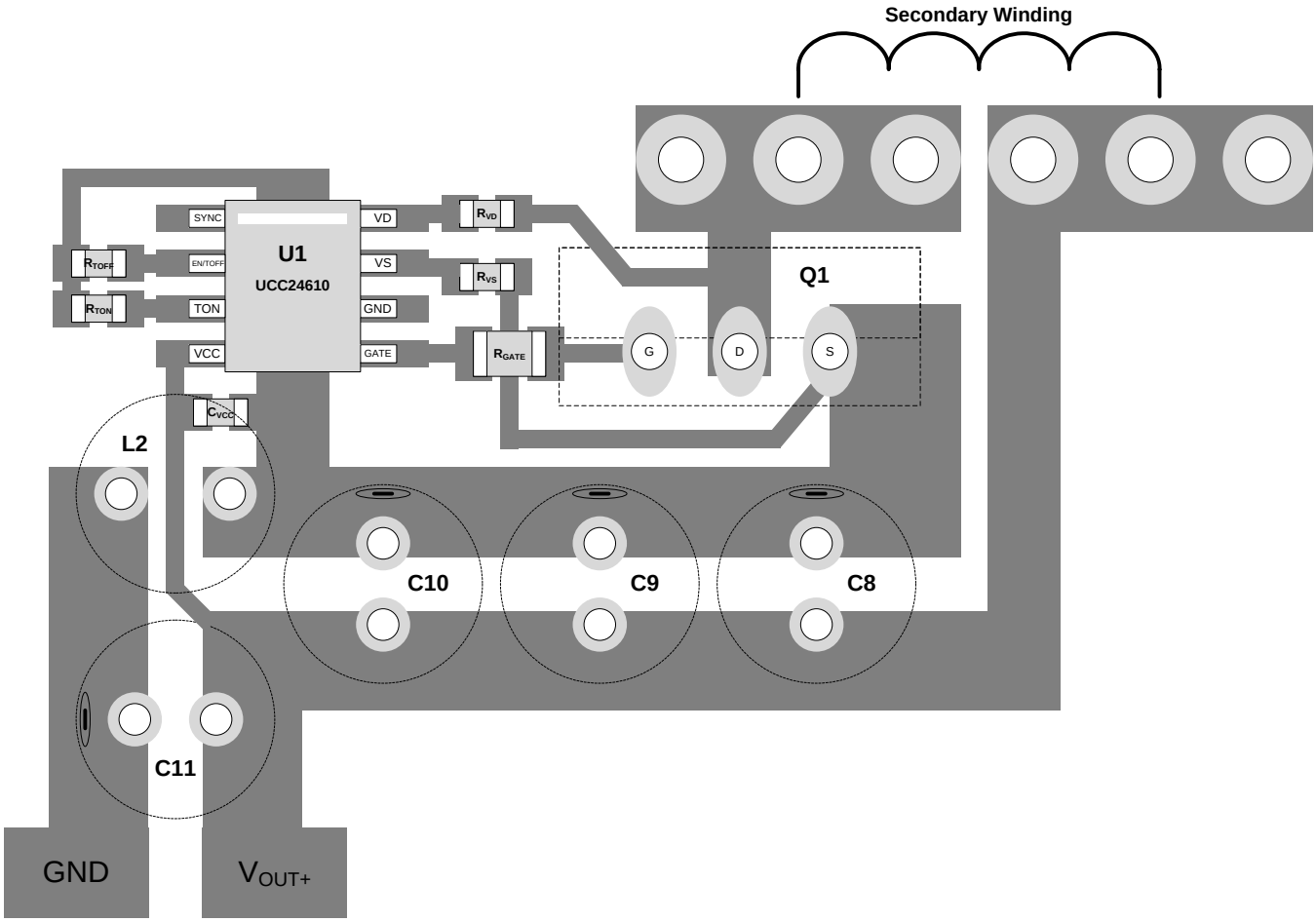


Figure 34. Single-Sided PCB Layout Using a TO-220 MOSFET

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

GREEN Rectifier, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC24610D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	24610	Samples
UCC24610DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	24610	Samples
UCC24610DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	4610	Samples
UCC24610DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	4610	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

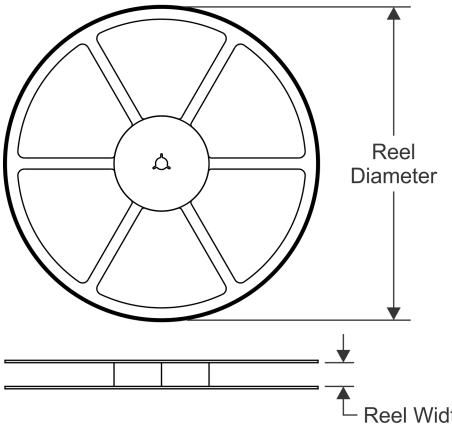
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

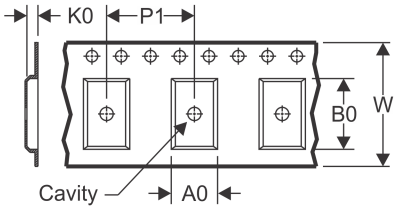
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

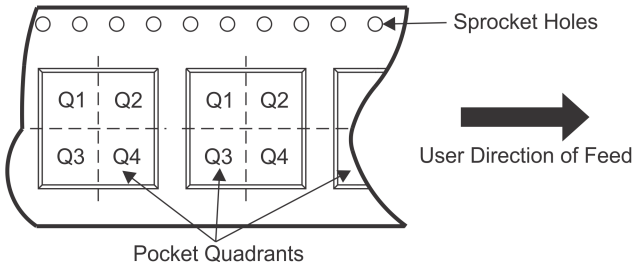


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

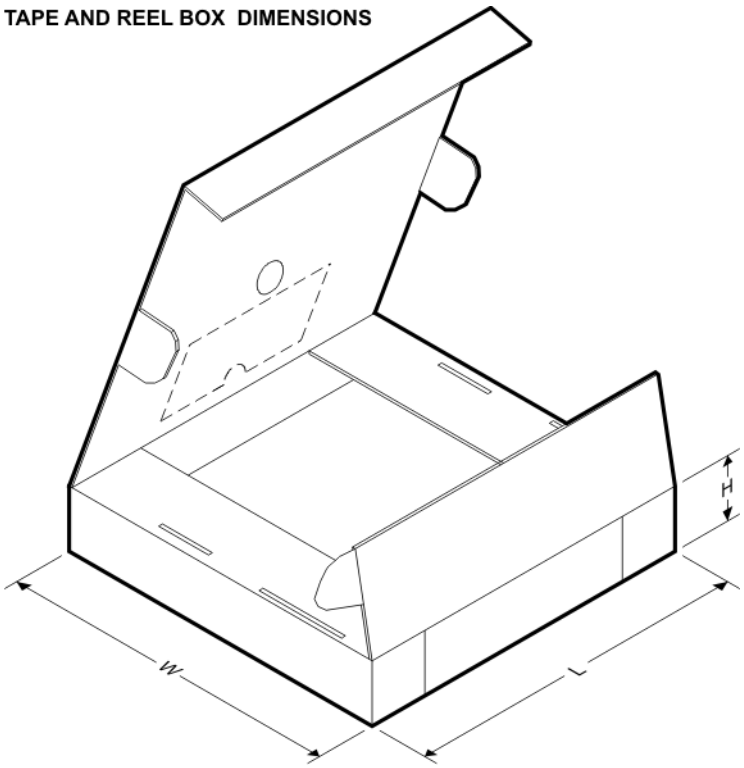
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC24610DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC24610DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC24610DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

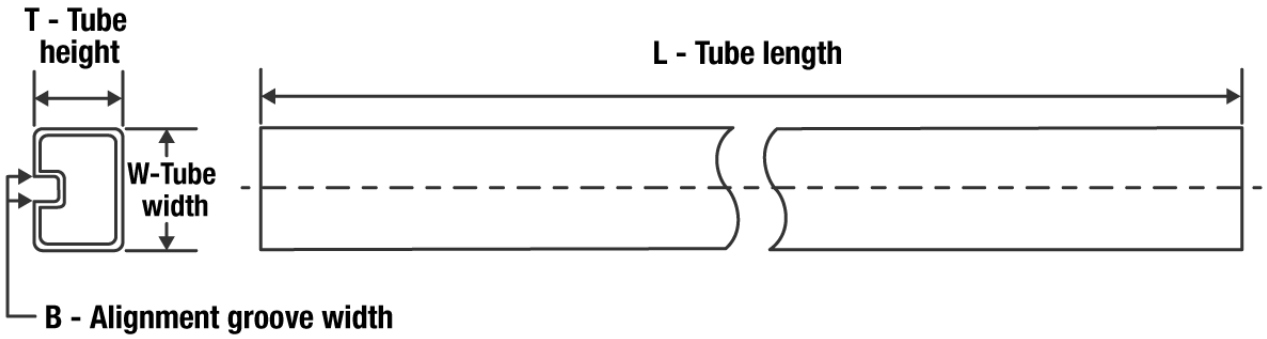
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

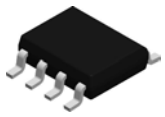
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC24610DR	SOIC	D	8	2500	340.5	336.1	25.0
UCC24610DRBR	SON	DRB	8	3000	367.0	367.0	35.0
UCC24610DRBT	SON	DRB	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC24610D	D	SOIC	8	75	507	8	3940	4.32

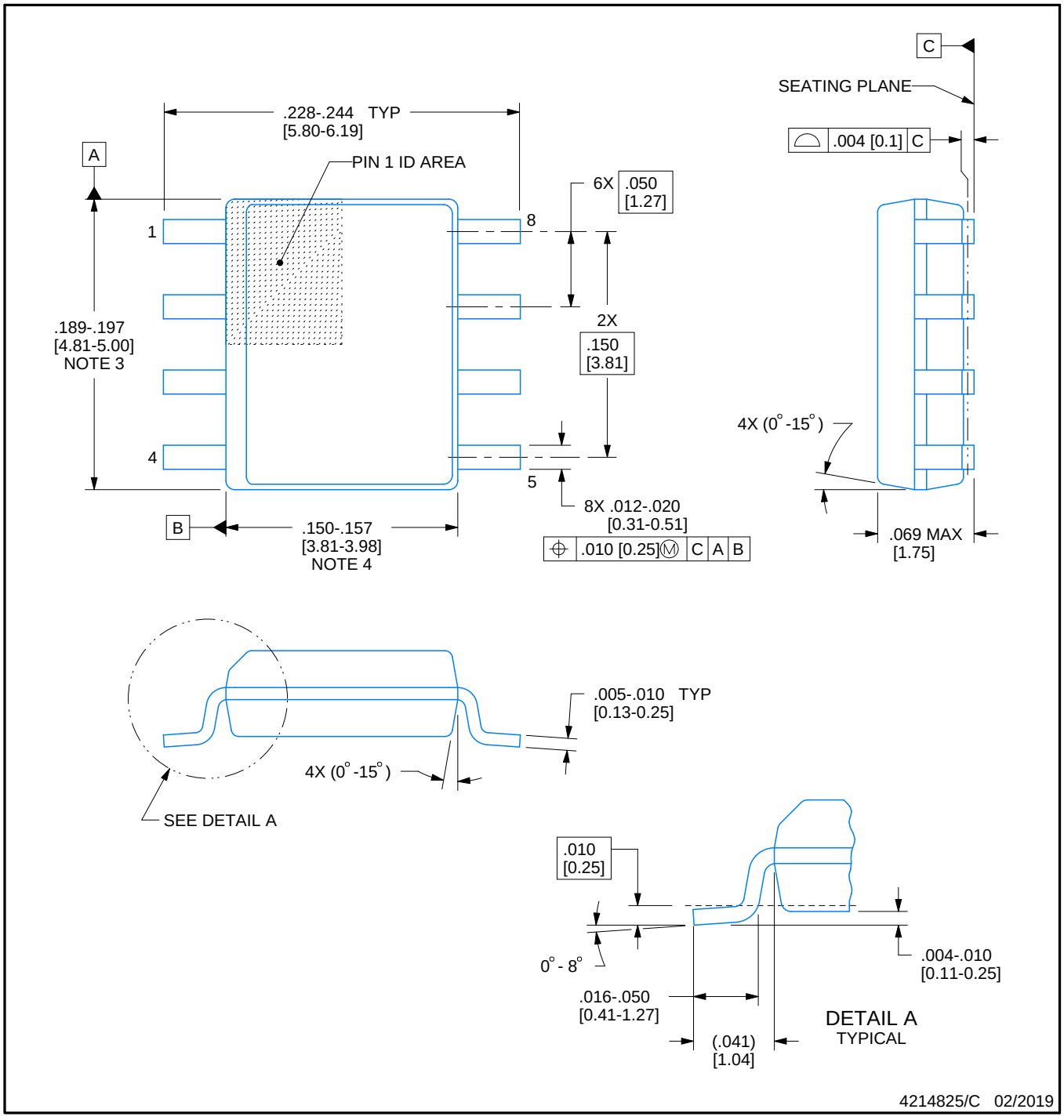


PACKAGE OUTLINE

D0008A

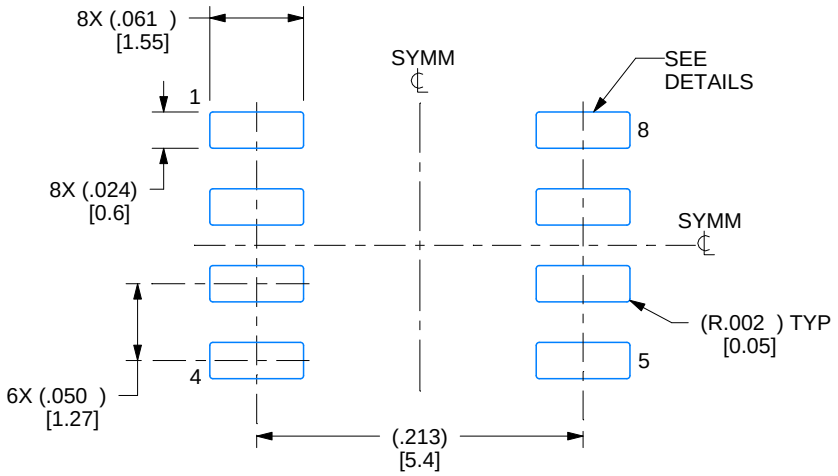
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

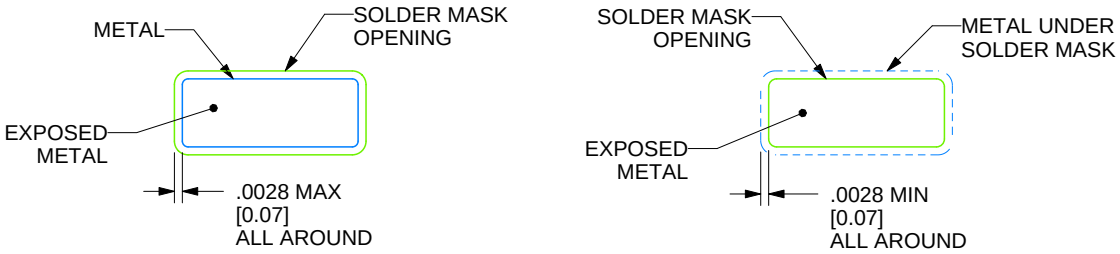


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

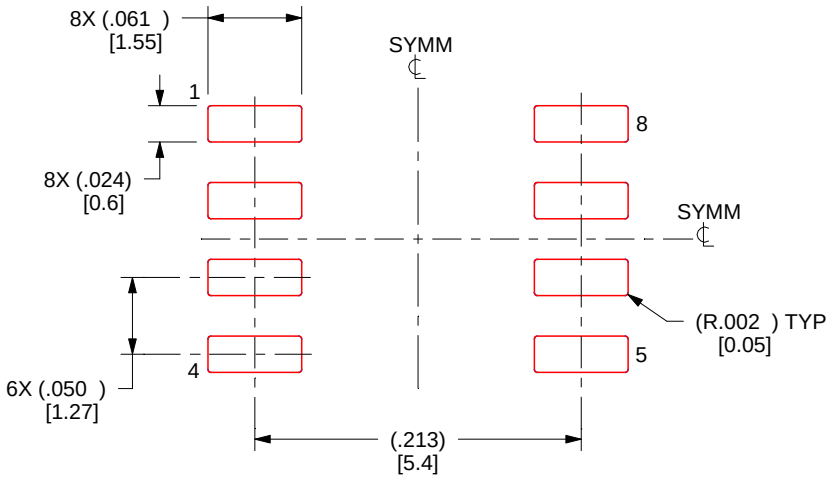
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

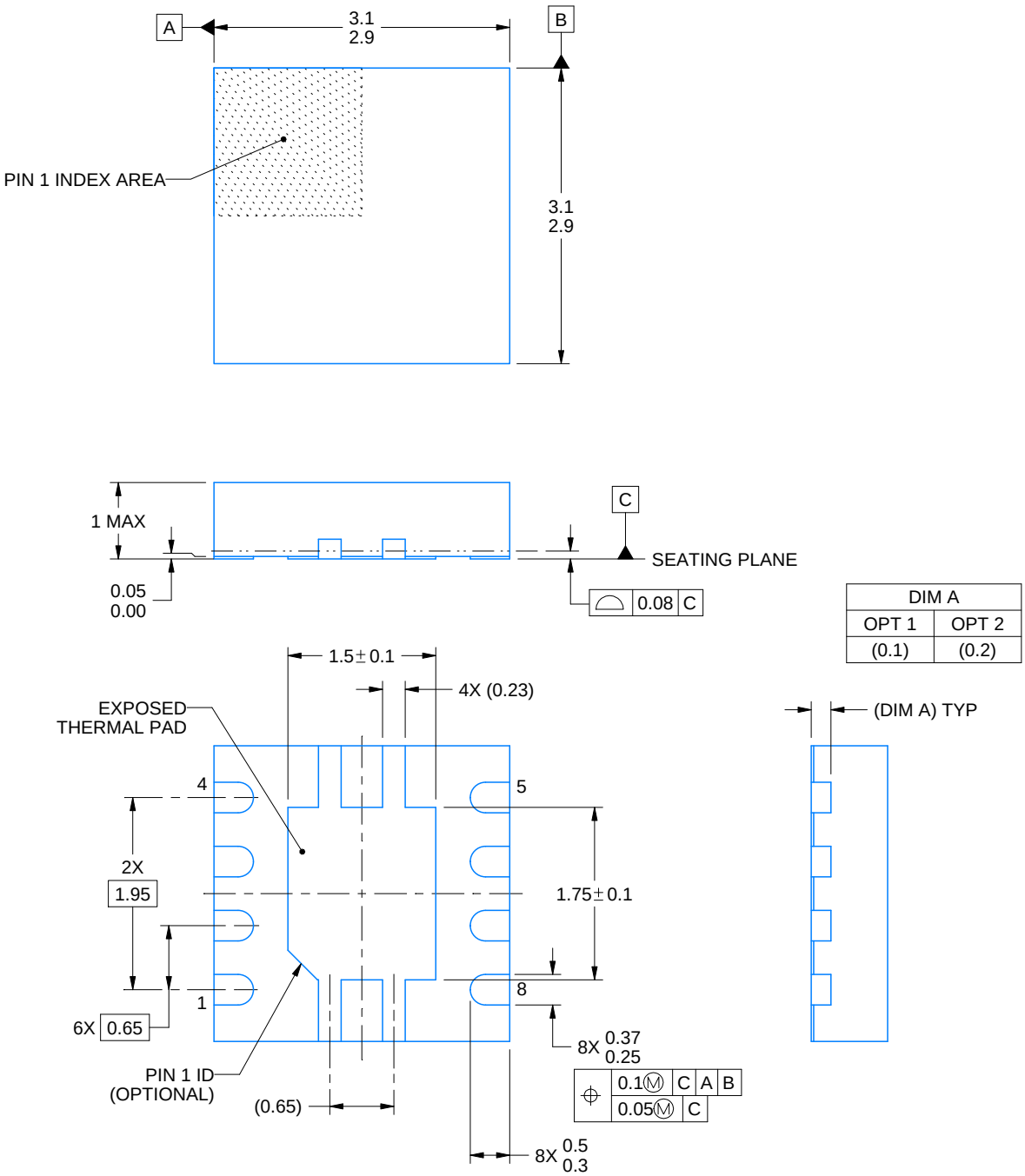
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

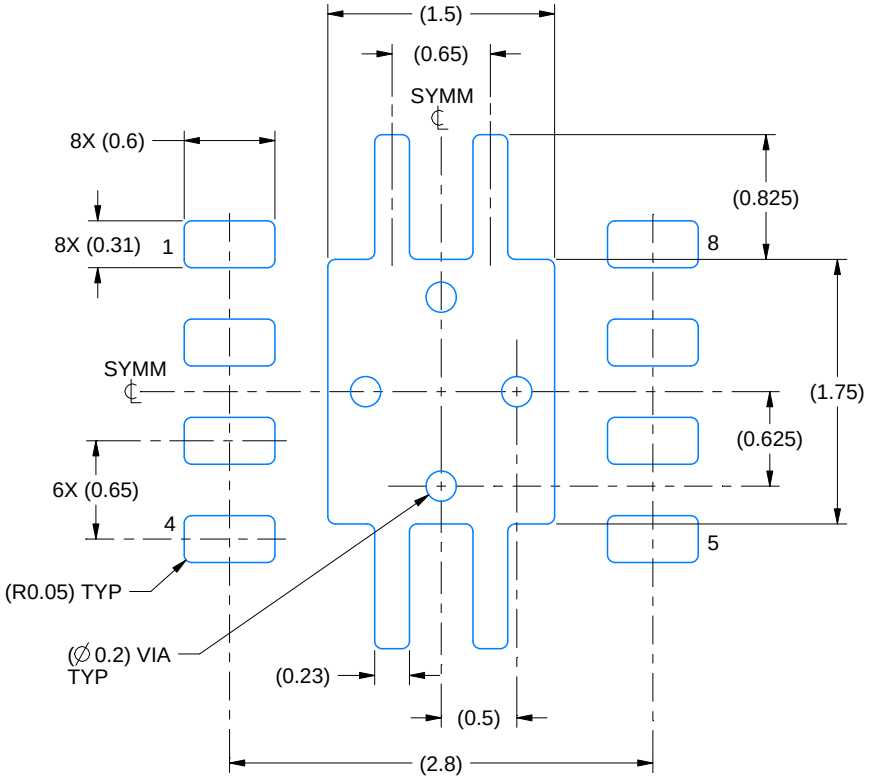
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

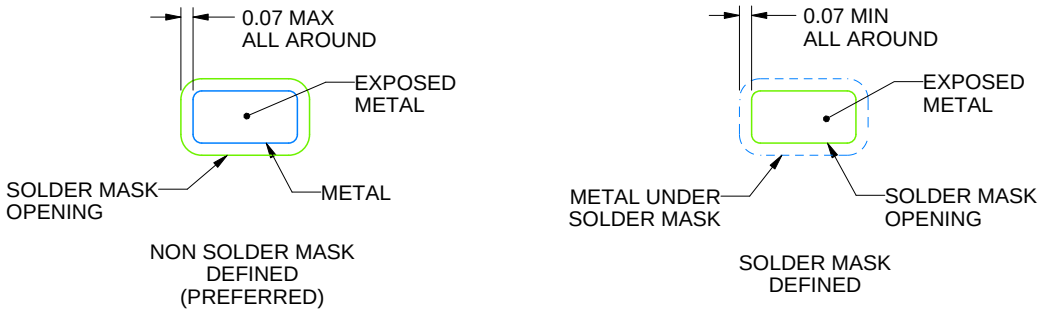
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

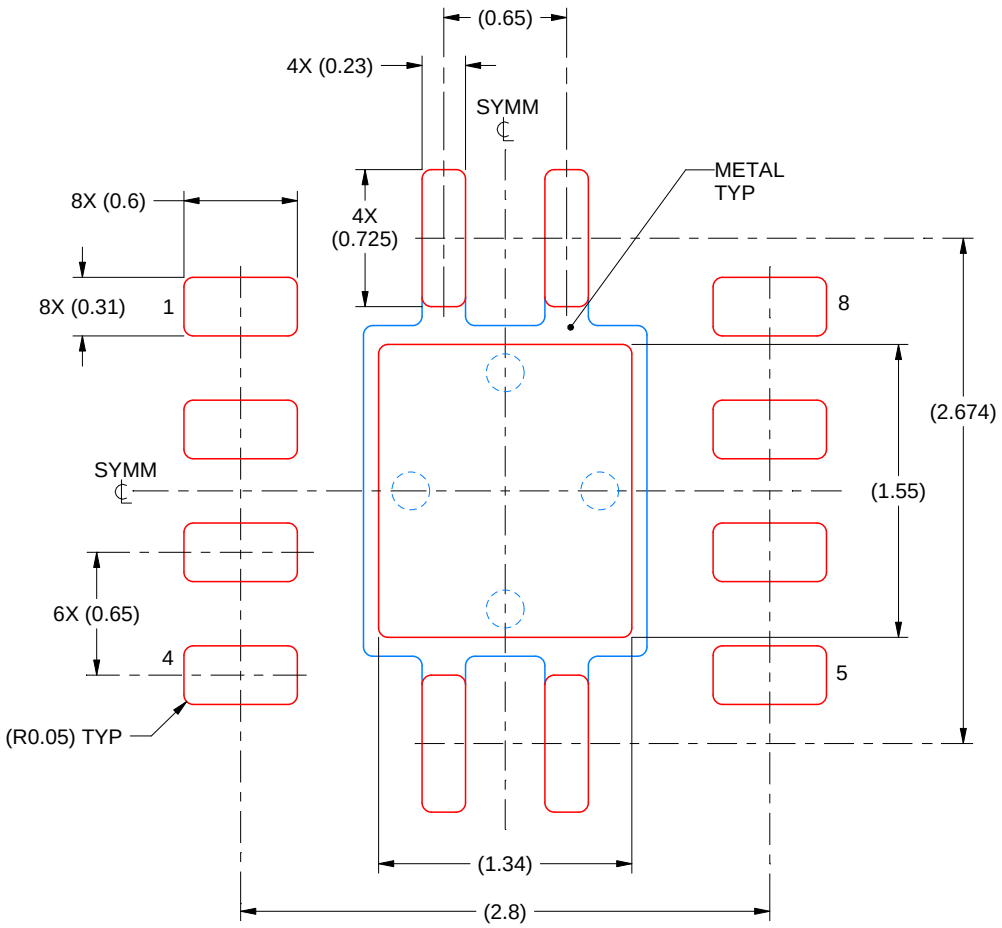


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265