128K X 36 Dual I/O Dual Address Synchronous SRAM

Features

- **Fast clock speed: 100 and 83 MHz**
- **Fast access times: 5.0/6.0 ns max.**
- **Single clock operation**
- **Single 3.3V –5% and +5% power supply V_{CC}**
- **Separate V_{CCQ} for output buffer**
- **Two chip enables for simple depth expansion**
- **Address, data input, CE1X, CE2X, CE1Y, CE2Y, PTX, PTY, WEX, WEY, and data output registers on-chip**
- **Concurrent Reads and Writes**
- **Two bidirectional data buses**
- **Can be configured as separate I/O**
- **Pass-through feature**
- **Asynchronous output enables (OEX, OEY)**
- **LVTTL-compatible I/O**
- **Self-timed Write**
- **Automatic power-down**
- **176-pin TQFP package**

Functional Description

The CY7C1300A SRAM integrates 131,072 × 36 SRAM cells with advanced synchronous peripheral circuitry. It employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1300A allows the user to concurrently perform Reads, Writes, or pass-through cycles in combination on the two data ports. The two address ports (AX, AY) determine the Read or Write locations for their respective data ports (DQX, DQY).

All input pins except output enable pins ($\overline{OEX}$, $\overline{OEY}$) are gated by registers controlled by a positive-edge-triggered clock (CLK) input. The synchronous inputs include all addresses, data inputs, depth-expansion chip enables ($\overline{CE1X}$, $\overline{CE2X}$, $\overline{CE1Y}$ and $\overline{CE2Y}$), pass-through controls ($\overline{PTX}$ and $\overline{PTY}$), and Read–Write control ($\overline{WEX}$ and $\overline{WEY}$).

The pass-through feature allows data to be passed from one port to another, in either direction. The $\overline{PTX}$ input must be asserted to pass data from port X to port Y. The $\overline{PTY}$ will likewise pass data from port Y to port X. A pass-through operation takes precedence over a Read operation.

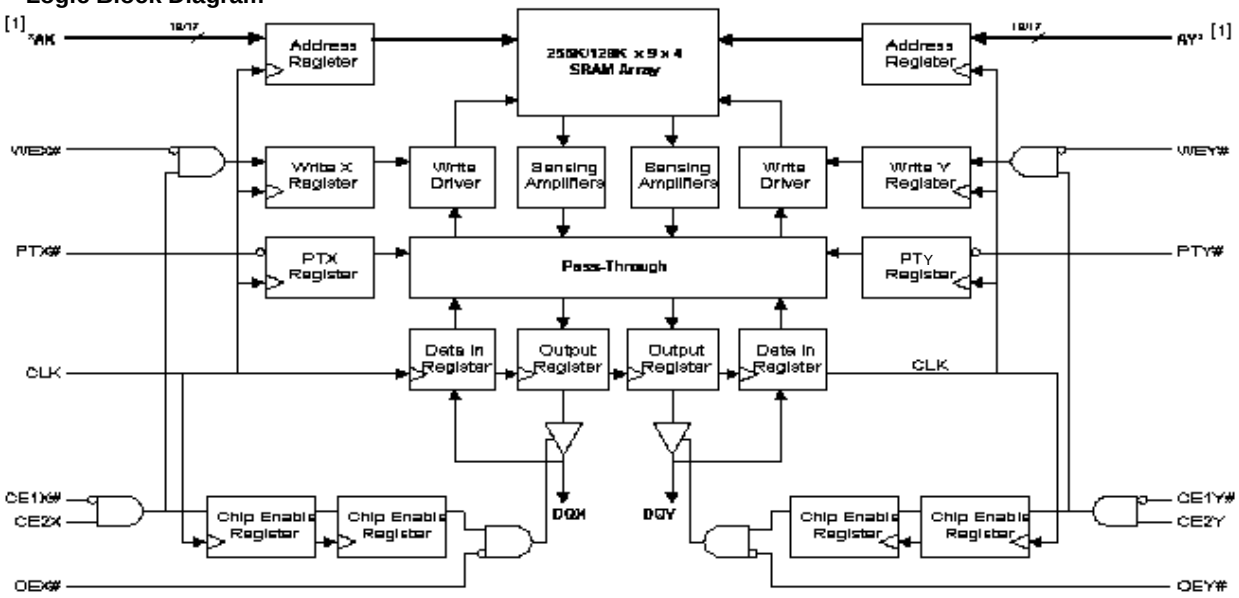
When AX and AY are the same, certain protocols are followed. If both ports are Read, the reads occur normally. If one port is written and the other is read, the read from the array will occur before the data is written. If both ports are written, only the data on DQY will be written to the array.

The CY7C1300A operates from a +3.3V power supply. All inputs and outputs are LVTTL-compatible. These dual I/O, dual address synchronous SRAMs are well suited for ATM, Ethernet switches, routers, cell/frame buffers, SNA switches, and shared memory applications.

The CY7C1300A needs one extra cycle after power for proper power-on reset. The extra cycle is needed after V_{CC} is stable on the device.

This device is available in a 176-pin TQFP package.

Logic Block Diagram[1]



Note:

1. For 128K x 36 devices, AX and AY are 17-bit-wide buses.

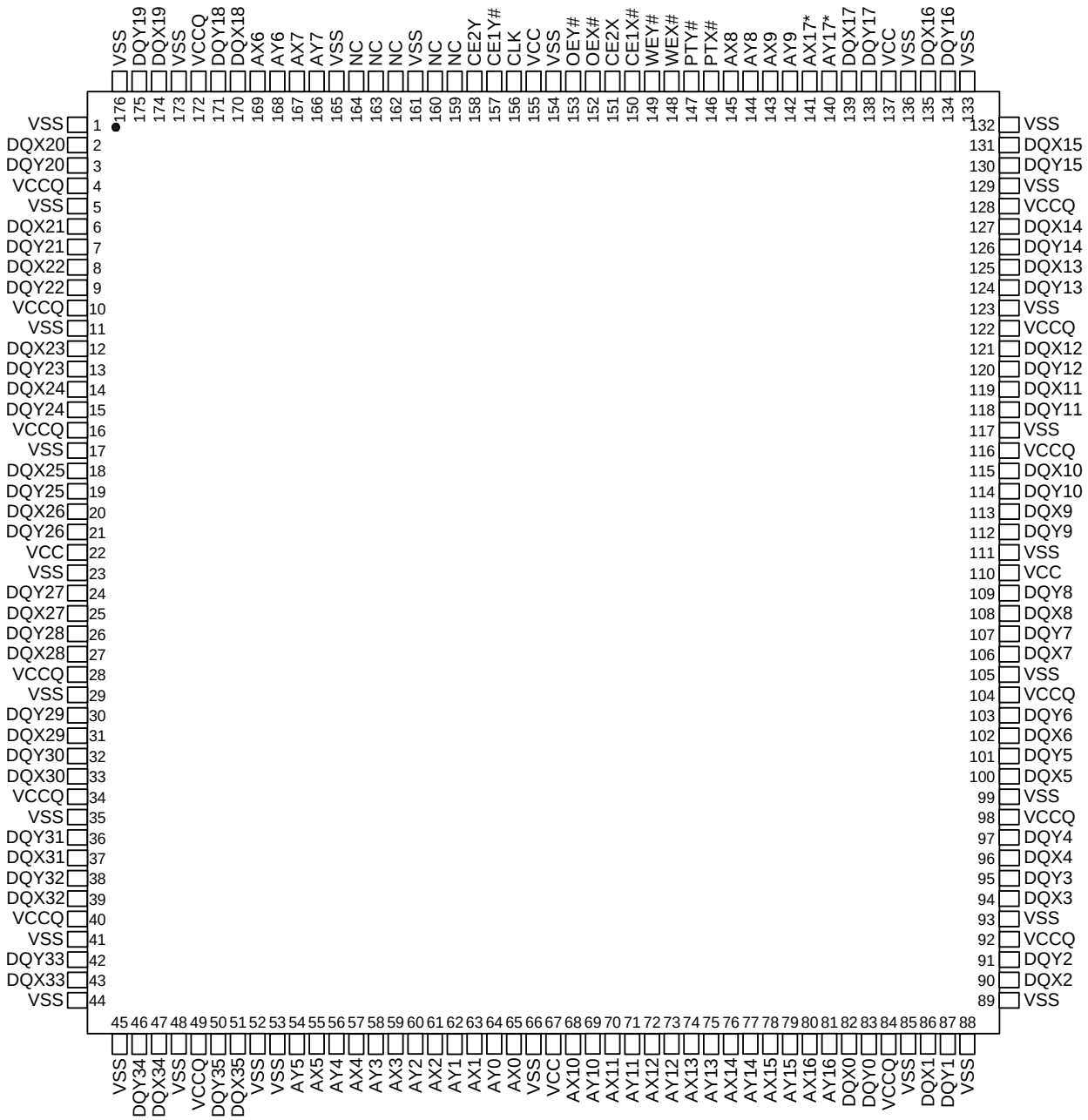
Selection Guide

	-100	-83	Unit
Maximum access time	5.0	6.0	ns
Maximum operating current	500	430	mA
Maximum CMOS standby current	100	100	mA

Shaded areas contain advance information.

Pin Configuration

176-pin TQFP



Pin Definitions

Name	I/O	Description
AX0–AX16	Input–Synchronous	***Synchronous Address Inputs of Port X***: Do not allow address pins to float.
AY0–AY16	Input–Synchronous	***Synchronous Address Inputs of Port Y***: Do not allow address pins to float.
$\overline{WEX}$	Input–Synchronous	***Read Write of Port X***: $\overline{WEX}$ signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation.
$\overline{WEY}$	Input–Synchronous	***Read Write of Port Y***: $\overline{WEY}$ signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation.
$\overline{PTX}$	Input–Synchronous	***Pass-Through of Port X***: $\overline{PTX}$ signal is a synchronous input that enables passing Port X input to Port Y output.
$\overline{PTY}$	Input–Synchronous	***Pass-Through of Port Y***: $\overline{PTY}$ signal is a synchronous input that enables passing Port Y input to Port X output.
$\overline{OEX}$	Input	***Asynchronous Output Enable of Port X***: $\overline{OEX}$ must be LOW to read data. When $\overline{OEX}$ is HIGH, the DQXx pins are in high-impedance state.
$\overline{OEY}$	Input	***Asynchronous Output Enable of Port Y***: $\overline{OEY}$ must be LOW to read data. When $\overline{OEY}$ is HIGH, the DQYx pins are in high-impedance state.
DQX0–DQX35	Input/Output	***Data Inputs/Outputs of Port X***: Both the data input path and data output path are registered and triggered by the rising edge of CLK.
DQY0–DQY35	Input/Output	***Data Inputs/Outputs of Port Y***: Both the data input path and data output path are registered and triggered by the rising edge of CLK.
CLK	Input–Synchronous	***Clock***: This is the clock input to this device. Except for $\overline{OEX}$ and $\overline{OEY}$, all timing references of the address, data in, and all control signals for the device are made with respect to the rising edge of CLK.
$\overline{CE1X}$	Input–Synchronous	***Synchronous Active LOW Chip Enable Port X***: $\overline{CE1X}$ is used with CE2X to enable Port X of this device. $\overline{CE1X}$ sampled HIGH at the rising edge of clock initiates a deselect cycle for Port X.
CE2X	Input–Synchronous	***Synchronous Active HIGH Chip Enable Port X***: CE2X is used with $\overline{CE1X}$ to enable Port X of this device. CE2X sampled LOW at the rising edge of clock initiates a deselect cycle for Port X.
$\overline{CE1Y}$	Input–Synchronous	***Synchronous Active LOW Chip Enable Port Y***: $\overline{CE1Y}$ is used with CE2Y to enable Port Y of this device. CE1Y sampled HIGH at the rising edge of clock initiates a deselect cycle for Port Y.
CE2Y	Input–Synchronous	***Synchronous Active HIGH Chip Enable Port Y***: CE2Y is used with $\overline{CE1Y}$ to enable Port Y of this device. CE2Y sampled LOW at the rising edge of clock initiates a deselect cycle for Port Y.
V_{CC}	Supply	***Power Supply***: +3.3V –5% and +5%.
V_{SS}	Ground	***Ground***: GND.
V_{SS}	Ground	***Ground***: GND. No chip current flows through these pins. However, the user needs to connect GND to these pins.
V_{CCQ}	I/O Supply	***Output Buffer Supply***: +3.3V -5% and +5%.
NC	–	***No Connect***: These signals are not internally connected. The user can connect them to V_{CC}, V_{SS}, or any signal lines, or simply leave them floating.

Cycle Description Truth Table [2, 3, 4, 5, 6, 7, 8, 9]

Operation	$\overline{CE1X}$	CE2X	$\overline{CE1Y}$	CE2Y	$\overline{WEX}$	$\overline{WEY}$	$\overline{PTX}$	$\overline{PTY}$
Deselect Cycle	H	X	H	X	X	X	X	X
Deselect Cycle	X	L	X	L	X	X	X	X
Write Port X	L	H	X	X	0	X	X	X

Notes:

2. X means “Don’t Care.” H means logic HIGH. L means logic LOW.
3. All inputs except OEX and OEY must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
4. OEX and OEY must be asserted to avoid bus contention during Write and Pass-through cycles. For Write and Pass-through operations following a Read operation, OEX/OEY must be HIGH before the input data required set-up time plus High-Z time for OEX/OEY and staying HIGH throughout the input data hold time.
5. Operation numbers 3–6 can be used in any combination.
6. Operation numbers 4 and 7, 3 and 8, and 7 and 8 can be combined.
7. Operation numbers 5 can not be combined with operation number 7 or 8 because Pass-through operation has higher priority over a Read operation.
8. Operation number 6 can not be combined with operation number 7 or 8 because Pass-through operation has higher priority over a Read operation.
9. This device contains circuitry that will ensure the outputs will be in High-Z during power-up

Cycle Description Truth Table (continued)[2, 3, 4, 5, 6, 7, 8, 9]

Operation	$\overline{CE1X}$	CE2X	$\overline{CE1Y}$	CE2Y	$\overline{WEX}$	$\overline{WEY}$	$\overline{PTX}$	$\overline{PTY}$
Write Port Y	X	X	L	H	X	0	X	X
Pass-through from X to Y	L	H	L	H	X	X	0	X
Pass-through from Y to X	L	H	L	H	X	X	X	0
Read Port X	L	H	X	X	1	X	1	1
Read Port Y	X	X	L	H	X	1	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied..... –10°C to +85°C

Supply Voltage on V_{DD} Relative to GND.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[10] .....–0.5V to V_{CCQ} + 0.5V

DC Input Voltage[10] .....–0.5V to V_{CCQ} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 1601V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature[11]	V_{DD}/V_{DDQ}[12]
Commercial	0°C to +70°C	3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.465	V
V_{DDQ}	I/O Supply Voltage			3.135	3.465	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage[13]			2.0	V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage[14]			–0.5	0.8	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{IN} ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{CC}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	10.0 ns cycle, MHz		500	mA
			12.0 ns cycle, 83 MHz		430	mA
I_{SB}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected[15], V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	10.0 ns cycle, 100 MHz		140	mA
			12.0 ns cycle, 83 MHz		120	mA

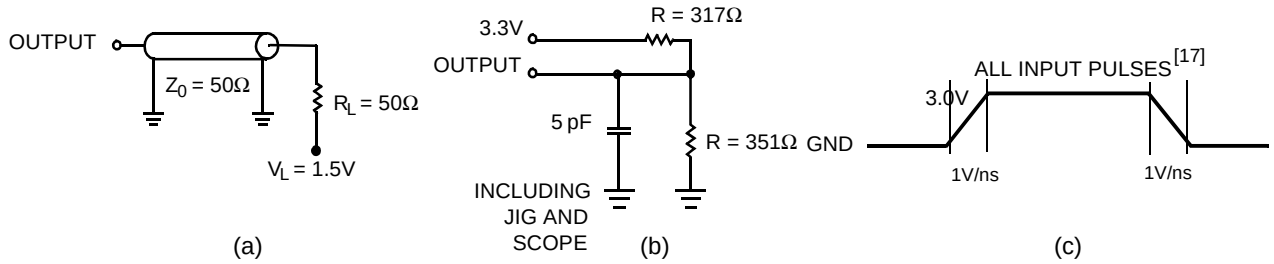
Capacitance[16]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V, V_{CCQ} = 3.3V	8	pF
C_{CLK}	Clock input capacitance		9	pF

Notes:

10. Minimum voltage equals –2.0V for pulse duration less than 20 ns.
11. T_A is the case temperature.
12. Power supply ramp up should be monotonic.
13. Overshoot: V_{IH} ≤ +6.0V for t ≤ $t_{KC/2}$.
14. Undershoot: V_{IL} ≤ –2.0V for t ≤ $t_{KC/2}$.
15. "Device Deselected" means the device is in power-down mode as defined in the truth table.
16. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms[17, 18]



Thermal Resistance

Parameter	Description	Test Conditions	TQFP Typ.	Units	Notes
Θ_{JA}	Thermal Resistance (Junction to Ambient)	(@200lfm) Single-layer printed circuit board	40	°C/W	15
Θ_{JC}	Thermal Resistance (Junction to Ambient)	(@200lfm) Four-layer printed circuit board	35	°C/W	15
Θ_{JA}	Thermal Resistance (Junction to Board)	Bottom	23	°C/W	15
Θ_{JC}	Thermal Resistance (Junction to Case)	Top	9	°C/W	15

Notes:

17. AC test conditions assume a signal transition time of 1 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading shown in part (a) of AC Test Loads.
18. Overshoot: VIH(AC) <VDD + 1.5V for t <tTCYC/2; undershoot: VIL(AC) < 0.5V for t <tTCYC/2; power-up: VIH < 2.6V and VDD <2.4V and VDDQ < 1.4V for t<200 ms.

Switching Characteristics Over the Operating Range[17, 19, 20]

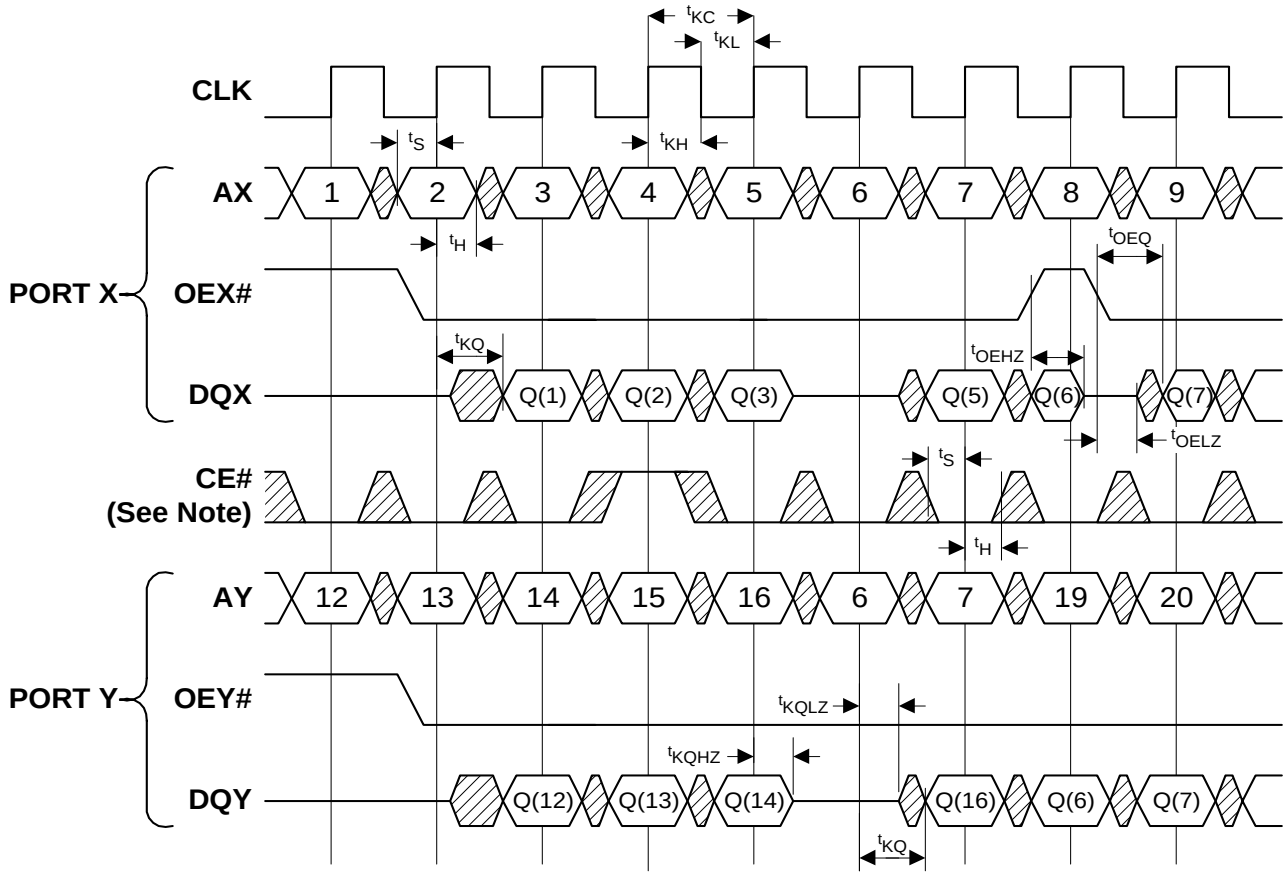
Parameter	Description	-100		-83		Unit
		Min.	Max.	Min.	Max.	
Clock						
t_{KC}	Clock cycle time	10		12		ns
t_{KH}	Clock HIGH time	3.5		4.0		ns
t_{KL}	Clock LOW time	3.5		4.0		ns
Output times						
t_{KQ}	Clock to output valid		5.0		6.0	ns
t_{KQX}	Clock to output invalid	1.5		1.5		ns
t_{KQLZ}	Clock to output in Low-Z[21]	0		0		ns
t_{KQHZ}	Clock to output in High-Z[21]		3.0		3.0	ns
t_{OEQ}	$\overline{OEX}$/$\overline{OEY}$ to output valid		5.0		6.0	ns
t_{OELZ}	$\overline{OEX}$/$\overline{OEY}$ to output in Low-Z[21]	0		0		ns
t_{OEHZ}	$\overline{OEX}$/$\overline{OEY}$ to output in High-Z[21]		3.0		3.0	ns
Set-up times						
t_S	Addresses, controls, and data In	1.8		2.0		ns
Hold times						
t_H	Addresses, controls, and data In	0.5		0.5		ns

Notes:

19. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions, as shown in part (a) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
20. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but rather reflect parameters guaranteed over worst-case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

Switching Waveforms [22]

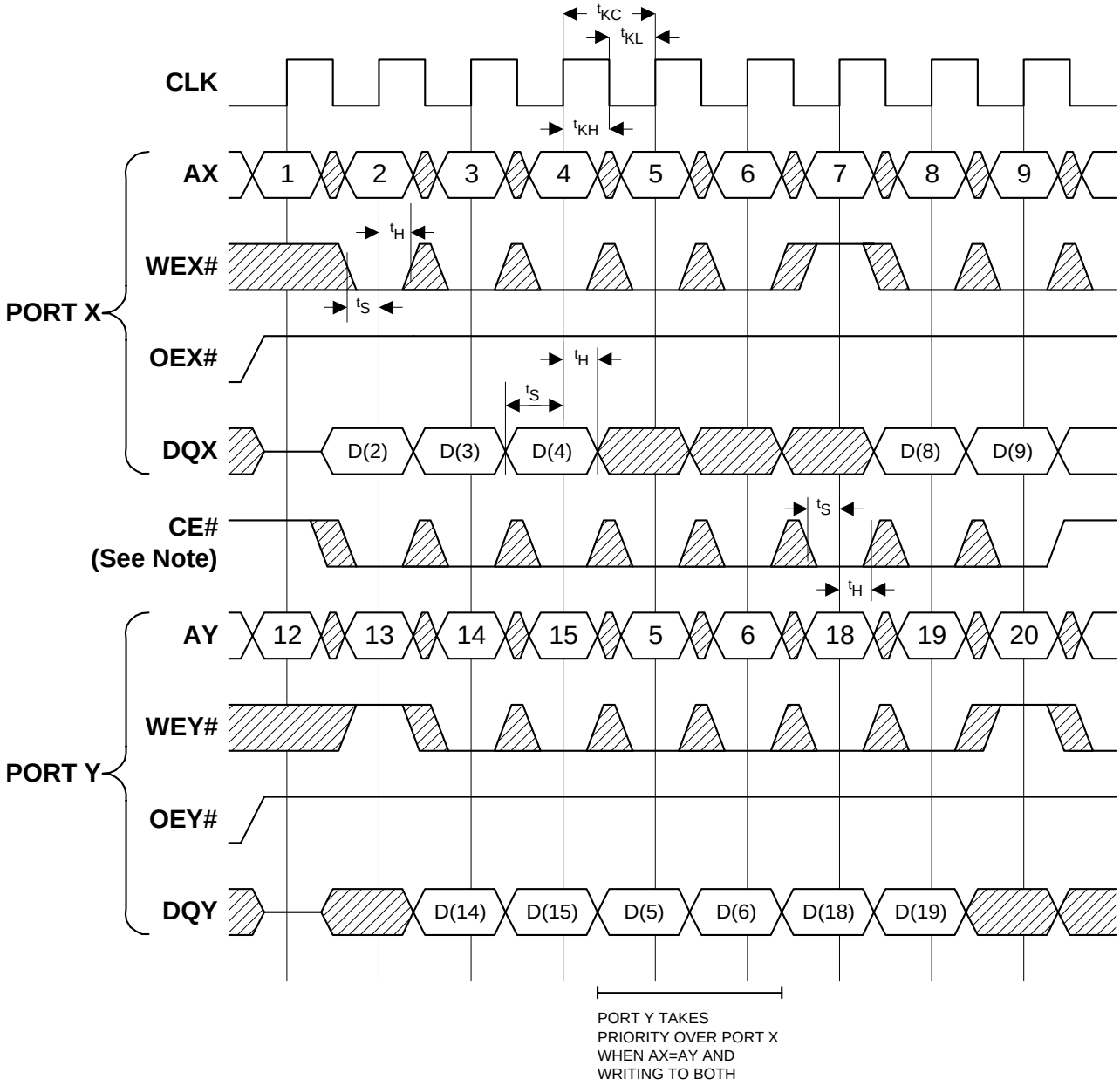
Read Cycle Timing from Both Ports (WEX, WEY, PTX, PTY HIGH)[22]



22. $\overline{CE}$ LOW means ($\overline{CE1X}$ and $\overline{CE1Y}$) equals LOW and (CE2X and CE2Y) equals HIGH. $\overline{CE}$ HIGH means ($\overline{CE1X}$ and $\overline{CE1Y}$) equals HIGH or (CE2X and CE2Y) equals LOW.

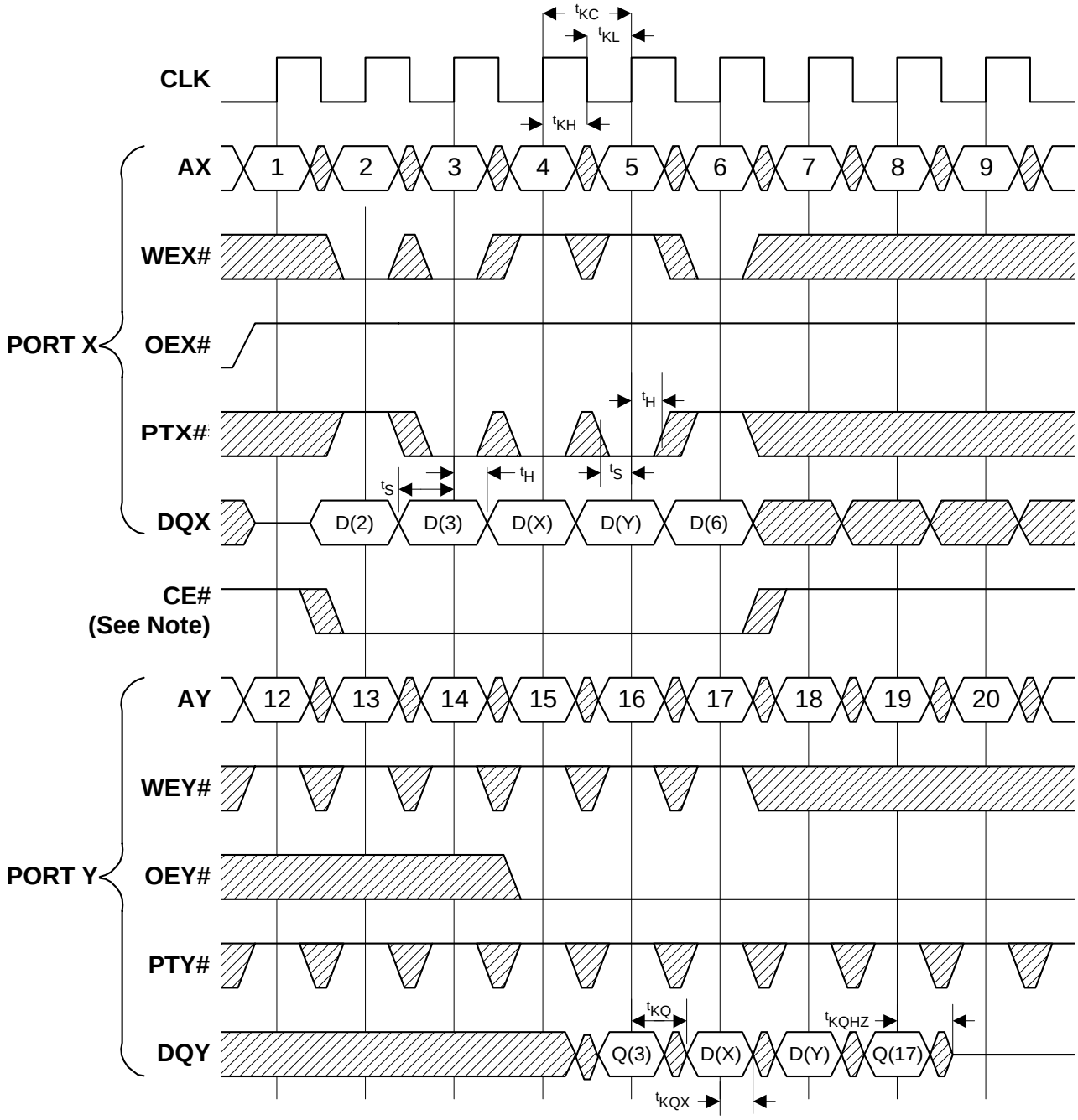
Switching Waveforms (continued)[22]

Write Cycle Timing to Both Ports (PTX, PTY HIGH)[21]



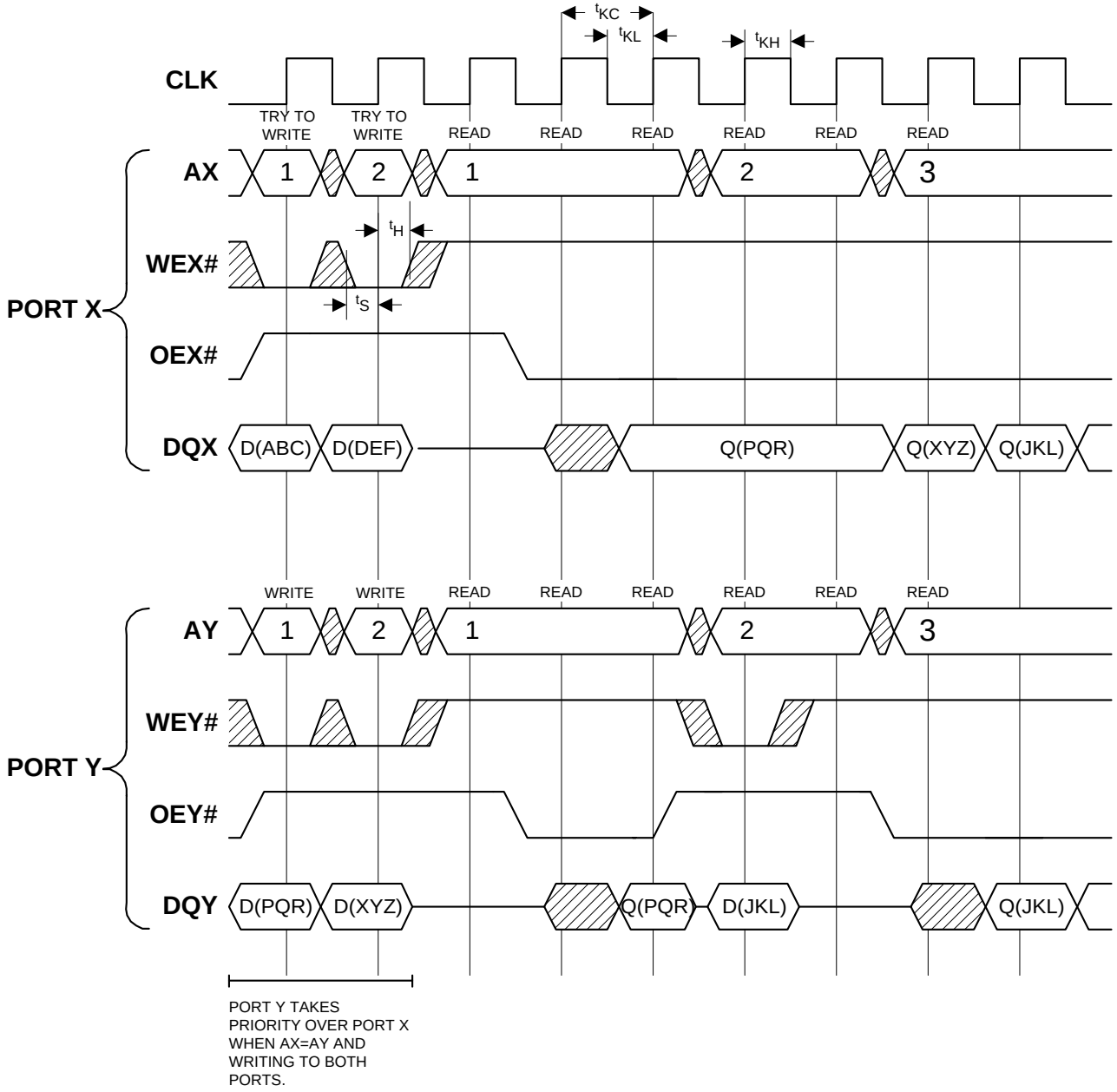
Switching Waveforms (continued)[22]

Write to Port X and Pass-through to Port Y[21]



Switching Waveforms (continued)[22]

Combination Read/Write with Same Address on Each Port



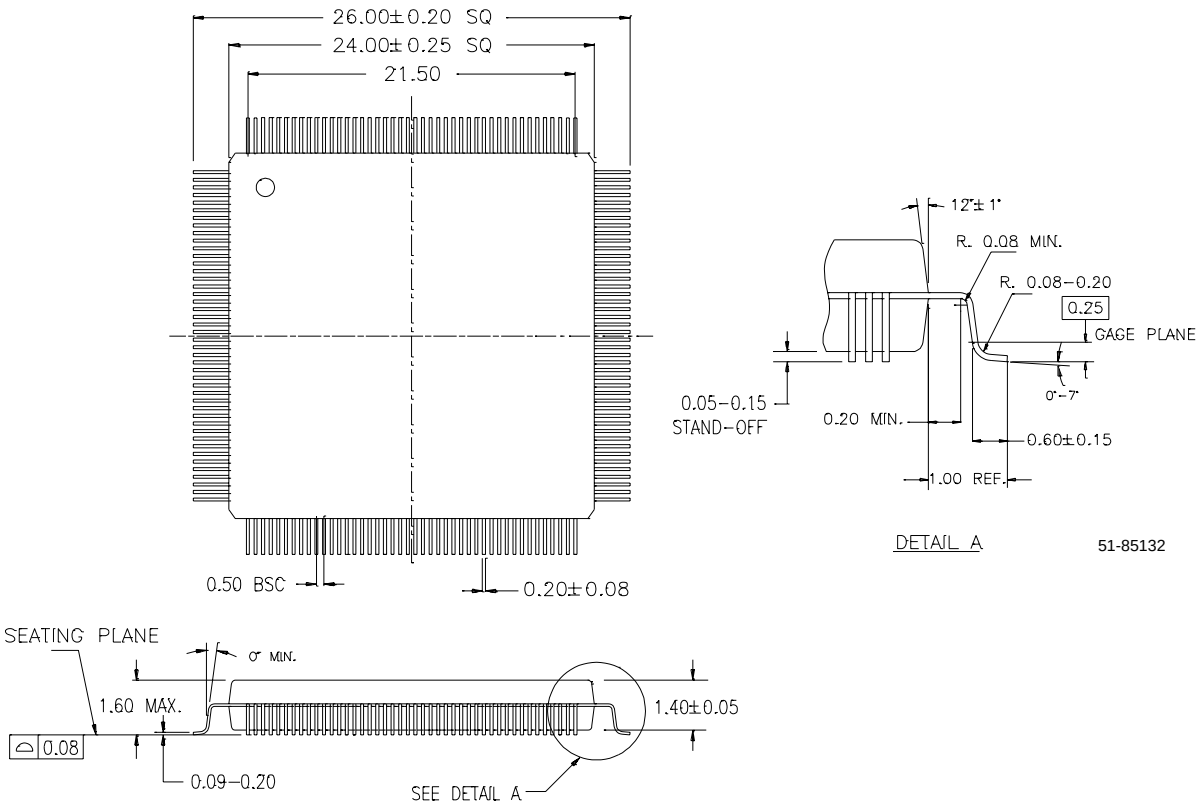
PTX# = PTY# = HIGH
D(Value) = Value is the input of the data port.
Q(Value) = Value is the output of the data port.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C1300A-100AC	AC	176-lead TQFP	Commercial
83	CY7C1300A-83AC			

Package Diagram

176-lead Thin Quad Flat Pack (24 × 24 × 1.4 mm) A176



Document Title: CY7C1300A 128K x 36 Dual I/O Dual Address Synchronous SRAM Document Number: 38-05075				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107304	06/08/01	NSL	New Data Sheet
*A	109296	10/31/01	CJM	1. Removed 133 MHz speed bin 2. Changed ESD voltage from >2001V to >1601V 3. Changed t_S from 1.5 ns to 1.8 ns (only 100 MHz) 4. Changed I_{SB} from 100 mA to 120 mA (All speeds) 5. Changed C_{IN} from 6 pF to 8 pF (All speeds) 6. Changed C_{CLK} from 6 pF to 9 pF (All speeds) 7. Changed I_{CC} to reflect char data (All speeds) 8. Changed ordering code from CY7C1301A to CY7C1300A (All speeds) 9. Removed Preliminary
*B	113017	04/09/02	KOM	Changed I_{CC} values on first page to correct value (500 and 430). Also updated Logic Block Diagram.
*C	123844	01/19/03	AJH	Updated power-up requirements in Operating Range and in AC Test Loads and Waveforms.