



F100102

Quint 2-Input OR/NOR Gate

General Description

The F100102 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 k Ω pull-down resistors and all outputs are buffered.

Refer to the F100302 datasheet for:

PCC packaging

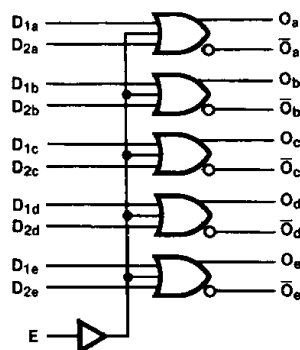
Lower power

Military versions

Extended voltage specs (–4.2V to –5.7V)

Ordering Code: See Section 8

Logic Symbol



TL/F/9836–3

Pin Names	Description
$D_{1a}-D_{1e}$	Data Inputs
E	Enable Input
O_a-O_e	Data Outputs
$\bar{O}_a-\bar{O}_e$	Complementary Data Outputs

TABLE 1. F100102 Truth Table

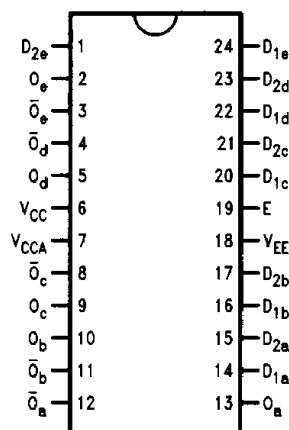
D_{1x}	D_{2x}	E	O_x	$\bar{O}_x$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

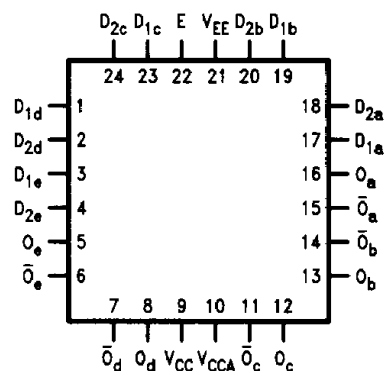
Connection Diagrams

24-Pin DIP



TL/F/9836–1

24-Pin Quad Cerpak



TL/F/9836–2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin

-7.0V to $+0.5\text{V}$

Input Voltage (DC)

V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH)

-50 mA

Operating Range (Note 2)

-5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V _{IN} = V _{IH(Max)} or V _{IL(Min)}	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1810	−1705	−1620	mV		
V _{OHC}	Output HIGH Voltage	−1035			mV	V _{IN} = V _{IH(Min)} or V _{IL(Max)}	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1610	mV		
V _{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL(Min)}	

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1020		−870	mV	V _{IN} = V _{IH(Max)} or V _{IL(Min)}	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1810		−1605	mV		
V _{OHC}	Output HIGH Voltage	−1030			mV	V _{IN} = V _{IH(Min)} or V _{IL(Max)}	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1595	mV		
V _{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL(Min)}	

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	− 1035		− 880	mV	V _{IN} = V _{IH(Max)} or V _{IL(Min)}	Loading with 50Ω to − 2.0V
V _{OL}	Output LOW Voltage	− 1830		− 1620	mV		
V _{OHC}	Output HIGH Voltage	− 1045			mV	V _{IN} = V _{IH(Min)} or V _{IL(Max)}	Loading with 50Ω to − 2.0V
V _{OLC}	Output LOW Voltage			− 1610	mV		
V _{IH}	Input HIGH Voltage	− 1165		− 880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	− 1830		− 1490	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL(Min)}	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ to -4.8V unless otherwise specified, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current Data Enable			350 300	μA	$V_{IN} = V_{IH(\text{Max})}$
I_{EE}	Power Supply Current	-80	-55	-38	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

$V_{EE} = -4.2\text{V}$ to -4.8V , $V_{CC} = V_{CCA} = \text{GND}$

Symbol	Parameter	$T_C = 0^\circ\text{C}$		$T_C = +25^\circ\text{C}$		$T_C = +85^\circ\text{C}$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.35	0.45	1.15	0.45	1.40	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.95	2.15	0.95	2.15	0.95	2.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.20	ns	

Cerpak AC Characteristics

$V_{EE} = -4.2\text{V}$ to -4.8V , $V_{CC} = V_{CCA} = \text{GND}$

Symbol	Parameter	$T_C = 0^\circ\text{C}$		$T_C = +25^\circ\text{C}$		$T_C = +85^\circ\text{C}$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.15	0.45	0.95	0.45	1.20	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.95	1.95	0.95	1.95	0.95	2.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.10	ns	

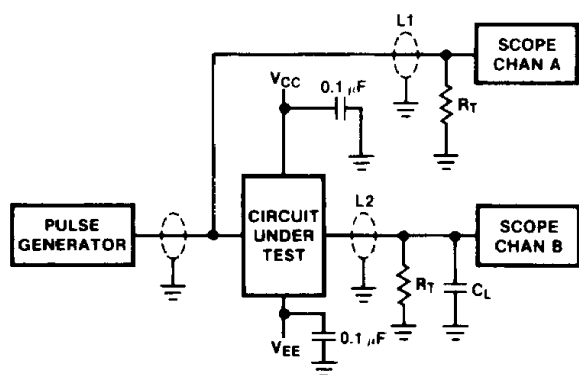


FIGURE 1. AC Test Circuit

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Notes:

$V_{CC}, V_{CCA} = +2\text{V}$, $V_{EE} = -2.5\text{V}$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1\mu\text{F}$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 C_L = Fixture and stray capacitance $\leq 3\text{ pF}$

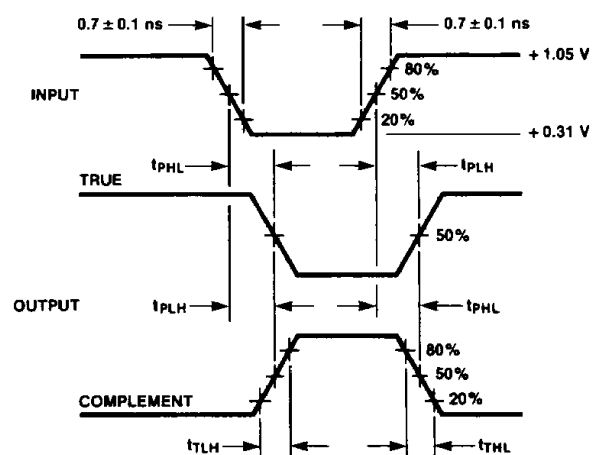


FIGURE 2. Propagation Delay and Transition Times

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