NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ZL2006

Data Sheet | February 23, 2011 | FN6848.2

Digital-DC™ Integrated Power Management and Conversion IC

Description

The ZL2005 is an innovative mixed-signal power management and conversion IC that combines a compact, efficient, synchronous DC/DC buck controller, adaptive drivers and key power and thermal management functions in one IC, providing flexibility and scalability while decreasing board space requirements and design complexity. Zilker Labs' Digital-DC technology enables a unique blend of performance and features not available in either traditional analog or newer digital approaches, resolving the issues associated with providing multiple, low-voltage power domains on a single PCB.

The ZL2005 is designed to be a flexible building block for DC power and can be easily adapted to designs ranging from a single-phase power supply operating from a 3.3 V input to a multi-phase supply operating from a 12 V input. The ZL2005 eliminates the need for complicated power supply managers as well as numerous external discrete components.

All operating features can be configured by simple pin-strap selection, resistor selection or through the on-board serial port. The PMBus™-compliant ZL2005 uses the SMBus™ serial interface for communication with other Digital-DC products or a host controller.

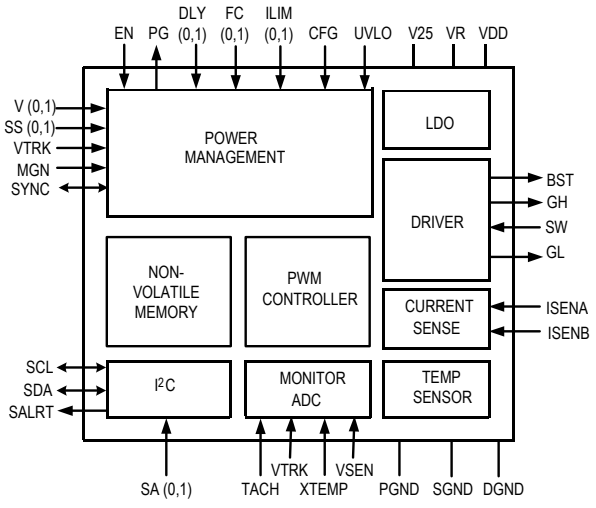


Figure 1. Block Diagram

Features

Power Management

- Digital soft start/stop
- Precision delay and ramp-up
- Power good/enable
- Voltage tracking, sequencing and margining
- Voltage/current/temperature monitoring
- I^2C/SMBus communication
- Output overvoltage and overcurrent protection
- PMBus compliant

Power Conversion

- Efficient synchronous buck controller
- 3 V to 14 V input range
- 0.6 V to 5.5 V output range
- ± 1% output accuracy
- Internal 3 A drivers support >30 A power stage
- Fast load transient response
- Phase interleaving
- RoHS compliant (6 x 6 mm) QFN package

Applications

- Servers/storage equipment
- Telecom/datacom equipment
- Power supplies (memory, DSP, ASIC, FPGA)
- Point of load converters

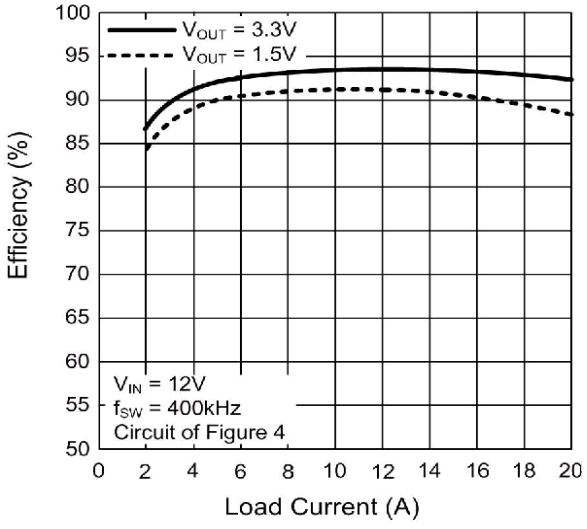


Figure 2. Efficiency vs. Load Current

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1 Electrical Characteristics

Table 1. Absolute Maximum Ratings

Operating beyond these limits may cause permanent damage to the device. Functional operation beyond the recommended operating conditions is not implied. Unless otherwise specified, all voltages are measured with respect to SGND.

Parameter	Pin(s)	Value	Unit
DC supply voltage	VDD	-0.3 to 17	V
Logic I/O voltage	DLY(0,1), EN, ILIM(0,1), MGN, PG, SA(0,1), SALRT, SCL, SDA, SS(0,1), SYNC, TACH, UVLO, V(0,1)	-0.3 to 6.5	V
Analog input voltages	ISENB, VSEN, VTRK, XTEMP,	-0.3 to 6.5	V
	ISENA	-1.5 to +30	V
MOSFET drive reference	VR	-0.3 to 6.5	V
		120	mA
Logic reference	V25	-0.3 to 3	V
		120	mA
High-side supply voltage	BST	-0.3 to +30	V
High-side drive voltage	GH	(V_{SW} - 0.3) to (V_{BST}+0.3)	V
Low-side drive voltage	GL	(PGND-0.3) to (VR+0.3+PGND)	V
Boost to switch differential voltage (V_{BST} - V_{SW})	BST, SW	-0.3 to 8	V
Switch node continuous	SW	(PGND-0.3) to 30	V
Switch node transient (<100 ns)	SW	(PGND-5) to 30	V
Ground voltage differential (V_{DGND}-V_{SGND}), (V_{PGND}-V_{SGND})	DGND, SGND, PGND	-0.3 to +0.3	V
Junction temperature	–	-55 to 150	^{o}C
Storage temperature range	–	-55 to 150	^{o}C
Lead temperature (soldering, 10 s)	–	300	^{o}C
ESD HBM tolerance (100 pF, 1.5 kΩ)	All	2	kV

Table 2. Recommended Operating Conditions and Thermal Information

Parameter	Symbol	Min	Typ	Max	Unit
Input Supply Voltage Range, V_{DD}	V_R tied to V_{DD} (Figure 9)	3.0	–	5.5	V
	V_R floating (Figure 9)	4.5	–	14	V
Output Voltage Range	V_{OUT}	0.6		5.5	V
Operating Junction Temperature Range	T_J	-40	–	125	°C
Junction to Ambient Thermal Impedance[1]	Θ_{JA}	–	35	–	°C/W
Junction to Case Thermal Impedance[2]	Θ_{JC}	–	5	–	°C/W

NOTES:

1. Θ_{JA} is measured in free air with the device mounted on a multi-layer FR4 test board and the exposed metal pad soldered to a low impedance ground plane using multiple vias.
2. For Θ_{JC}, the "case" temperature is measured at the center of the exposed metal pad

Table 3. Electrical Specifications

Unless otherwise specified V_{DD} = 12 V, T_A = -40°C to +85°C. Typical values are at T_A = 25°C.

Parameter	Condition	Min[5]	Typ	Max[5]	Unit
Input and Supply Characteristics					
Supply current (I_{DD}) (No load on GH and GL)	f_{SW} = 200 kHz	–	16	30	mA
	f_{SW} = 2,000 kHz	–	25	50	mA
Standby supply current (I_{DD})	EN = Low no I^2C/SMBus activity	–	2	5	mA
VR reference voltage (V_R)	$V_{DD} \geq 6$ V $I_{VR} < 50$ mA	4.5	5.2	5.5	V
V25 reference voltage (V_{25})	$V_R \geq 3$ V $I_{V25} < 50$ mA	2.25	2.5	2.75	V
Output Characteristics					
Output voltage adjustment range		0.6	–	5.5	V
Output voltage setpoint resolution	Set using resistors	–	10	–	mV
	Set using I^2C/SMBus	–	±0.025	–	% of F.S.[1]
Output voltage accuracy	Over line, load and temperature	-1	–	1	%
VSEN input bias current	VSEN = 5.5 V	–	110	200	µA
Current sense differential input voltage (ground referenced)	V_{ISENA} - V_{ISENB}	-100	–	100	mV
Current sense differential input voltage (V_{OUT} referenced)	V_{ISENA} - V_{ISENB}	-100	–	100	mV
Current sense input bias current	Ground referenced	-100	–	100	µA

NOTE:

1. Percentage of Full Scale (F.S.) with temperature compensation applied

Current sense input bias current (V_{OUT} referenced, V_{OUT} <= 3.6V)	ISENA	-1	–	1	µA
	ISENB	-100	–	100	µA

Table 3. Electrical Specifications

Unless otherwise specified V_{DD} = 12 V, T_A = -40°C to +85°C. Typical values are at T_A = 25°C. (Continued)

Parameter	Condition	Min[5]	Typ	Max[5]	Unit
Soft start delay duration range	Set using DLY pin or resistor	7	–	200	ms
	Configurable via I^2C/SMBus	0.007	–	500	s
Soft start delay duration accuracy		–	6	–	ms
Soft start ramp duration range	Set using SS pin or resistor	0	–	200	ms
	Configurable via I^2C/SMBus	0	–	200	ms
Soft start ramp duration accuracy		–	100	–	µs
Logic Input/Output Characteristics					
Logic input bias current	EN, PG, SCL, SDA, SALRT, TACH	-10	–	10	µA
	During configuration restore	-1	–	1	mA
MGN input bias current		-1	–	1	mA
Logic input low threshold (V_{IL})		–	–	0.8	V
Logic input OPEN (N/C)	Multi-mode logic pins	–	1.4	–	V
Logic input high threshold (V_{IH})		2	–	–	V
Logic output low (V_{OL})	I_{OL} <= 4 mA	–	–	0.4	V
Logic output high (V_{OH})	I_{OH} >= - 2 mA	2.25	–	–	V
Oscillator and Switching Characteristics					
Switching frequency range		200	–	2000	kHz
Switching frequency setpoint accuracy	Predefined settings (See table 14)	-5	–	5	%
Maximum PWM duty cycle	Factory default	95	–	–	%
Minimum SYNC pulse width		150	–	–	ns
Input clock frequency drift tolerance	External clock signal	-13	–	13	%
Tachometer Characteristics					
TACH pulse width		150	–	–	ns
TACH frequency range		1	–	500	Hz
TACH accuracy		-10	–	10	%

Table 3. Electrical Specifications

Unless otherwise specified V_{DD} = 12 V, T_A = -40°C to +85°C. Typical values are at T_A = 25°C. (Continued)

Parameter	Condition	Min[5]	Typ	Max[5]	Unit
Gate Drivers					
High-side driver voltage (V_{BST} - V_{SW})		–	4.5	–	V
High-side driver peak gate drive current (pull down)	(V_{BST} - V_{SW}) = 4.5 V	2	3	–	A
High-side driver pull-up resistance	(V_{BST} - V_{SW}) = 4.5 V, (V_{BST} - V_{GH}) = 50 mV	–	0.8	2	Ω
High-side driver pull-down resistance	(V_{BST} - V_{SW}) = 4.5 V, (V_{GH} - V_{SW}) = 50 mV	–	0.5	2	Ω
Low-side driver peak gate drive current (pull-up)	V_R = 5 V	–	2.5	–	A
Low-side driver peak gate drive current (pull-down)	V_R = 5 V	–	1.8	–	A
Low-side driver pull-up resistance	V_R = 5 V, (V_R - V_{GL}) = 50 mV	–	1.2	2	Ω
Low-side driver pull-down resistance	V_R = 5 V, (V_{GL} - PGND) = 50 mV	–	0.5	2	Ω
Switching timing					
GH rise and fall time	(V_{BST} - V_{SW}) = 4.5 V, C_{LOAD} = 2.2 nF	–	5	20	ns
GL rise and fall time	V_R = 5 V, C_{LOAD} = 2.2 nF	–	5	20	ns
Tracking					
VTRK input bias current	VTRK = 5.5 V	–	110	200	µA
VTRK tracking threshold	VTRK >= 0.3 V	– 100		+ 100	mV

Table 3. Electrical Specifications

Unless otherwise specified V_{DD} = 12 V, T_A = -40°C to +85°C. Typical values are at T_A = 25°C. (Continued)

Parameter	Condition	Min[5]	Typ	Max[5]	Unit
Fault Protection Characteristics					
UVLO threshold range		2.85	–	16	V
UVLO setpoint accuracy		-150	–	150	mV
UVLO hysteresis	Factory default	–	3	–	%
	Configurable via I²C/SMBus	0	–	100	%
UVLO delay		–	–	2.5	µs
Power good V_{OUT} low threshold	Factory default	–	90	–	% V_{OUT}
Power good V_{OUT} high threshold	Factory default	–	115	–	% V_{OUT}
Power good V_{OUT} hysteresis	Factory default	–	5	–	%
Power good delay	Set using pin-strap or resistor[4]	0	–	200	ms
	Configurable via I²C/SMBus	0	–	500	s
VSEN undervoltage threshold	Factory default		85	–	% V_{OUT}
	Configurable via I²C/SMBus	0	–	110	% V_{OUT}
VSEN overvoltage threshold	Factory default		115	–	% V_{OUT}
	Configurable via I²C/SMBus	0	–	115	% V_{OUT}
VSEN undervoltage/overvoltage fault response time	Factory default	–	16	–	µs
	Configurable via I²C/SMBus	5	–	60	µs
Current limit setpoint accuracy (V_{OUT} referenced)		–	±10	–	% F.S.[1]
Current limit setpoint accuracy[2] (Ground referenced)	$\lvert V_{ISENA} - V_{ISENB} \rvert > 12$ mV	–	±10	–	% F.S.
Current limit protection delay	Factory default	–	5	–	τ_{SW}[3]
	Configurable via I²C/SMBus	1	–	32	
Temperature compensation of current limit protection threshold	Factory default	–	4400	–	ppm/°C
	Configurable via I²C/SMBus	100	–	12700	
Thermal protection threshold	Factory default	–	125	–	°C
	Configurable via I²C/SMBus	- 40	–	125	°C
Thermal protection hysteresis		–	15	–	°C

NOTES:

1. Percentage of Full Scale (F.S.) with temperature compensation applied
2. T_A = 0°C to +85°C
3. $\tau_{SW} = 1/f_{SW}$, f_{SW} switching frequency
4. Automatically set to same value as soft start ramp time
5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

2 Pin Descriptions

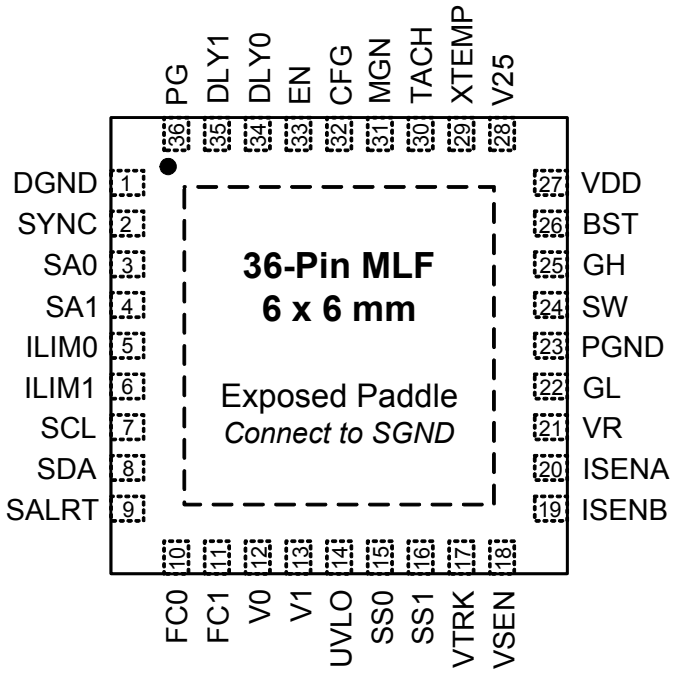


Figure 3. Pin Assignments (top view)

Table 4. Pin Descriptions

Pin	Label	Type[1]	Description
1	DGND	PWR	Digital ground. Connect to low impedance ground plane.
2	SYNC	I/O, M[2]	Clock synchronization input. Used to set the frequency of the internal switch clock, to sync to an external clock or to output internal clock.
3	SA0	I, M	Serial address select pins. Used to assign unique address for each individual device or to enable certain management features.
4	SA1		
5	ILIM0	I, M	Current limit select. Sets the overcurrent threshold voltage for ISENA, ISENB.
6	ILIM1		
7	SCL	I/O	Serial clock. Connect to external host and/or to other ZL2005s.
8	SDA	I/O	Serial data. Connect to external host and/or to other ZL2005s.
9	SALRT	O	Serial alert. Connect to external host if desired.
10	FC0	I	Loop compensation selection pins.
11	FC1	I	
12	V0	I, M	Output voltage selection pins. Used to set V_{OUT} setpoint and V_{OUT} max.
13	V1		
14	UVLO	I, M	Undervoltage lockout selection. Sets the minimum value for V_{DD} voltage to enable V_{OUT}.

NOTES:

1. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pin (refer to Section 4.4, “Multi-mode Pins,”)
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.
3. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

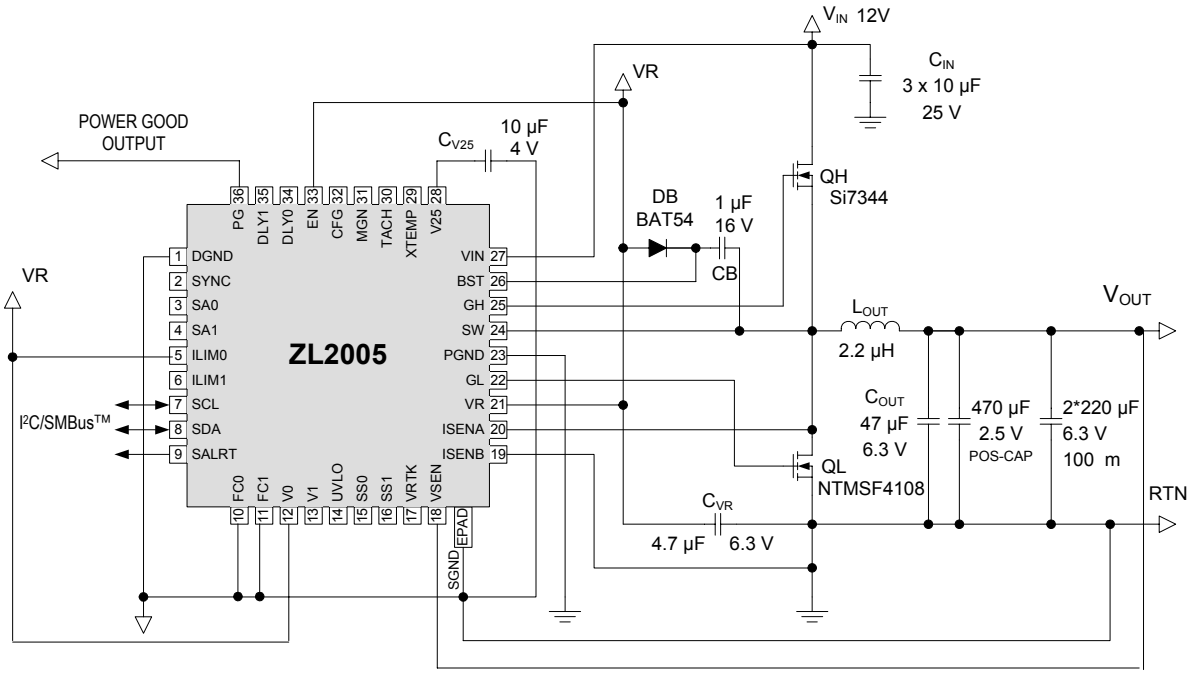
Table 4. Pin Descriptions (Continued)

Pin	Label	Type[1]	Description
15	SS0	I, M	Soft start pins. Set the output voltage ramp time during turn-on and turn-off.
16	SS1		
17	VTRK	I	Tracking sense input. Used to track an external voltage source.
18	VSEN	I	Output voltage feedback. Connect to output regulation point.
19	ISENB	I	Differential voltage input for current limit.
20	ISENA	I	Differential voltage input for current limit. High voltage tolerant.
21	VR	PWR	Internal 5V reference used to power internal drivers.
22	GL	O	Low side FET gate drive.
23	PGND	PWR	Power ground. Connect to low impedance ground plane.
24	SW	PWR	Drive train switch node.
25	GH	O	High-side FET gate drive.
26	BST	PWR	High-side drive boost voltage.
27	VDD[3]	PWR	Supply voltage.
28	V25	PWR	Internal 2.5 V reference used to power internal circuitry.
29	XTEMP	I	External temperature sensor input. Connect to external 2N3904 diode connected transistor.
30	TACH	I	Tachometer input used to measure fan speed. Connect to TACH output of external fan.
31	MGN	I	Digital V_{OUT} margin control
32	CFG	I	Configuration pin. Used to control the switching phase offset, sequencing and other management features.
33	EN	I	Enable. Active signal enables PWM switching.
34	DLY0	I, M	Softstart delay select. Sets the delay from when EN is asserted until the output voltage starts to ramp.
35	DLY1		
36	PG	O	Power good output.
ePad	SGND	PWR	Exposed thermal pad. Connect to low impedance ground plane. Internal connection to SGND.

NOTES:

1. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pin (refer to Section 4.4, “Multi-mode Pins,”)
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.
3. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

3 Typical Application Example



Notes:

1. Conditions: V_{IN} = 12 V, V_{OUT} = 1.8 V, Freq = 400 kHz, I_{OUT} = 20 A
2. The I^2C/SMBus requires pullup resistors. Please refer to the I^2C/SMBus specifications for more details.

Figure 4. Typical Application Circuit

4 ZL2005 Overview

4.1 Digital-DC Architecture

The ZL2005 is an innovative mixed-signal power conversion and power management IC based on Zilker Labs' patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications. Its unique digital PWM loop utilizes an innovative mixed-signal topology to enable precise control of the power conversion process with no software required, resulting in a very flexible device that is also easy to use. An extensive set of power management functions is fully integrated and can be configured using simple pin connections or via the I^2C/SMBus hardware interface using standard PMBus commands. The user configuration can be saved in an on-chip non-volatile memory (NVM), allowing ultimate flexibility.

Once enabled, the ZL2005 is immediately ready to regulate power and perform power management tasks with no programming required. The ZL2005 can be configured by simply connecting its pins according to the tables provided in this document. Advanced configuration options and real-time configuration changes are available via the I^2C/SMBus interface if desired, and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any supply between 3V and 14V with no secondary bias supplies needed.

Zilker Labs provides a comprehensive set of on-line tools and application notes to assist with power supply design and simulation. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a stand-alone platform using pin configuration settings. Additionally, a Windows™-based GUI is provided to enable full configuration and monitoring capability via the I^2C/SMBus interface using an available computer and the included USB cable.

Please refer to www.zilkerlabs.com for access to the most up-to-date documentation and the PowerPilot™ simulation tool, or call your local Zilker Labs' sales office to order an evaluation kit.

4.2 Power Conversion Overview

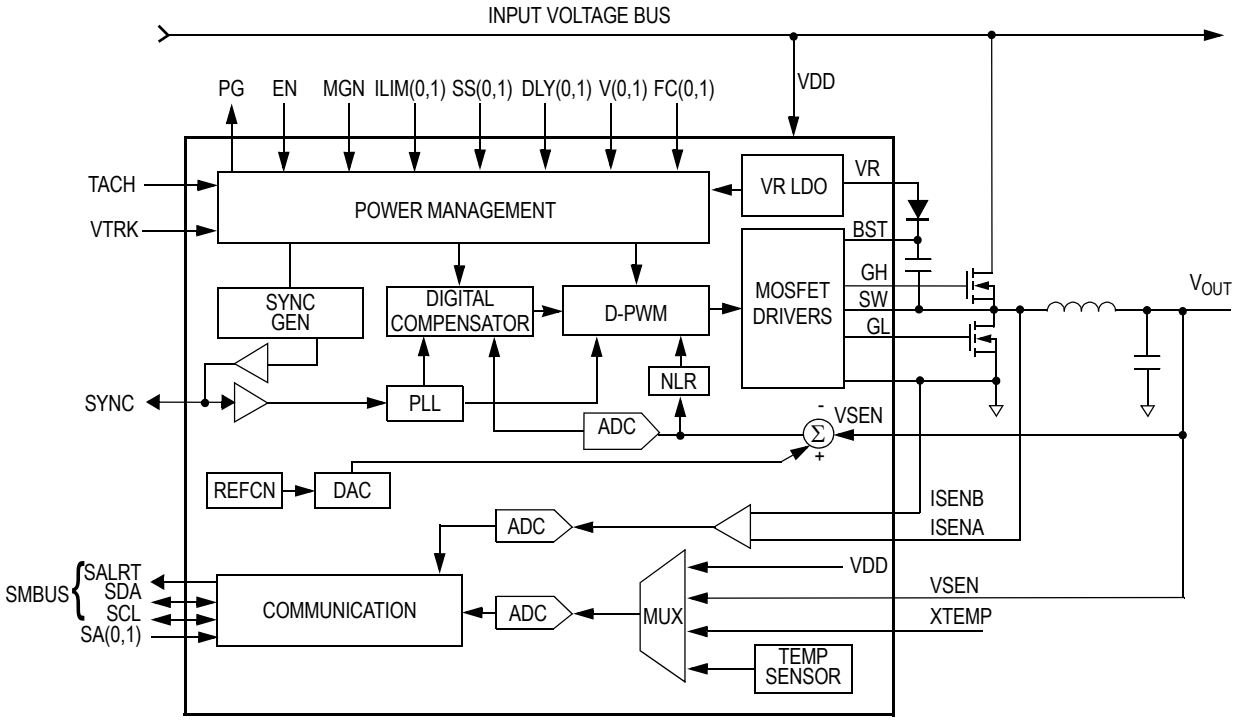


Figure 5. ZL2005 Detailed Block Diagram

The ZL2005 operates as a voltage-mode, synchronous buck converter with a selectable, constant frequency Pulse Width Modulator (PWM) control scheme that uses external MOSFETs, inductor and capacitors to perform power conversion.

Figure 6 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage.

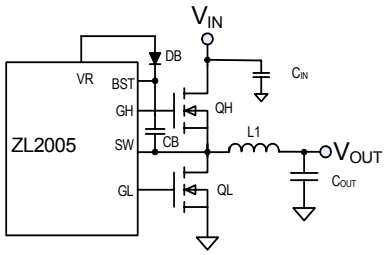


Figure 6. Synchronous Buck Converter

In its most simple configuration, the ZL2005 requires two external N-channel power MOSFETs, one for the top control MOSFET (QH) and one for the bottom synchronous MOSFET (QL). The amount of time that QH is on as a fraction of the total switching period is known as the duty cycle *D*, which is described by the following equation:

$$D \approx \frac{VOUT}{VIN}$$

During time D, QH is on and $V_{IN} - V_{OUT}$ is applied across the inductor. The current ramps up as shown in Figure 7.

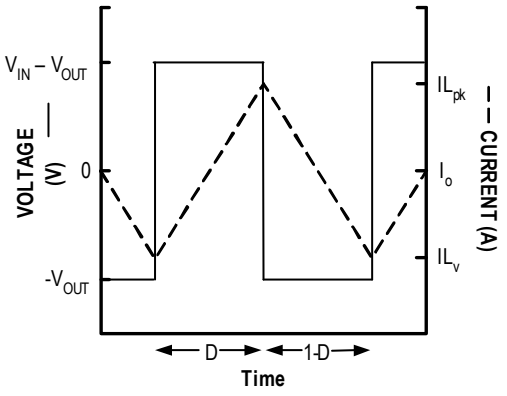


Figure 7. Inductor Waveform

When QH turns off (time 1-D), the current flowing in the inductor must continue to flow from the ground up through QL, during which the current ramps down. Since the output capacitor C_{OUT} exhibits a low impedance at the switching frequency, the AC component of the inductor current is filtered from the output voltage so the load sees nearly a DC voltage.

Typically, buck converters specify a maximum duty cycle that effectively limits the maximum output voltage that can be realized for a given input voltage. This duty cycle limit ensures that the low-side MOSFET is allowed to turn on for a minimum amount of time during each switching cycle, which enables the bootstrap capacitor (CB in Figure 6) to be charged up and provide adequate gate drive voltage for the high-side MOSFET. See Section 5.2, “High-side Driver Boost Circuit,” for more details.

In general, the size of components L1 and C_{OUT} as well as the overall efficiency of the circuit are inversely proportional to the switching frequency, f_{SW}. Therefore, the highest efficiency circuit may be realized by switching the MOSFETs at the lowest possible frequency; however, this will result in the largest component size. Conversely, the smallest possible footprint may be realized by switching at the fastest possible frequency but this gives a somewhat lower efficiency. Each user should determine the optimal combination of size and efficiency when determining the switching frequency for each application.

The block diagram for the ZL2005 is illustrated in Figure 5. In this circuit, the target output voltage is regulated by connecting the VSEN pin directly to the output regulation point. The VSEN signal is then compared to a reference voltage that has been set to the desired output voltage level by the user. The error signal derived from this comparison is converted to a digital value with a low-resolution, analog to digital (A/D) converter. The digital signal is applied to an adjustable digital compensation filter, and the compensated signal is used to derive the appropriate PWM duty cycle for driving the external MOSFETs in a way that produces the desired output.

The ZL2005 also incorporates a non-linear response (NLR) loop to reduce the response time and output deviation in response to a load transient. The ZL2005 has an efficiency optimization circuit that continuously monitors the power converter’s operating conditions and adjusts the turn-on and turn-off timing of the high-side and low-side MOSFETs to optimize the overall efficiency of the power supply.

4.3 Power Management Overview

The ZL2005 incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL2005 includes circuit protection features that continuously safeguard the load from damage due to unexpected system faults. The ZL2005 can continuously monitor input voltage, output voltage/current, internal temperature, and the temperature of an external thermal diode. A Power Good output signal is provided to enable power-on reset functionality for an external processor.

All power management functions can be configured using either simple pin configuration techniques (Figure 8) or via the I^2C/SMBus interface. Monitoring parameters can be pre-configured to provide alerts for specific conditions. See Application Note AN13 for more details on SMBus monitoring.

4.4 Multi-mode Pins

In order to simplify circuit design, the ZL2005 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device without requiring the user to program the IC. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 5. Any combination of connections is allowed among the multi-mode pins.

These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note AN13).

Table 5. Multi-mode Pin Configuration

Pin Tied To	Value
GND (Logic low)	< 0.8 VDC
OPEN (N/C)	No connection
HIGH (Logic high)	> 2.0 VDC
Resistor to GND	Set by resistor value

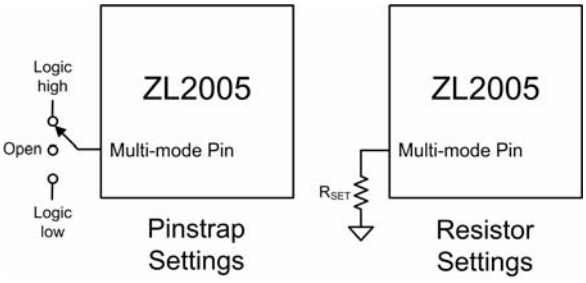


Figure 8. Pin-strap and Resistor Setting Examples

Pin-strap Settings: This is the simplest implementation method, as no external components are required. Using this method, each pin can take on one of three possible states: GND, OPEN, or HIGH. These pins can be connected to the VR or V25 pins for logic HIGH settings, as either pin provides a regulated voltage greater than 2V. Using a single pin, the user can select one of three settings, and using two pins, the user can select one of nine settings.

Resistor Settings: This method allows a greater range of adjustability when connecting a finite valued resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so that the device can reliably recognize the value of resistance connected to the pin while eliminating the errors associated with the resistor accuracy. A total of 25 unique selections are available using a single resistor.

I^2C/SMBus Settings: Almost any ZL2005 function can be configured via the I^2C/SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I^2C/SMBus. See Application Note AN13 for details.

5 Power Conversion Functional Description

5.1 Internal Bias Regulators and Input Supply Connections

The ZL2005 employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR: The VR LDO provides a regulated 5V bias supply for the MOSFET driver circuits. It is powered from the VDD pin and can supply up to 100mA output current. A 4.7 µF filter capacitor is required at the VR pin.

V25: The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node and can supply up to 50 mA output current. A 10 µF filter capacitor is required at the V25 pin.

Note: The internal bias regulators are designed for powering internal circuitry only. Do not attach external loads to any of these pins. The multi-mode pins may be connected to the VR or V25 pins for logic HIGH settings.

When the input supply (VDD) is higher than 5.5V, the VR pin should not be connected to any other pin. It should only have a filter capacitor attached as shown in Figure 9. Due to the dropout voltage associated with the VR bias regulator, the VDD pin must be connected to the VR pin for designs operating from a VDD supply from 3.0V to 5.5V. Figure 9 illustrates the required connections for both cases. For input supplies between 4.5V and 5.5V, either method can be used.

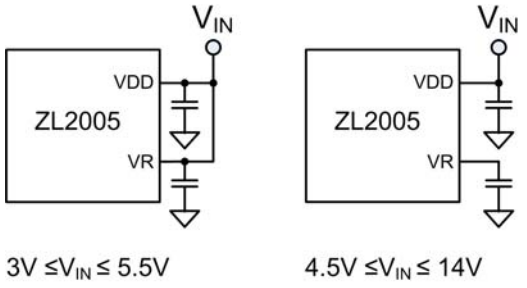


Figure 9. Input Supply Connections

5.2 High-side Driver Boost Circuit

The gate drive voltage for the upper MOSFET driver is generated by a floating bootstrap capacitor, CB (see Figure 4). When the lower MOSFET (QL) is turned on, the SW node is pulled to ground and the capacitor is charged from the internal VR bias regulator through diode DB. When QL turns off and the upper MOSFET (QH) turns on, the SW node is pulled up to V_{DD} and the voltage on the BST pin is boosted approximately 5V above V_{IN} to provide the necessary voltage for the high-side driver. A Schottky diode should be used for DB to maximize the high-side drive voltage.

5.3 Output Voltage Selection

The output voltage may be set to any voltage between 0.6V and 5.5V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. By connecting the V0 and V1 pins to logic high, logic low, or leaving them floating, V_{OUT} can be set to any of nine standard voltages as shown in Table 6.

Table 6. Pin-strap Output Voltage Settings

		V0		
		LOW	OPEN	HIGH
V1	LOW	0.6V	0.8V	1.0V
	OPEN	1.2V	1.5V	1.8V
	HIGH	2.5V	3.3V	5.0V

If an output voltage other than those in Table 6 is desired, the resistor setting method can be used. Using this method, resistors R0 and R1 are selected to produce a specific voltage between 0.6V and 5.5V in 10 mV steps. Resistor R1 provides a coarse setting and R0 a fine adjustment, thus eliminating the additional errors associated with using two 1% resistors in a standard analog implementation (this typically adds 1.4% error using two 1% resistors).

To set V_{OUT} using resistors, follow the steps below to calculate an index value and then use Table 7 to select the resistor that corresponds to the calculated index value as follows:

1. Calculate Index1:
   Index1 = 4 x V_{OUT}
2. Round the result down to the nearest whole number.
3. Select the value for R1 from Table 7 using the Index1 rounded value from step 2.
4. Calculate Index0 using equation
   Index0 = 100 x V_{OUT} - 25 x Index1
5. Select the value for R0 from Table 7 using Index0 from step 4.

Table 7. Resistors for Setting Output Voltage

Index	R0 or R1
0	10 kΩ
1	11 kΩ
2	12.1 kΩ
3	13.3 kΩ
4	14.7 kΩ
5	16.2 kΩ
6	17.8 kΩ
7	19.6 kΩ
8	21.5 kΩ
9	23.7 kΩ
10	26.1 kΩ
11	28.7 kΩ
12	31.6 kΩ

Index	R0 or R1
13	34.8 kΩ
14	38.3 kΩ
15	42.2 kΩ
16	46.4 kΩ
17	51.1 kΩ
18	56.2 kΩ
19	61.9 kΩ
20	68.1 kΩ
21	75 kΩ
22	82.5 kΩ
23	90.9 kΩ
24	100 kΩ

Example:

For V_{OUT} = 1.33V:

Index1 = 4 x 1.33V = 5.32 (5);

From Table 7, using Index = 5
R1 = 16.2 kΩ

Index0 = (100 x 1.33V) - (25 x 5) = 8;
From Table 7; R0 = 21.5 kΩ

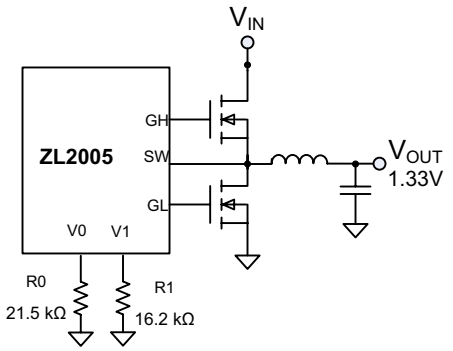


Figure 10. Output Voltage Resistor Setting Example

The output voltage may also be set to any value between 0.6V and 5.5V using the I^2C/SMBus interface. See Application Note AN13 for details.

5.4 Start-up Procedure

The ZL2005 follows a specific internal start-up procedure after power is applied to the VDD pin. Table 8 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock must be stable prior to asserting the EN pin. The device requires approximately 10-20 ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 6 ms before its output voltage may be allowed to start its ramp-up process. If a soft start delay period less than 6 ms has been configured (using the DLY (0,1) pins), the device will default to a 6 ms delay period. If a delay period of 6 ms or higher is configured, the device will wait for the configured delay period before starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time (using the SS (0,1) pins).

Table 8. ZL2005 Start-up Sequence

Step #	Step Name	Description	Time Duration
1	Power Applied	Input voltage is applied to the ZL2005's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 10-20 ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	—
5	Pre-ramp Delay	The device requires approximately 6 ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the Delay pins.	Approx. 6 ms

5.5 Soft Start Delay and Ramp Times

In some system applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its nominal value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its nominal value after the delay period has expired. The ZL2005 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods for V_{OUT}. These features may be used as part of an overall in-rush current management strategy or to precisely control how fast a load IC is turned on.

The soft start delay period begins when the Enable pin is asserted and ends when the delay time expires. The soft-start delay period is set using the DLY (0,1) pins.

The soft start ramp enables a controlled ramp to the nominal V_{OUT} value that begins once the delay period has timed out. The ramp-up is guaranteed monotonic and its slope may be precisely set by setting the soft-start ramp time using the SS (0,1) pins.

The soft start delay and ramp times can be set to standard values according to Table 9 and Table 10 respectively.

Table 9. Soft Start Delay Settings

		DLY0		
		LOW	OPEN	HIGH
DLY1	LOW	0 ms[1]	Reserved	
	OPEN	5 ms[1]	10 ms	20 ms
	HIGH	50 ms	100 ms	200 ms

NOTE:
1. When the device is set to 0 ms or 5 ms delay, it will begin its ramp up after the internal circuitry has initialized (approx. 6 ms).

Table 10. Soft Start Ramp Settings

		SS0		
		LOW	OPEN	HIGH
SS1	LOW	0 ms[1]	1 ms	2 ms
	OPEN	5 ms	10 ms	20 ms
	HIGH	50 ms	100 ms	200 ms

NOTE:
1. When the soft start ramp is set to zero, the device will ramp up as quickly as the internal circuitry and output load capacitance will allow.

If the desired soft start delay and ramp times are not one of the values listed in Table 8 and Table 9, the times can be set to a custom value by connecting a resistor from the DLY0 or SS0 pin to SGND using the appropriate resistor value from Table 11. The value of this resistor is measured upon start-up or Restore and will not change if this resistor is varied after power has been applied to the ZL2005. See Figure 11 for typical connections using resistors.

Note: Do not connect a resistor to the DLY1 or SS1 pin. These pins are not utilized for setting soft-start delay and ramp times. Connecting an external resistor to these pins may cause conflicts with other device settings.

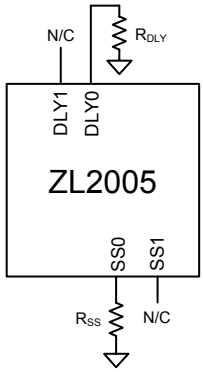


Figure 11. DLY and SS Pin Resistor Connections

Table 11. DLY and SS Resistor Values

DLY or SS	R_{DLY} or R_{SS}	DLY or SS	R_{DLY} or R_{SS}
0 ms	10 kΩ	110 ms	28.7 kΩ
10 ms	11 kΩ	120 ms	31.6 kΩ
20 ms	12.1 kΩ	130 ms	34.8 kΩ
30 ms	13.3 kΩ	140 ms	38.3 kΩ
40 ms	14.7 kΩ	150 ms	42.2 kΩ
50 ms	16.2 kΩ	160 ms	46.4 kΩ
60 ms	17.8 kΩ	170 ms	51.1 kΩ
70 ms	19.6 kΩ	180 ms	56.2 kΩ
80 ms	21.5 kΩ	190 ms	61.9 kΩ
90 ms	23.7 kΩ	200 ms	68.1 kΩ
100 ms	26.1 kΩ		

The soft start delay and ramp period can be set to custom values via the I^2C/SMBus interface. When the soft start delay is set to 0 ms, the device will begin its ramp up after the internal circuitry has initialized (approx. 6ms).

5.6 Power Good

The ZL2005 provides a Power Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within -10%/+15% of the target voltage These limits may be changed via the I^2C/SMBus interface. See Application Note AN13 for details.

A PG delay period is defined as the time from when all conditions within the ZL2005 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL2005 PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10 ms, the PG delay will be set to 10 ms. The PG delay may be set independently of the soft-start ramp using the I^2C/SMBus as described in Application Note AN13.

5.7 Switching Frequency and PLL

The ZL2005 incorporates an internal phase locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an internal oscillator or driven from an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock output for use by other devices. The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured. The CFG pin is used to select the operating mode of the SYNC pin as shown in Table 12. Figure 12 illustrates the typical connections for each mode.

Table 12. SYNC Pin Function Selection

CFG Pin	SYNC Pin Function
LOW	SYNC is configured as an input
OPEN	Auto Detect mode
HIGH	SYNC is configured as an output f_{SW} = 400 kHz (default)

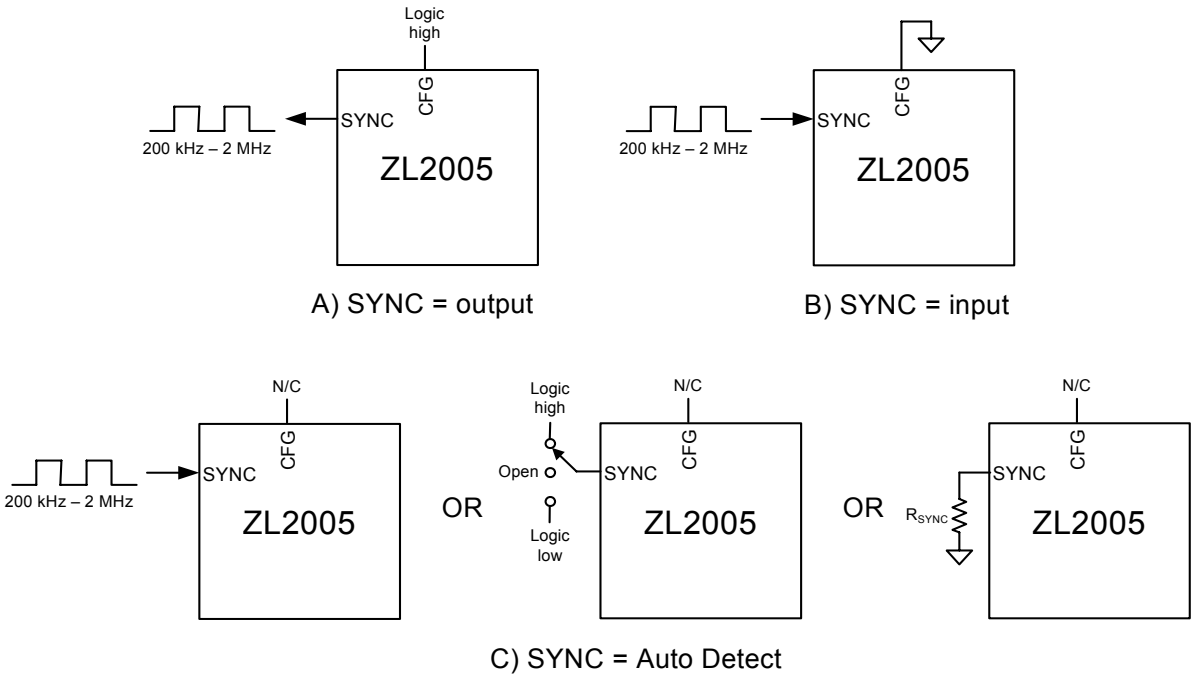


Figure 12. SYNC Pin Configurations

Configuration A: SYNC OUTPUT

When the SYNC pin is configured as an output (CFG pin is tied HIGH), the device will operate from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400 kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this configuration.

Configuration B: SYNC INPUT

When the SYNC pin is configured as an input (CFG pin is tied LOW), the device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL2005's oscillator will then synchronize with the rising edge of external clock.

The incoming clock signal must be in the range of 200 kHz to 2 MHz and must be stable when the enable pin is asserted. The clock signal must also exhibit the necessary performance requirements (see Table 3). In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot.

If this happens, the ZL2005 will turn off the power FETs (QH and QL in Figure 4) typically within 10 µS. Users are discouraged from removing an external SYNC clock while the ZL2005 is operating with Enable asserted.

Configuration C: SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode (CFG pin is left OPEN), the device will automatically check for a clock signal on the SYNC pin after enable is asserted.

If a clock signal is present, The ZL2005's oscillator will then synchronize the rising edge of the external clock. Refer to SYNC INPUT description.

If no incoming clock signal is present, the ZL2005 will configure the switching frequency according to the state of the SYNC pin as listed in Table 13. In this mode, the ZL2005 will only read the SYNC pin connection during the start-up sequence. Changes to SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on.

Table 13. Switching Frequency Selection

SYNC Pin Setting	Frequency
LOW	200 kHz
OPEN	400 kHz
HIGH	1 MHz
Resistor	See Table 14

If the user wishes to run the ZL2005 at a frequency other than those listed in Table 13, the switching frequency can be set using an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 14.

Table 14. R_{SYNC} Resistor Values

f_{SW}	R_{SYNC}	f_{SW}	R_{SYNC}
200 kHz	10 kΩ	571 kHz	28.7 kΩ
222 kHz	11 kΩ	615 kHz	31.6 kΩ
242 kHz	12.1 kΩ	667 kHz	34.8 kΩ
267 kHz	13.3 kΩ	727 kHz	38.3 kΩ
296 kHz	14.7 kΩ	889 kHz	46.4 kΩ
320 kHz	16.2 kΩ	1000 kHz	51.1 kΩ
364 kHz	17.8 kΩ	1143 kHz	56.2 kΩ
400 kHz	19.6 kΩ	1333 kHz	68.1 kΩ
421 kHz	21.5 kΩ	1600 kHz	82.5 kΩ
471 kHz	23.7 kΩ	2000 kHz	100 kΩ
533 kHz	26.1 kΩ		

The switching frequency can also be set to any value between 200 kHz and 2 MHz using the I^2C/SMBus interface. The available frequencies are bounded by the relation f_{sw} = 8 MHz/N, (with 4<= N <= 40). See Application Note AN13 for details on configuring the switching frequency using the I^2C/SMBus interface.

If multiple ZL2005s are used together, connecting the SYNC pins together will force all devices to synchronize to one another. The CFG pin of one device must have its SYNC pin set as an output and the remaining devices must have their SYNC pins set as an input or all devices must be driven by the same external clock source.

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected value in Table 14. The difference is due to hardware quantization.

5.8 Selecting Power Train Components

The ZL2005 is a synchronous buck controller that uses external MOSFETs, inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance. Zilker Labs offers an online circuit design and simulation tool, PowerPilot, to assist designers in this task.

Please visit http://www.zilkerlabs.com to access PowerPilot. For more detailed guidelines regarding component selection, please refer to Application Note AN11.

To select the appropriate power stage components for a set of desired performance goals, the power supply requirements listed in Table 15 must be known.

Table 15. Power Supply Requirements Example

Parameter	Range	Example Value
Input voltage (V_{IN})	3.0 – 14.0 V	12 V
Output voltage (V_{OUT})	0.6 – 5.0 V	1.2 V
Output current (I_{OUT})	0 to ~25 A	20 A
Output voltage ripple (V_{orip})	< 3% of V_{OUT}	1% of V_{OUT}
Output load step (I_{ostep})	< Io	50% of I_o
Output load step rate	—	10 A/µS
Allowable output deviation due to load step	—	± 50 mV
Maximum PCB temp.	120°C	85°C
Desired efficiency	—	85%
Other considerations	Various	Optimize for small size

Design Trade-offs

The design of a switching regulator power stage requires the user to consider trade-offs between cost, size and performance. For example, size can be optimized at the expense of efficiency. Additionally, cost can be optimized at the expense of size. For a detailed description of circuit trade-offs, refer to Application Note AN11.

To start a design, select a switching frequency (f_{SW}) based on Table 16. This frequency is a starting point and may be adjusted as the design progresses.

Table 16. Circuit Design Considerations

Frequency Range	Efficiency	Circuit Size
200 – 400 kHz	Highest	Larger
400 – 800 kHz	Moderate	Smaller
800 kHz – 2 MHz	Lower	Smallest

Inductor Selection

The output inductor selection process will include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce the output capacitance requirement and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be

struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple current (I_{opp}) equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep} \quad (3)$$

Now the output inductance can be calculated using the following equation:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{f_{sw} \times I_{opp}} \quad (4)$$

where V_{INM} is the maximum input voltage.

The average inductor current is equal to the maximum output current. The peak inductor current (IL_{pk}) is calculated using the following equation where I_{OUT} is the maximum output current:

$$IL_{pk} = I_{OUT} + \frac{I_{opp}}{2} \quad (5)$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed above.

In over-current or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that is not saturated at these conditions to protect the load and the power supply MOSFETs from damaging currents.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}^{2} \quad (6)$$

I_{Lrms} is given by:

$$I_{Lrms} = \sqrt{I_{OUT}^{2} + \frac{I_{opp}^{2}}{12}} \quad (7)$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor's datasheet. Add the core loss and the DCR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

Output Capacitor Selection

Several trade-offs also must be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up to the new steady state output current value.

As a starting point, allocate one-half of the output voltage ripple to the capacitor ESR and the other half to its capacitance, as shown in the following equations:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}} \quad (8)$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}} \quad (9)$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using the following equation:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}} \quad (10)$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

For more information on the performance of the power supply in response to a transient load, refer to Application Note AN11.

Input Capacitor

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5 or 12 V "bulk" supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This input ripple (I_{CINrms}) can be determined from the following equation:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1-D)} \qquad (11)$$

Please refer to Application Note AN11 for detailed derivation including efficiency and ripple current.

Without capacitive filtering near the power supply input circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated above to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

Bootstrap Circuit Component Selection

The high-side driver boost circuit utilizes an external Schottky diode (DB) and an external bootstrap capacitor (CB) to supply sufficient gate drive for the high-side MOSFET driver. DB should be a 20 mA, 30 V Schottky diode or equivalent device and CB should be a 1 µF ceramic type rated for at least 6.3V.

QL Selection

The bottom MOSFET should be selected primarily based on the device's $R_{DS(ON)}$ and secondarily based on its gate charge. To choose QL, use the following equation and allow 2–5% of the output power to be dissipated in the $R_{DS(ON)}$ of QL (lower output voltages and higher step-down ratios will be closer to 5%):

$$P_{QL} = 0.05 \times V_{OUT} \times I_{OUT} \qquad (12)$$

Calculate the RMS current in QL as follows:

$$I_{botrms} = I_{Lrms} \times \sqrt{1-D} \qquad (13)$$

Calculate the desired maximum $R_{DS(ON)}$ as follows:

$$R_{DS(ON)} = P_{QL}/I_{botrms}^2 \qquad (14)$$

Note that the $R_{DS(ON)}$ given in the manufacturer's datasheet is measured at 25°C. The actual $R_{DS(ON)}$ in the end-use application will be much higher. For example, a Vishay Si7114 MOSFET with a junction temperature of 125°C has an $R_{DS(ON)}$ 1.4 times higher than the value at 25°C.

Select a candidate MOSFET, and calculate the required gate drive current as follows:

$$I_g = f_{sw} \times Q_g \qquad (15)$$

Keep in mind that the total allowed gate drive current for both QH and QL is 80 mA.

MOSFETs with lower $R_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off. Since the MOSFET gate drive circuits are integrated in the ZL2005, this power is dissipated in the ZL2005 according to the following equation:

$$P_{QL} = f_{sw} \times Q_g \times V_{INM} \qquad (16)$$

QH Selection

In addition to the $R_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. The procedure to select QH is similar to the procedure for QL. First, assign 2–5% of the output power to be dissipated in the $R_{DS(ON)}$ of QH using the equation for QL above. As was done with QL, calculate the RMS current as follows:

$$I_{toprms} = I_{Lrms} \times \sqrt{D} \qquad (17)$$

Calculate a starting $R_{DS(ON)}$ as follows, in this example using 5%:

$$P_{QH} = 0.05 \times V_{OUT} \times I_{OUT} \qquad (18)$$

$$R_{DS(ON)} = P_{QH} / I_{toprms}^2 \qquad (19)$$

Select a MOSFET and calculate the resulting gate drive current. Verify that the combined gate drive current from QL and QH does not exceed 80 mA.

Next, calculate the switching time using

$$t_{sw} = \frac{Q_g}{I_{gdr}} \quad (20)$$

where Q_g is the gate charge of the selected QH and I_{gdr} is the peak gate drive current available from the ZL2005.

Although the ZL2005 has a typical gate drive current of 3 A, use the minimum guaranteed current of 2 A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw} \quad (21)$$

The total power dissipated by QH is given by the following equation:

$$P_{QHtot} = P_{QH} + P_{swtop} \quad (22)$$

MOSFET Thermal Check

Once the power dissipations for QH and QL have been calculated, the MOSFETs junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature as follows:

$$T_{j\,max} = T_{pcb} + P_Q \times R_{th} \quad (23)$$

For further details of thermal analysis and design see Application Note AN10.

Current Sensing Components

Once the current sense method has been selected (Refer to Section 5.9, "Current Limit Threshold Selection,"), the procedure to select the component is the following:

When using the inductor DCR sensing method, the user must also select an R/C network comprised of R1 and CL (see Figure 13).

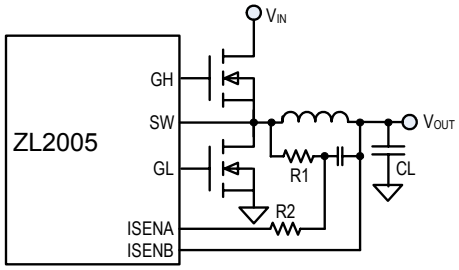


Figure 13. DCR Current Sensing

These components should be selected according to the following equation:

$$\tau_{RC} = L / DCR \quad (24)$$

R1 should be in the range of 500 Ω to 5 kΩ in order to minimize the power dissipation through it. The user should make sure the resistor package size is appropriate for the power dissipated. Once R1 has been calculated, the value of R2 should be selected based on the following equation:

$$R2 = 5 \times R1 \quad (25)$$

If $R_{DS(ON)}$ is being used the external low side MOSFET will act as the sensing element as indicated in Figure 14.

5.9 Current Limit Threshold Selection

It is recommended that the user include a current limiting mechanism in their design to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current flowing through the circuit during a portion of the duty cycle.

Output current sensing can be accomplished by measuring the voltage across a series resistive sensing element according to equation 26.

$$V_{LIM} = I_{LIM} \times R_{SENSE} \quad (26)$$

Where:

I_{LIM} is the desired maximum current that should flow in the circuit

R_{SENSE} is the resistance of the sensing element

V_{LIM} is the voltage across the sensing element at the point the circuit should start limiting the output current.

The ZL2005 supports “lossless” current sensing, by measuring the voltage across a resistive element that is already present in the circuit. This eliminates additional efficiency losses incurred by devices that must use an additional series resistance in the circuit.

To set the current limit threshold, the user must first select a current sensing method. The ZL2005 incorporates two methods for current sensing, synchronous MOSFET $R_{DS(ON)}$ sensing and inductor DC resistance (DCR) sensing; Figure 14 shows a simplified schematic for each method.

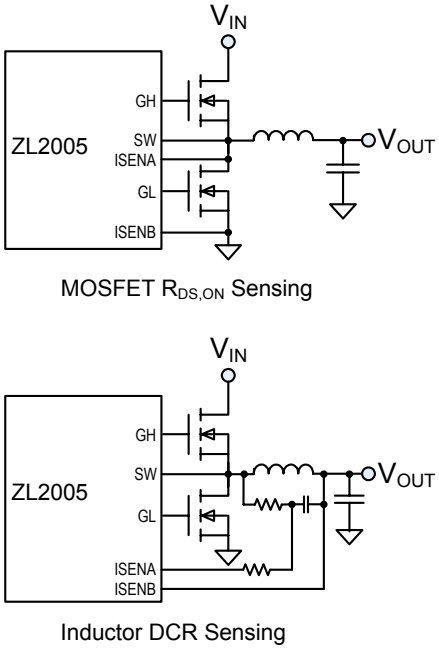


Figure 14. Current Sensing Methods

The current sensing method can be selected using the ILIM1 pin using Table 17. The ILIM0 pin must have a finite resistor connected to ground in order for Table 17 to be valid. If no resistor is connected between ILIM0 and ground, the default method is MOSFET $R_{DS(ON)}$ sensing. The current sensing method can be modified via the I^2C/SMBus interface. Please refer to Application Note AN13 for details.

In addition to selecting the current sensing method, the ZL2005 gives the power supply designer several choices for the fault response during over or under current condition. The user can select the number of violations allowed before declaring fault, a blanking time and the action taken when a fault is detected.

The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a current load step (Less accurate due to potential ringing).It is a configurable parameter.

Table 17 includes default parameters for the number of violations and the blanking time using pin-strap.

Table 17. Current Sensing Method Selection

ILIM0 Pin [1]	ILIM1 Pin	Current Limiting Configuration	Number of Violations Allowed[2]	Comments
R_{ILIM0}	LOW	Ground-referenced ($R_{DS,ON}$) sensing Blanking time: 672 ns	4	Best for low duty cycle and low f_{SW}
R_{ILIM0}	OPEN	Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 352 ns	4	Best for low duty cycle and high f_{SW}
R_{ILIM0}	HIGH	Output-referenced, up-slope sensing (Inductor DCR sensing) Blanking time: 352 ns	4	Best for high duty cycle
	Resistor	Depends on resistor value used; see Table 18		

NOTES:

1. $10\ k\Omega < R_{ILIM0} < 100\ k\Omega$
2. The number of violations allowed prior to issuing a fault response.

Table 18. Resistor Configured Current Sensing Method Selection

R_{ILIM1}	Current Sensing Method	Number of Violations Allowed[1]
10 kΩ	Ground-referenced ($R_{DS,ON}$) sensing Best for low duty cycle and low f_{SW} Blanking time: 672 ns	1
11 kΩ		3
12.1 kΩ		5
13.3 kΩ		7
14.7 kΩ		9
16.2 kΩ		11
17.8 kΩ		13
19.6 kΩ		15
21.5 kΩ	Output-referenced, down-slope sensing (Inductor DCR sensing) Best for low duty cycle and high f_{SW} Blanking time: 352 ns	1
23.7 kΩ		3
26.1 kΩ		5
28.7 kΩ		7
31.6 kΩ		9
34.8 kΩ		11
38.3 kΩ		13
42.2 kΩ		15
46.4 kΩ	Output-referenced, up-slope sensing (Inductor DCR sensing) Best for high duty cycle Blanking time: 352 ns	1
51.1 kΩ		3
56.2 kΩ		5
61.9 kΩ		7
68.1 kΩ		9
75 kΩ		11
82.5 kΩ		13
90.9 kΩ		15

NOTES:

1. The number of violations allowed prior to issuing a fault response.

Once the sensing method has been selected, the user must select the voltage threshold (V_{LIM}) based on equation 26, the desired current limit threshold, and the resistance of the sensing element.

The current limit threshold can be selected by simply connecting the ILIM0 and ILIM1 pins as shown in Table 19. The ground-referenced sensing method is being used in this mode.

Table 19. Current Limit Threshold Voltage Settings

		ILIM0		
		LOW	**OPEN**	**HIGH**
ILIM1	**LOW**	20 mV	30 mV	40 mV
	OPEN	50 mV	60 mV	70 mV
	HIGH	80 mV	90 mV	100 mV

The threshold voltage can also be selected in 5 mV increments by connecting a resistor, R_{LIM0}, between the ILIM0 pin and ground according to Table 20. This method is preferred if the user does not desire to use or does not have access to the I^2C/SMBus interface and the desired threshold value is contained in Table 20.

Table 20. Current Limit Threshold Voltage Settings

V_{LIM}	R_{LIM0}	V_{LIM}	R_{LIM0}
0 mV	10 kΩ	55 mV	28.7 kΩ
5 mV	11 kΩ	60 mV	31.6 kΩ
10 mV	12.1 kΩ	65 mV	34.8 kΩ
15 mV	13.3 kΩ	70 mV	38.3 kΩ
20 mV	14.7 kΩ	75 mV	42.2 kΩ
25 mV	16.2 kΩ	80 mV	46.4 kΩ
30 mV	17.8 kΩ	85 mV	51.1 kΩ
35 mV	19.6 kΩ	90 mV	56.2 kΩ
40 mV	21.5 kΩ	95 mV	61.9 kΩ
45 mV	23.7 kΩ	100 mV	68.1 kΩ
50 mV	26.1 kΩ		

The current limit threshold can be set via the I^2C/SMBus interface. Please refer to Application Note AN13 for further details on setting current limit parameters.

5.10 Loop Compensation

The ZL2005 operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. Although the ZL2005 uses a digital control loop, it operates much like a traditional analog PWM controller. See Figure 15 for a simplified block diagram of the ZL2005 control loop, which differs from an analog control loop by the constants in the PWM and compensation blocks. As in the analog controller case, the compensation block compares the output voltage to the desired voltage reference and compensation zeros are added to keep the loop stable. The resulting integrated error signal is used to drive the PWM logic, converting the error signal into a duty cycle value to drive the external MOSFETs.

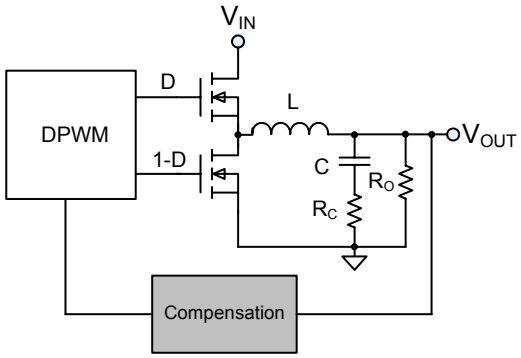


Figure 15. Control Loop Block Diagram

In the ZL2005, the compensation zeros are set by configuring the FC0 and FC1 pins or via the I^2C/SMBus interface once the user has calculated the required settings. This method eliminates the inaccuracies due to the component tolerances associated with using external resistors and capacitors. Most applications can be served by using the pin-strap compensation settings listed in Table 21. These settings will yield a conservative crossover frequency at a fixed fraction of the switching frequency (f_{SW}/20) and 60° of phase margin.

Table 21. Pin-Strap Setting for Loop Compensation

FC0 Range	FC0 Pin	FC1 Range	FC1 Pin
$f_{sw}/60 < f_n < f_{sw}/30$	HIGH	$f_{zesr} > f_{sw}/10$	HIGH
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	OPEN
		TBD	LOW
$f_{sw}/120 < f_n < f_{sw}/60$	OPEN	$f_{zesr} > f_{sw}/10$	HIGH
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	OPEN
		TBD	LOW
$f_{sw}/240 < f_n < f_{sw}/120$	LOW	$f_{zesr} > f_{sw}/10$	HIGH
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	OPEN
		TBD	LOW

Step 1: Using the following equation, calculate the resonant frequency of the LC filter, f_n.

$$f_n = \frac{1}{2\pi\sqrt{L \times C}} \quad (27)$$

Step 2: Based on Table 21, determine the FC0 setting.

Step 3: Calculate the ESR zero frequency (f_{ZESR}).

$$f_{zesr} = \frac{1}{2\pi CRc} \quad (28)$$

Step 4: Based on Table 21, determine the FC1 setting.

The parameters of the feedback compensation can also be set using the I^2C/SMBus interface. Refer to Application Note AN13 for details.

Refer to Application Note AN16 for details on setting FC0 and FC1.

The Zilker Labs web site (www.zilkerlabs.com) provides an on-line tool (PowerPilot) which computes compensation coefficients, and provides a parameter-driven design tool, schematic and BOM generation, and circuit simulation including control loop simulation.

5.11 Non-Linear Response Settings

The ZL2005 incorporates a non-linear response (NLR) loop that decreases the response time and the output voltage deviation in the event of a sudden output load current step. The NLR loop incorporates a secondary error signal processing path that bypasses the primary error loop when the output begins to transition outside of the standard regulation limits. This scheme results in a higher equivalent loop bandwidth than is possible using a traditional linear loop.

When a load current step function imposed on the output causes the output voltage to drop below the lower regulation limit, the NLR circuitry will force a positive correction signal that will turn on the upper MOSFET and quickly force the output to increase. Conversely, a negative load step (i.e., removing a large load current) will cause the NLR circuitry to force a negative correction signal that will turn on the lower MOSFET and quickly force the output to decrease.

The ZL2005 has been pre-configured with appropriate NLR settings that correspond to the loop compensation settings in Table 21.

5.12 Efficiency Optimized Driver Dead-time Control

The ZL2005 utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the top and bottom FETs. In a synchronous buck converter, the MOSFET drive circuitry must be designed such that the top and bottom MOSFETs are never in the conducting state at the same time. (Potentially damaging currents flow in the circuit if both top and bottom MOSFETs are simultaneously on for periods of time exceeding a few nanoseconds.) Conversely, long periods of time in which both MOSFETs are off reduce overall circuit efficiency by allowing current to flow in their parasitic body diodes.

It is therefore advantageous to minimize this deadtime to provide optimum circuit efficiency. In the first order model of a buck converter, the duty cycle is determined by the equation:

$$D = V_{OUT}/V_{IN} \quad (29)$$

However, non-idealities exist that cause the real duty cycle to extend beyond the ideal. Deadtime is one of those non-idealities that can be manipulated to improve efficiency. The ZL2005 has an internal algorithm that constantly adjusts deadtime non-overlap to minimize duty cycle, thus maximizing efficiency. This circuit will null out deadtime differences due to component variation, temperature and loading effects.

This algorithm is independent of application circuit parameters such as MOSFET type, gate driver delays, rise and fall times and circuit layout. In addition, it does not require drive or MOSFET voltage or current waveform measurements.

6 Power Management Functional Description

6.1 Input Undervoltage Lockout (UVLO)

The input undervoltage lockout (UVLO) prevents the ZL2005 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 2.85 V and 16 V using the UVLO pin. The simplest implementation is to connect the UVLO pin as shown in Table 22. If the UVLO pin is left unconnected, the UVLO threshold will default to 4.5 V.

Table 22. UVLO Threshold Settings

Pin Setting	UVLO Threshold
LOW	3 V
OPEN	4.5 V
HIGH	10.8 V

If the desired UVLO threshold is not one of the listed choices, the user can configure a threshold between 2.85 V and 16 V by connecting a resistor between the UVLO pin and GND by selecting the appropriate resistor from Table 23.

Table 23. UVLO Resistor Values

UVLO	R_{UVLO}
2.85 V	17.8 kΩ
3.14 V	19.6 kΩ
3.44 V	21.5 kΩ
3.79 V	23.7 kΩ
4.18 V	26.1 kΩ
4.59 V	28.7 kΩ
5.06 V	31.6 kΩ
5.57 V	34.8 kΩ
6.13 V	38.3 kΩ
6.75 V	42.2 kΩ

UVLO	R_{UVLO}
7.42 V	46.4 kΩ
8.18 V	51.1 kΩ
8.99 V	56.2 kΩ
9.9 V	61.9 kΩ
10.9 V	68.1 kΩ
12 V	75 kΩ
13.2 V	82.5 kΩ
14.54 V	90.9 kΩ
16 V	100 kΩ

V_{UVLO} can also be set to any value between 2.85 V and 16 V via I^2C/SMBus.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay time, followed by shutdown if the fault still persists at the end of the delay period. The device will remain in shutdown until permitted to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL2005 will be re-enabled.

Please refer to Application Note AN13 for details on how to configure the UVLO threshold or to select specific UVLO fault response options via the I^2C/SMBus interface.

6.2 Output Overvoltage Protection

The ZL2005 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. This feature is especially useful in protecting expensive processors, FPGAs, and ASICs from excessive voltages.

A hardware comparator is used to compare the actual output voltage (seen at the VSEN pin) to a threshold set to 15 % higher than the target output voltage by default. If the voltage at the VSEN pin exceeds this upper threshold level, the PG pin will de-assert. The device can then respond in a number of ways as follows:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart.

The default response from an overvoltage fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL2005 will be re-enabled.

Please refer to Application Note AN13 for details on how to select specific overvoltage fault response options via the I^2C/SMBus interface.

6.3 Output Pre-Bias Protection

An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a pre-bias condition exists at the output. The ZL2005 provides pre-bias protection by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the ramp rate set by the SS (0,1) pins. The actual time the output will take to ramp from the pre-bias voltage to the target voltage will vary depending on the pre-bias voltage but the total time elapsed from when the delay period expires and when the output reaches its target value will match the pre-configured ramp time. See Figure 16.

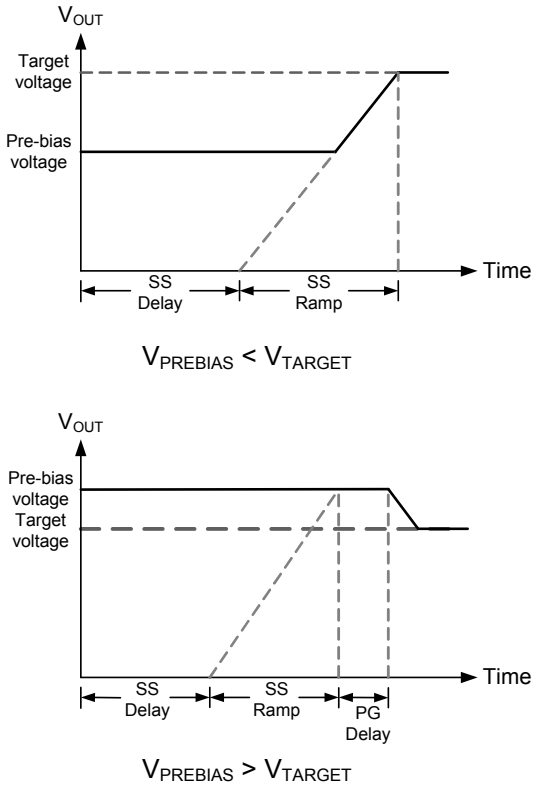


Figure 16. Output Response to Pre-Bias Voltages

If the pre-bias voltage is higher than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled with a PWM duty cycle that would ideally create the pre-bias voltage. Once the pre-configured soft-start ramp period has expired, the Power Good pin will be asserted (assuming the pre-bias voltage is not higher than the overvoltage limit). The PWM will then adjust its duty cycle to match the original target voltage and the output will ramp down to the pre-configured output voltage.

If a pre-bias voltage higher than the overvoltage limit, the device will not initiate a turn-on sequence and will declare an overvoltage fault condition to exist. In this case, the device will respond based on the output overvoltage fault response method that has been selected. See Section 6.2, "Output Overvoltage Protection," for response options due to an overvoltage condition.

6.4 Output Overcurrent Protection

The ZL2005 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Once the current limit threshold has been selected (see Section 5.9, "Current Limit Threshold Selection,"), the user may determine the desired course of action to be taken when an overload condition exists.

The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay time.
2. Initiate a shutdown and attempt to restart the power supply a preset number of times with a preset delay between attempts.
3. Continue operating throughout a specific delay time, followed by shutdown.
4. Continue operating throughout the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL2005 will be re-enabled.

Please refer to Application Note AN15 for details on how to select specific overcurrent fault response options via the I^2C/SMBus interface.

6.5 Thermal Protection

The ZL2005 includes an on-chip thermal sensor that continuously measures the internal temperature of the die and will shut down the device when the temperature exceeds the preset limit. The default temperature limit is set to 125°C in the factory, but the user may set the limit to a different value if desired. See Application Note AN13 for details. Note that setting a higher thermal limit via the I^2C/SMBus interface may result in permanent damage to the device. Once the device has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay time.
2. Initiate a shutdown and attempt to restart the power supply a preset number of times with a preset delay between attempts.
3. Continue operating throughout a specific delay time, followed by shutdown.
4. Continue operating throughout the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the device to restart, the device will wait the preset delay period (if configured to do so) and will then check the temperature. If the temperature has dropped below a value that is approximately 15°C lower than the selected temperature limit (the over-temperature warning threshold), the device will attempt to re-start. If the temperature is still above the over-temperature warning threshold, the device will wait the preset delay period and retry again.

The default response from a temperature fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL2005 will be re-enabled.

Please refer to Application Note AN13 for details on how to select specific temperature fault response options via the I^2C/SMBus interface.

6.6 Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O operates at a higher voltage than the Core and therefore the Core supply voltage, must not exceed the I/O supply voltage by some amount (typically 300 mV).

Voltage tracking protects these sensitive ICs by limiting the differential voltage between multiple power supplies during the power-up and power down sequence. The ZL2005 integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device's output regulation.

The ZL2005 offers two modes of tracking:

1. Coincident. This mode configures the ZL2005 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.
2. Ratiometric. This mode configures the ZL2005 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor string may be used to configure a different tracking ratio.

Figure 17 illustrates the typical connection and the two tracking modes.

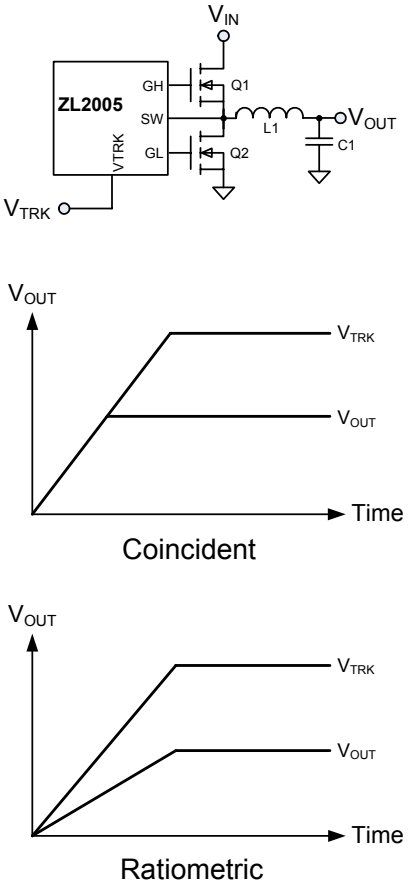


Figure 17. Tracking Modes

The master ZL2005 device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. A delay of at least 10 ms must be configured into the master device using the DLY0/1 pins, and the user may also configure a specific ramp rate using the SS0/1 pins. Any device that is configured for tracking mode will ignore its soft-start delay and ramp time settings (SS0/1 and DLY0/1 pins) and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin. The tracking mode for all other devices can be set by connecting a resistor from the SS1 pin to ground according to Table 24. All of the ENABLE pins in the tracking group must be connected together and driven by a single logic source.

Table 24. Tracking Mode Configuration

R_{SS1}	Tracking Ratio	Upper Track Limit	Ramp-up/Ramp-down Behavior
No resistor	Tracking mode is disabled		
10 kΩ	100%	Limited by target voltage and 110% of V(0,1) pin-strap setting	Output not allowed to decrease before PG
11 kΩ			Output will always follow VTRK
12.1 kΩ		Limited by VTRK pin voltage 110% of V(0,1) pin-strap setting	Output not allowed to decrease before PG
13.3 kΩ			Output will always follow VTRK
14.7 kΩ	50%	Limited by target voltage and 110% of V(0,1) pin-strap setting	Output not allowed to decrease before PG
16.2 kΩ			Output will always follow VTRK
17.8 kΩ		Limited by VTRK pin voltage 110% of V(0,1) pin-strap setting	Output not allowed to decrease before PG
19.6 kΩ			Output will always follow VTRK

6.7 Voltage Margining

The ZL2005 offers a simple means to vary its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. The MGN pin is a TTL-compatible input that is continuously monitored and can be driven directly by a processor I/O pin or other logic-level output.

The ZL2005's output will be forced higher than its nominal setpoint when the MGN pin is driven HIGH, and the output will be forced lower than its nominal setpoint when the MGN pin is driven LOW. When the MGN pin is left floating (high impedance), the ZL2005's output voltage will be set to its nominal voltage setpoint determined by the V0 and V1 pins and/or the I^2C/SMBus settings that configure the nominal output voltage. Default margin limits of V_{NOM} ±5% are pre-loaded in the factory, but the margin limits can be modified through the I^2C/SMBus interface to as high as V_{NOM} + 10% or as low as 0V, where V_{NOM} is the nominal output voltage setpoint determined by the V0 and V1 pins.

The margin limits and the MGN command can both be set individually through the I^2C/SMBus interface. Additionally, the transition rate between the nominal output voltage and either margin limit can be configured through the I^2C/SMBus interface. Please refer to Application Note AN13 for detailed instructions on modifying the margining configurations.

6.8 I^2C/SMBus Communications

The ZL2005 provides an I^2C/SMBus digital interface that enables the user to configure all aspects of the device operation as well as monitor the input and output parameters. The ZL2005 can be used with any standard 2-wire I^2C host device. In addition, the device is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. The ZL2005 accepts most standard PMBus commands.

6.9 I^2C/SMBus Device Address Selection

When communicating with multiple ZL2005s using the I^2C/SMBus serial interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 25 to provide up to eight unique device addresses. Address values are right-justified.

Table 25. Serial Bus Device Address Selection

		SA1		
		LOW	OPEN	HIGH
SA0	LOW	0x20	0x23	0x26
	OPEN	0x21	0x24	0x27
	HIGH	0x22	0x25	Reserved

If additional device addresses are required, a resistor can be connected to the SA0 pin according to Table 26 to provide up to 25 unique device addresses. In this case the SA1 pin should be tied to SGND.

Table 26. SMBus Address Values

SMBus Address	R_{SA0}	SMBus Address	R_{SA0}
0x00	10 kΩ	0x0D	34.8 kΩ
0x01	11 kΩ	0x0E	38.3kΩ
0x02	12.1 kΩ	0x0F	42.2 kΩ
0x03	13.3 kΩ	0x10	46.4 kΩ
0x04	14.7 kΩ	0x11	51.1 kΩ
0x05	16.2 kΩ	0x12	56.2 kΩ
0x06	17.8 kΩ	0x13	61.9 kΩ
0x07	19.6 kΩ	0x14	68.1 kΩ
0x08	21.5 kΩ	0x15	75 kΩ
0x09	23.7 kΩ	0x16	82.5 kΩ
0x0A	26.1 kΩ	0x17	90.9 kΩ
0x0B	28.7 kΩ	0x18	100 kΩ
0x0C	31.6 kΩ		

If more than 25 unique device addresses are required or if other SMBus address values are desired, both the SA0 and SA1 pins can be configured with a resistor to SGND according to the equation (30) and Table 27.

$$\text{SMBus address} = 25 \times (\text{SA1 index}) + (\text{SA0 index}) \quad (30)$$

Using this method, the user can theoretically configure up to 625 unique SMBus addresses, however the SMBus is inherently limited to 128 devices so attempting to configure an address higher than 128 will cause the device address to repeat (i.e, attempting to configure a device address of 129 would result in a device address of 1). Therefore, the user should use index values 0-4 on the SA1 pin and the full range of index values on the SA0 pin, which will provide 125 device address combinations.

Table 27. SMBus Address Index Values

SA0 or SA1 Index	R_{SA}	SA0 or SA1 Index	R_{SA}
0	10 kΩ	13	34.8 kΩ
1	11 kΩ	14	38.3 kΩ
2	12.1 kΩ	15	42.2 kΩ
3	13.3 kΩ	16	46.4 kΩ
4	14.7 kΩ	17	51.1 kΩ
5	16.2 kΩ	18	56.2 kΩ
6	17.8 kΩ	19	61.9 kΩ
7	19.6 kΩ	20	68.1 kΩ
8	21.5 kΩ	21	75 kΩ
9	23.7 kΩ	22	82.5 kΩ
10	26.1 kΩ	23	90.9 kΩ
11	28.7 kΩ	24	100 kΩ
12	31.6 kΩ		

6.10 Phase Spreading

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

In order to enable phase spreading, all converters must be synchronized to the same switching clock. The CFG pin is used to set the configuration of the SYNC pin for each device as described in Section 5.7, “Switching Frequency and PLL,” .

Selecting the phase offset for the device is accomplished by selecting a device address according to the following equation:

Phase offset = device address x 45°

For example:

A device address of 0x00 or 0x20 would configure no phase offset

A device address of 0x01 or 0x21 would configure 45° of phase offset

A device address of 0x02 or 0x22 would configure 90° of phase offset.

The phase offset of each device may also be set to any value between 0° and 337.5° in 22.5° increments via the I^2C/SMBus interface. Please refer to Application Note AN13 for details.

6.11 Output Sequencing

A group of ZL2005 devices may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage. Multi-device sequencing can be achieved by configuring each device through the I^2C/SMBus interface or by using Zilker Labs’ patented autonomous sequencing mode.

Autonomous sequencing mode configures sequencing using status information broadcast by ZL2005 onto the I^2C/SMBus pins SCL and SDA. No I^2C or SMBus host device is involved in this method, but the SCL and SDA pins must be interconnected between all devices that the user wishes to sequence using this method. Note: Pull-up resistors on SCL and SDA are required and should be selected using the criteria in the SMBus 2.0 specification.

The sequence order is determined using each device’s I^2C/SMBus device address. Using autonomous sequencing mode (configured using the CFG pin), the devices must exhibit sequential device addresses with no missing addresses in the chain. This mode will also constrain each device to have a phase offset according to its device address as described in Section 6.10, “Phase Spreading” on this page.

The group will turn on in order starting with the device with the lowest address and will continue to turn on each device in the address chain until all devices connected have been turned on. When turning off, the device with the highest address will turn off first followed in reverse order by the other devices in the group.

Sequencing is configured by connecting a resistor from the CFG pin to ground as described in Table 28. The CFG pin is used to set the configuration of the SYNC pin as well as to determine the sequencing method and order. Please refer to Switching Frequency and PLL for more details on the operating parameters of the SYNC pin.

Table 28. CFG Pin Configurations for Sequencing

R_{CFG}	SYNC Pin Config	Sequencing Configuration
10 kΩ	Input	Sequencing is disabled
11 kΩ	Auto detect	
12.1 kΩ	Output	
14.7 kΩ	Input	The ZL2005 is configured as the first device in a nested sequencing group. Turn-on order is based on the device SMBus address.
16.2 kΩ	Auto detect	
17.8 kΩ	Output	
21.5 kΩ	Input	The ZL2005 is configured as a last device in a nested sequencing group. Turn-on order is based on the device SMBus address.
23.7 kΩ	Auto detect	
26.1 kΩ	Output	
31.6 kΩ	Input	The ZL2005 is configured as the middle device in a nested sequencing group. Turn-on order is based on the device SMBus address
34.8 kΩ	Auto detect	
38.3 kΩ	Output	

Multiple device sequencing may also be achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain. This method places less restrictions on device address (no need of sequential address) and also allows the user to assign any phase offset to any device irrespective of its device address.

Event based sequencing and fault spreading are broadcast in address groups of up to eight ZL2005 devices. An address group consists of all devices whose addresses differ in only the three least significant bits of the address. For example, addresses 20, 25 and 27 are all within the same group. Addresses 1F, 20 and 28 are all in different groups. Devices in the same address group can broadcast power on and power off sequencing and fault spreading events with each other. Devices in different groups cannot.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group.

Please refer to Application Note AN13 for details on sequencing via the I^2C/SMBus interface.

6.12 Monitoring via I^2C/SMBus

A system controller can monitor a wide variety of different ZL2005 system parameters through the I^2C/SMBus interface. The controller can monitor for fault conditions by monitoring the SALRT pin, which will be asserted when any number of pre-configured fault or warning conditions occur. The system controller can also continuously monitor for any number of power conversion parameters including but not limited to the following:

1. Input voltage
2. Output voltage
3. Output current
4. Internal junction temperature
5. Temperature of an external device
6. Switching frequency
7. Duty cycle

Please refer to Application Note AN13 for details on how to monitor specific parameters via the I^2C/SMBus interface.

6.13 Temperature Monitoring Using the XTEMP Pin

The ZL2005 supports measurement of an external device temperature using either a thermal diode integrated in a processor, FPGA or ASIC, or using a discrete diode-connected NPN transistor such as a 2N3904 or equivalent. Figure 18 illustrates the typical connections required.

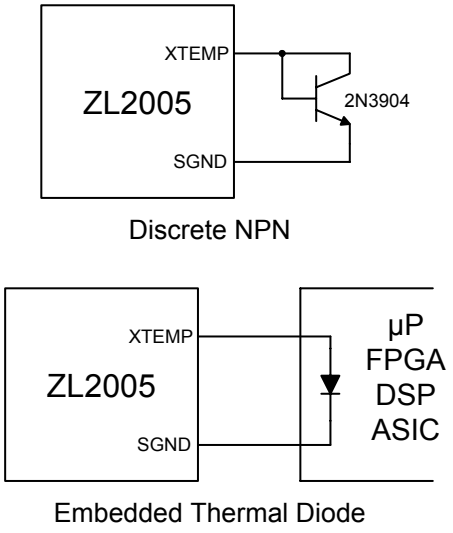


Figure 18. External Temperature Monitoring

6.14 Fan Monitoring using the TACH Pin

The ZL2005 can monitor the tachometer pulse of an external 3-wire fan connected to the TACH pin. The device will report a revolutions per minute (RPM) value assuming one pulse per revolution. The TACH pin is only monitored when the device is enabled or when it is configured to always be in monitoring mode. Refer to Application Note AN13 for more details on configuring specific operating modes.

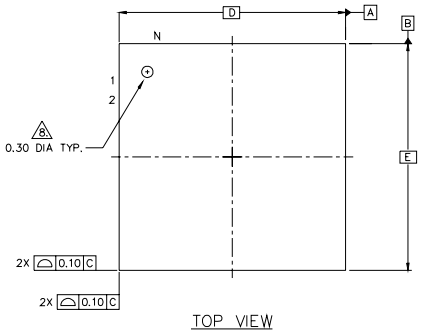
6.15 Device Security Features

Note that the ZL2005 integrates several security measures to ensure that the user can only restore the device to a level that has been made available to them. During the initialization process, the ZL2005 checks for stored values contained in its internal memory. The ZL2005 offers two internal memory storage units that are accessible by the user as follows:

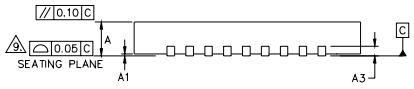
1. *Default Store:* A power supply module manufacturer may want to protect the module from damage by preventing the user from being able to modify certain values that are related to the physical construction of the module. In this case, the module manufacturer would use the Default Store and would allow the user to restore the device to its default setting but would restrict the user from restoring the device to the factory setting.
2. *User Store:* The manufacturer of a piece of equipment may want to provide the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the User Store to achieve this goal.

Please refer to Application Note AN13 for details on how to set specific security measures via the I^2C/SMBus interface.

7 Package Dimensions

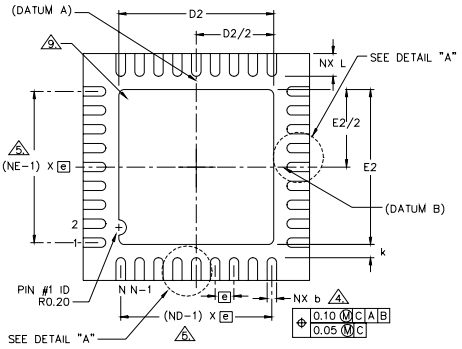


TOP VIEW

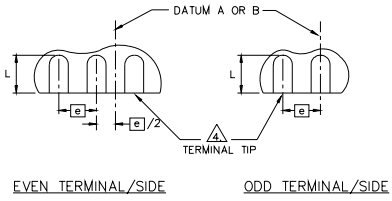


SIDE VIEW

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
e		0.50 BSC.		
N		36		3
ND		9		5
NE		9		5
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	4.00	4.10	4.20	
E2	4.00	4.10	4.20	
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
θ	0	——	12	2
K		0.20 MIN.		
D		6.00 BSC		
E		6.00 BSC		



BOTTOM VIEW

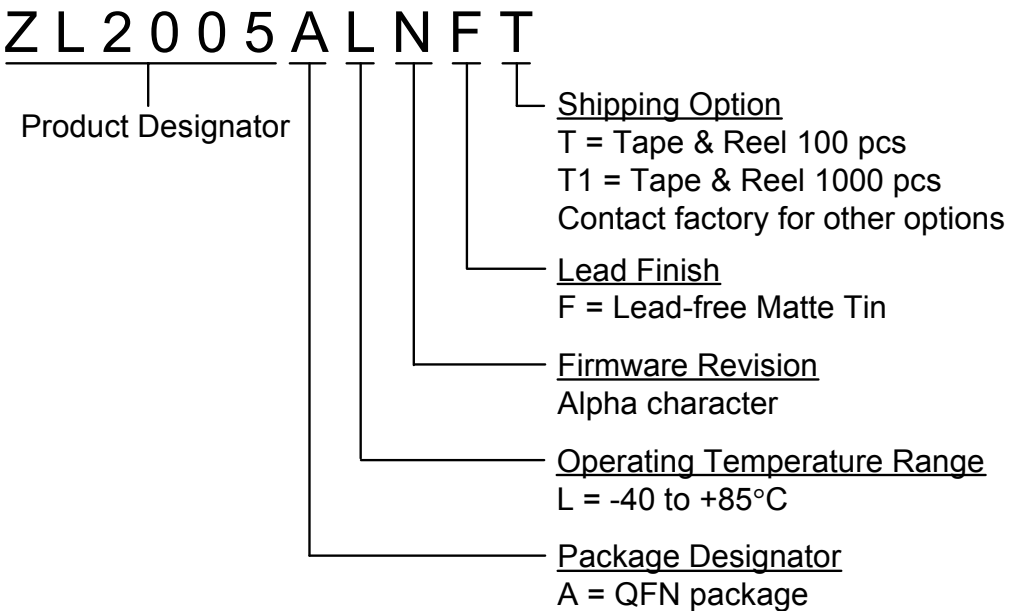


DETAIL "A"

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS (mm), ~~θ~~ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE, RESPECTIVELY.
6. MAXIMUM PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMS TO JEDEC REGISTERED OUTLINE MO-220.

8 Ordering Information



Related Documentation

The following application support documents and tools are available to help simplify your design.

Item	Description
ZL2005EVK1	Evaluation Kit: 12V to 3.3V, 20A DC/DC Converter with Power Management
AN10	Application Note: ZL2005 and ZL2105 Thermal and Layout Guidelines
AN11	Application Note: ZL2005 Component Selection Guide
AN13	Application Note: PMBus Command Set
AN15	Application Note: ZL2005 Current Protection and Measurement
AN16	Application Note: ZL2005 Digital Control Loop Compensation
AN21	Application Note: Protecting Configuration During Manufacturing
AN22	Application Note: Autonomous Sequencing Technology
AN23	Application Note: Voltage Tracking with the ZL2005

Revision History

Revision Number	Description	Date
1.0	Initial release	2/16/06
1.1	Table 3 update	4/25/06
1.2	Table 3, 28 update	9/07/06
FN6848.0	Assigned file number FN6848 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read "Intersil and it's subsidiaries including Zilker Labs, Inc." No changes to datasheet content	2/18/09
FN6848.0	Stamped datasheet “Not Recommended For New Designs Recommended Replacement Part ZL2006”. No file rev, no date change, no changes to datasheet content.	8/5/09
FN6848.1	Added following statement to disclaimer on page 40: “This product is subject to a license from Power One, Inc. related to digital power technology as set forth in U.S. Patent No. 7,000,125 and other related patents owned by Power One, Inc. These license rights do not extend to stand-alone POL regulators unless a royalty is paid to Power One, Inc.”	12/8/10
FN6848.2	In Table 3, under “UVLO setpoint accuracy,” changed min/max limits from -100 / 100 to -150 / 150 mV. In Table 3, added Note 5: "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." and referenced it in the headings of the Min and Max columns.	1/20/2011



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