

P-Channel 1.5-V (G-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 20	0.041 at $V_{GS} = - 4.5$ V	- 10.0	22 nC
	0.048 at $V_{GS} = - 2.5$ V	- 9.32	
	0.058 at $V_{GS} = - 1.8$ V	- 8.48	
	0.075 at $V_{GS} = - 1.5$ V	- 7.45	

FEATURES

- TrenchFET® Power MOSFET
- Ultra Small MICRO FOOT® ChipScale Packaging Reduces Footprint Area, Profile (0.62 mm) and On-Resistance Per Footprint Area



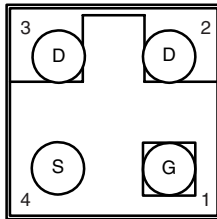
RoHS
COMPLIANT

APPLICATIONS

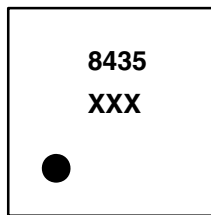
- Low Threshold Load Switch for Portable Devices
- Low Power Consumption
- Increased Battery Life

MICRO FOOT

Bump Side View



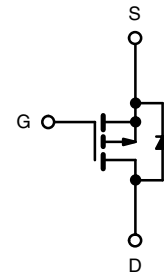
Backside View



Device Marking: 8435

xxx = Date/Lot Traceability Code

Ordering Information: Si8435DB-T1-E1 (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 5	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	- 15	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	W
Maximum Power Dissipation	P_D	$T_C = 25$ °C	
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Package Reflow Conditions ^d	IR/Convection	260	

Notes:

a. Based on $T_C = 25$ °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. Refer to IPC/JEDEC (J-STD-020C), no manual or hand soldering.

e. In this document, any reference to the Case represents the body of the MICRO FOOT device and Foot is the bump.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a,b}	R_{thJA}	35	45	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	16	20	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 72 °C/W.

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 15.5		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 0.35		- 1.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ °C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	- 15			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$		0.034	0.041	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		0.040	0.048	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.048	0.058	
		$V_{GS} = -1.5\text{ V}, I_D = -1\text{ A}$		0.055	0.075	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -1\text{ A}$		10.5	16	S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1600		pF
Output Capacitance	C_{oss}			265		
Reverse Transfer Capacitance	C_{rss}			175		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -5\text{ V}, I_D = -1\text{ A}$		23	35	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = -16\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$		22	33	
Gate-Drain Charge	Q_{gd}			3.25		
				1.95		
Gate Resistance	R_g	$V_{GS} = -0.1\text{ V}, f = 1\text{ MHz}$		20		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \equiv -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		15	23	ns
Rise Time	t_r			29	44	
Turn-Off Delay Time	$t_{d(off)}$			230	345	
Fall Time	t_f			91	137	

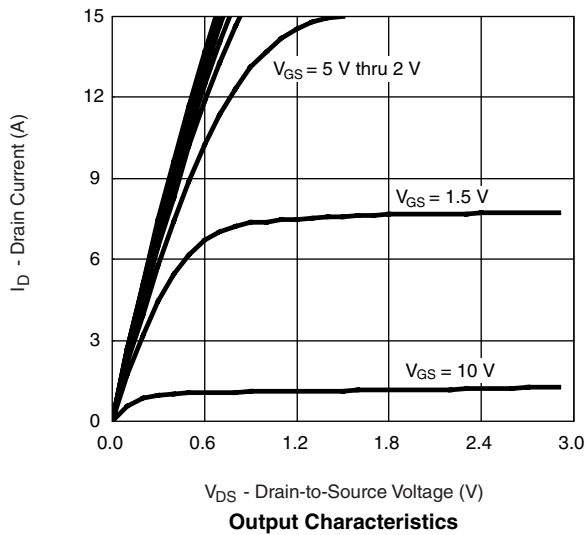
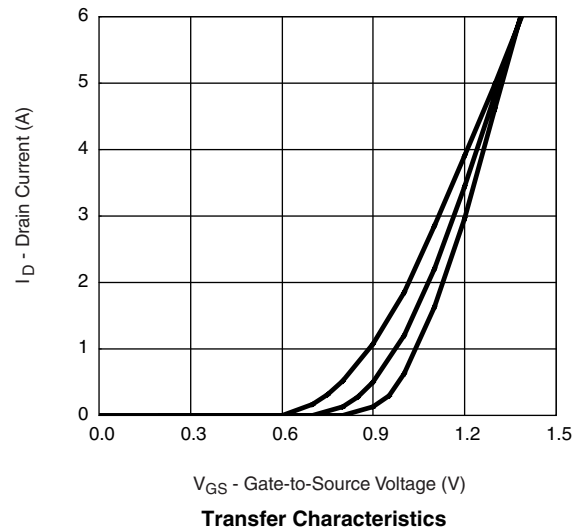
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			- 5.21	A
Pulse Diode Forward Current	I_{SM}				- 15	
Body Diode Voltage	V_{SD}	$I_S = -1\text{ A}$, $V_{GS} = 0\text{ V}$		0.6	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -1\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		116	174	ns
Body Diode Reverse Recovery Charge	Q_{rr}			203	305	nC
Reverse Recovery Fall Time	t_a			45		ns
Reverse Recovery Rise Time	t_b			71		

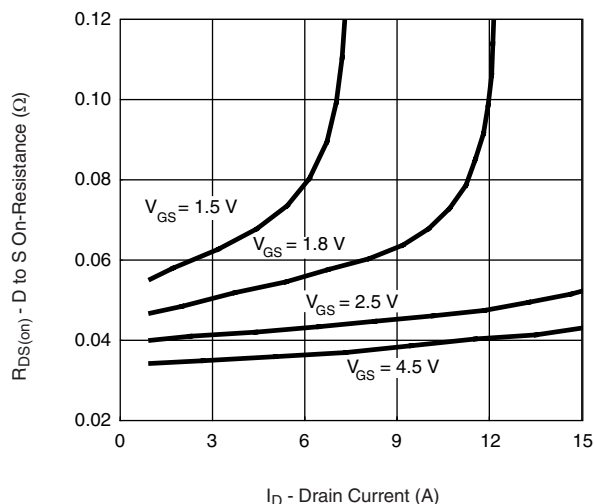
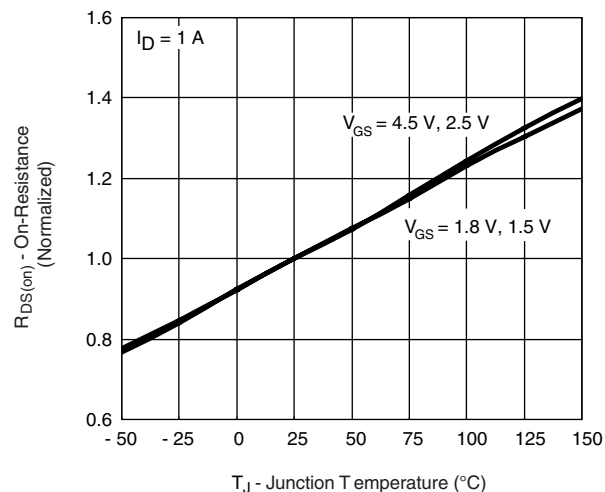
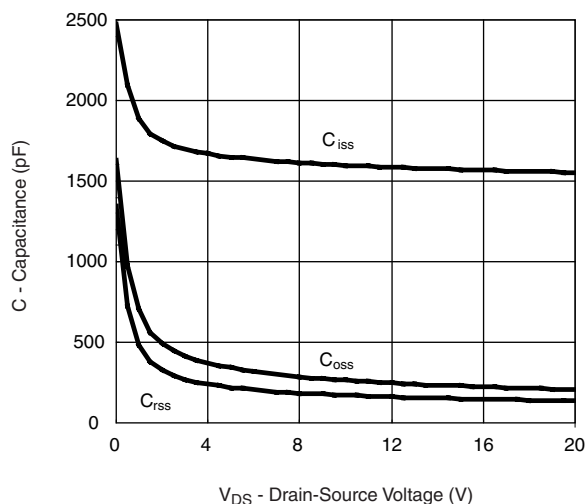
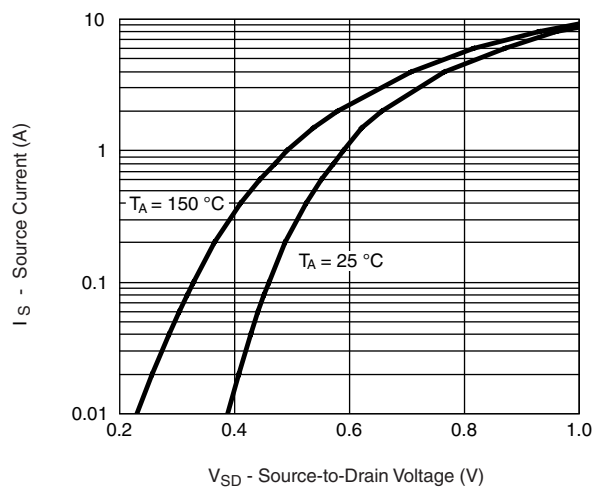
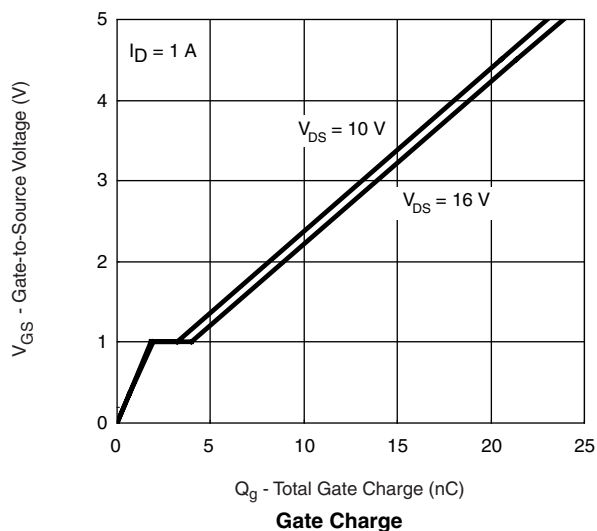
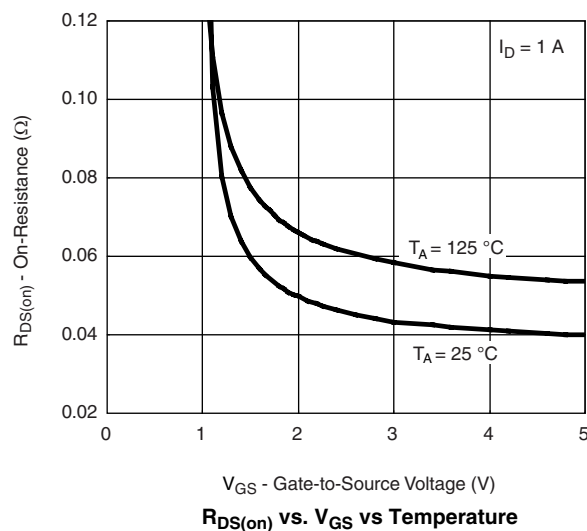
Notes:

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

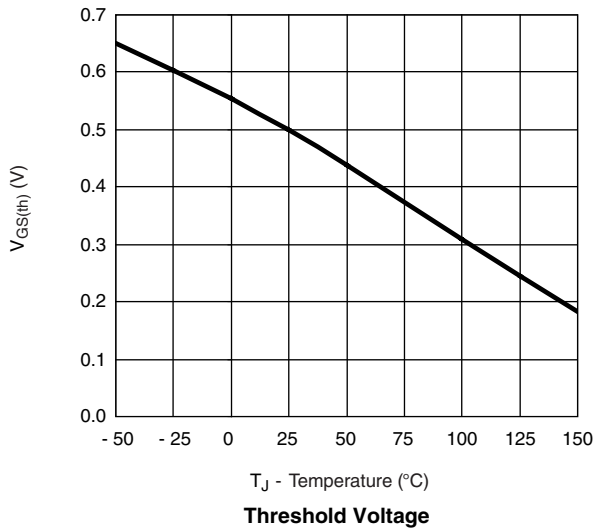
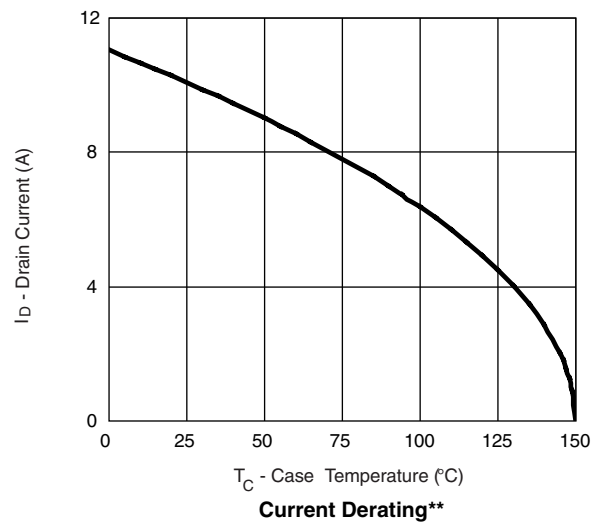
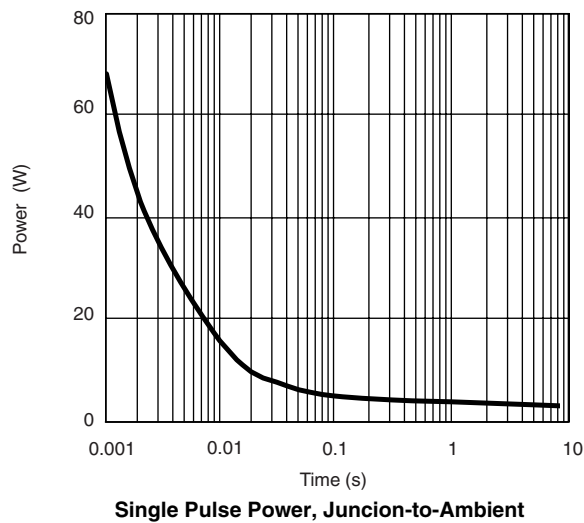
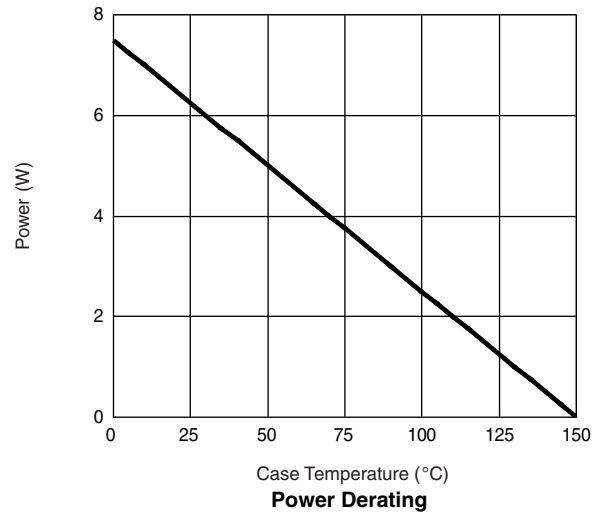
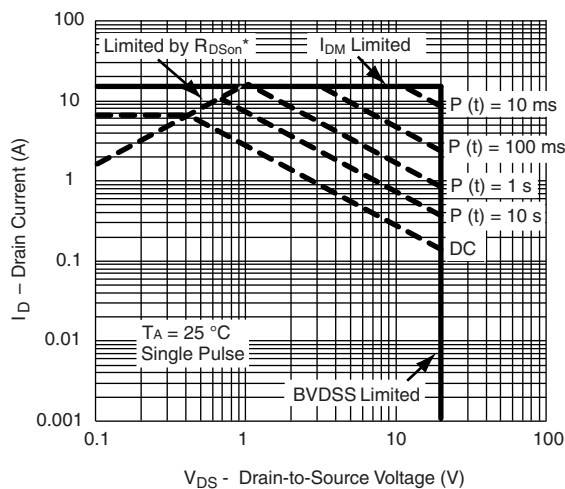
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



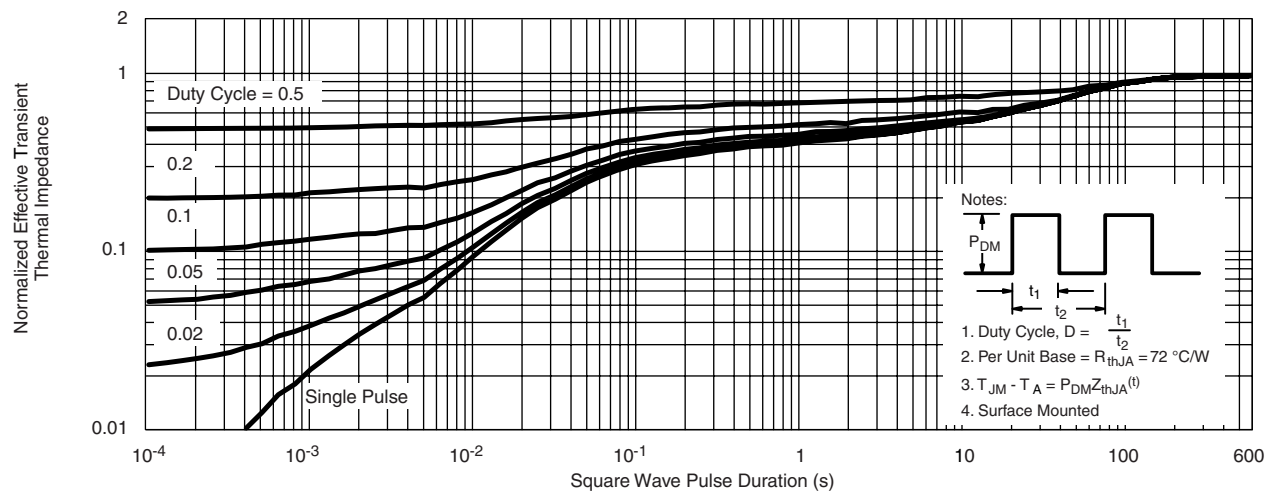
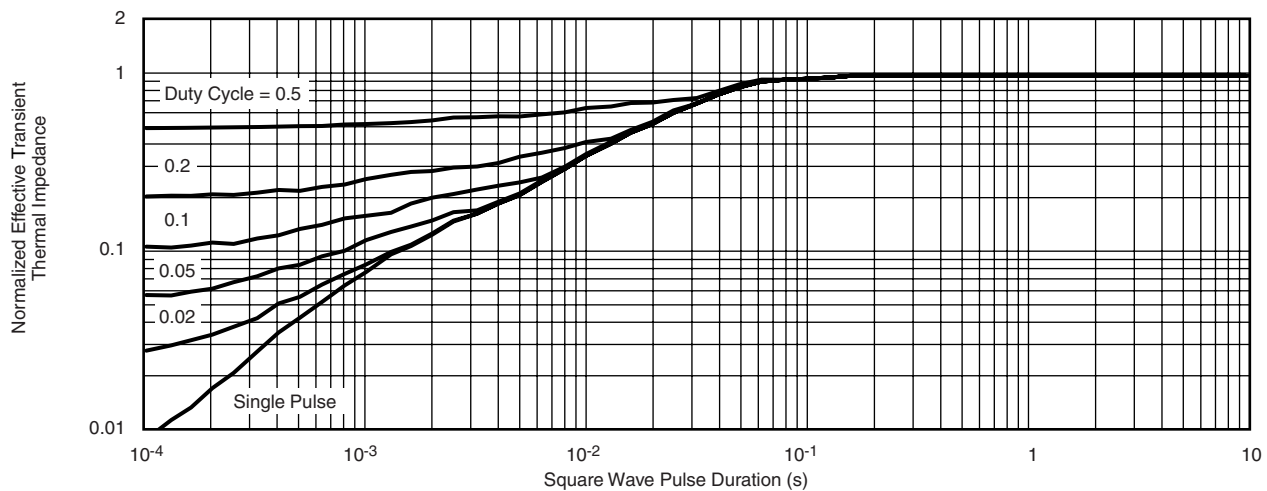
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 $R_{DS(on)}$ vs. Drain Current

On-Resistance vs. Junction Temperature

Capacitance

Forward Diode Voltage vs. Temp.

Gate Charge

 $R_{DS(on)}$ vs. V_{GS} vs Temperature

TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



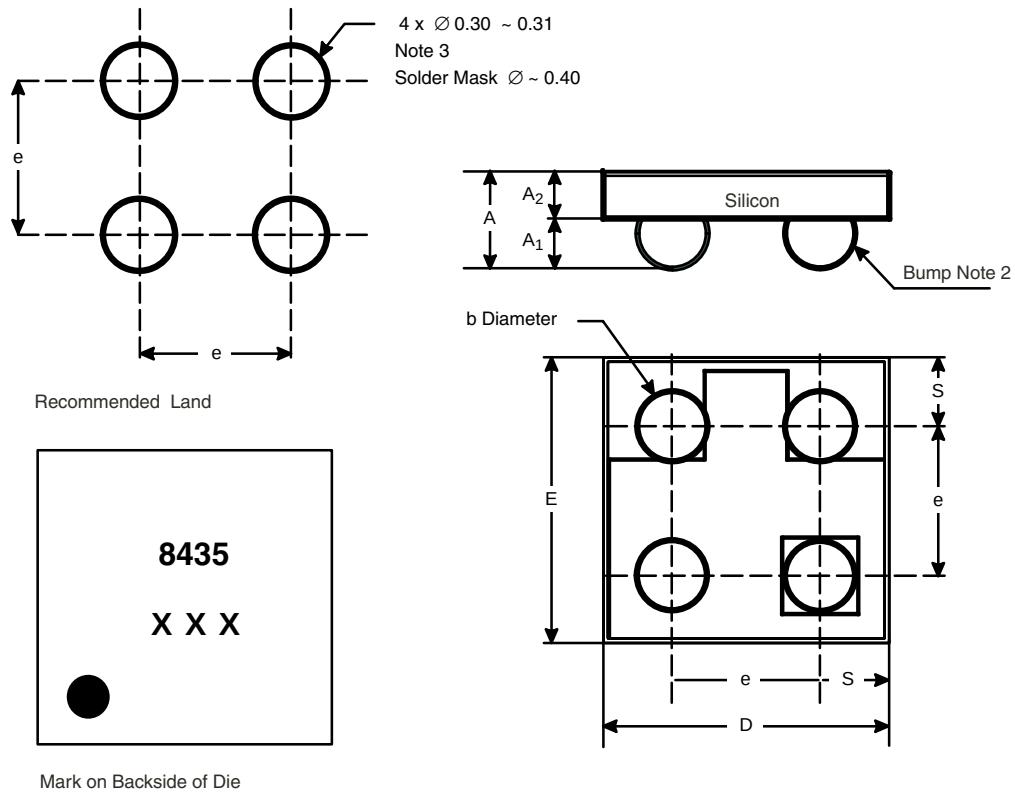
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

** The power dissipation P_D is based on $T_{J(max)} = 150^\circ\text{C}$, using junction-to-foot thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (2 x 2, 0.8 mm PITCH)



Notes (Unless Otherwise Specified):

1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are Sn/Ag/Cu.
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A ₁	0.260	0.290	0.0102	0.0114
A ₂	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.750	0.850	0.0295	0.0335
S	0.370	0.380	0.0146	0.0150

Notes:

- a. Use millimeters as the primary measurement.

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