LP2996A DDR 终端稳压器

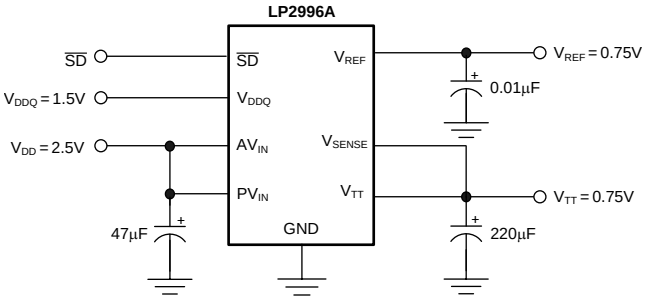
1 特性

- V_{DDQ} 最小值为 1.35V
- 拉电流和灌电流
- 低输出电压偏移
- 无需外部电阻
- 线性拓扑
- 挂起到 RAM (STR) 功能
- 低外部元件数
- 热关断
- -40°C 至 125°C 条件下推荐使用 LP2998/8Q

2 应用

- DDR1、DDR2、DDR3 和 DDR3L 端接电压
- FPGA
- 工业/医疗 PC
- SSTL-2 和 SSTL-3 端接
- HSTL 端接

简化电路原理图



3 说明

LP2996A 线性稳压器的设计符合 DDR-SDRAM 端接的 JEDEC SSTL-2 规范。 此器件还支持 DDR2、DDR3 和 DDR3L VTT 总线端接，V_{DDQ} 最小值为 1.35V。 此器件包含高速运算放大器，可提供出色的负载瞬变响应。 输出级可防止在 DDR-SDRAM 端接所需的应用中提供 1.5A 连续电流和最大 3A 的瞬态峰值电流时发生直通。 LP2996A 还包含一个 V_{SENSE} 引脚（用于提供出色的负载调节），以及一个 V_{REF} 输出（作为芯片组和 DIMM 的参考）。

LP2996A 的一个附加特性是具有一个低电平有效关断 ($\overline{SD}$) 引脚，该引脚提供“挂起到 RAM”(STR) 功能。 当 $\overline{SD}$ 下拉时，V_{TT} 输出将变为三态，并提供高阻抗输出，但 V_{REF} 将保持有效。 在此模式下，可通过较低的静态电流获得节能优势。

器件信息(1)

部件号	封装	封装尺寸（标称值）
LP2996A	SO PowerPAD (8)	4.89mm x 3.90mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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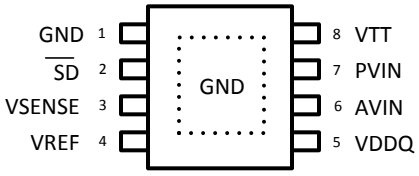
4 修订历史记录

日期	修订版本	注释
2014 年 6 月	*	最初发布。

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5 Pin Configuration and Functions

SO PowerPAD
8 LEAD DDA
TOP VIEW



Pin Functions

PIN	TYPE	DESCRIPTION
1	GND	Ground
2	$\overline{SD}$	Shutdown
3	VSENSE	Feedback pin for regulating V_{TT}.
4	VREF	Buffered internal reference voltage of $V_{DDQ}/2$
5	VDDQ	Input for internal reference equal to $V_{DDQ}/2$
6	AVIN	Analog input pin
7	PVIN	Power input pin
8	VTT	Output voltage for connection to termination resistors
	EP	Exposed pad thermal connection. Connect to Ground.

5.1 Pin Descriptions

AVIN AND PVIN	AVIN and PVIN are the input supply pins for the LP2996A. AVIN is used to supply all the internal control circuitry. PVIN, however, is used exclusively to provide the rail voltage for the output stage used to create VTT. These pins have the capability to work off separate supplies depending on the application. Higher voltages on PVIN will increase the maximum continuous output current because of output RDSON limitations at voltages close to VTT. The disadvantage of high values of PVIN is that the internal power loss will also increase, thermally limiting the design. For SSTL-2 applications, a good compromise would be to connect the AVIN and PVIN directly together at 2.5 V. This eliminates the need for bypassing the two supply pins separately. The only limitation on input voltage selection is that PVIN must be equal to or lower than AVIN. It is recommended to connect PVIN to voltage rails equal to or less than 3.3 V to prevent the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown than the part will enter a shutdown state identical to the manual shutdown where V_{TT} is tri-stated and V_{REF} remains active.
VDDQ	VDDQ is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50 kΩ resistors. This ensures that V_{TT} will track VDDQ / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 2.5 V rail at the DIMM instead of AVIN and PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications VDDQ will be a 2.5 V signal, which will create a 1.25 V termination voltage at V_{TT} (See *Electrical Characteristics* Table for exact values of V_{TT} over temperature).
V_{SENSE}	The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the LP2996A then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The V_{SENSE} pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the V_{SENSE} pin must still be connected to V_{TT}. Care should be taken when a long V_{SENSE} trace is implemented in close proximity to the memory. Noise pickup in the V_{SENSE} trace can cause problems with precise regulation of V_{TT}. A small 0.1 uF ceramic capacitor placed next to the V_{SENSE} pin can help filter any high frequency signals and preventing errors.
SHUTDOWN	The LP2996A contains an active low shutdown pin that can be used to tri-state VTT. During shutdown V_{TT} should not be exposed to voltages that exceed AVIN. With the shutdown pin asserted low the quiescent current of the LP2996A will drop, however, V_{DDQ} will always maintain its constant impedance of 100 kΩ for generating the internal reference. Therefore to calculate the total power loss in shutdown both currents need to be considered. For more information refer to the *Thermal Dissipation* section. The shutdown pin also has an internal pull-up current, therefore to turn the part on the shutdown pin can either be connected to AVIN or left open.

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Pin Descriptions (continued)

V_{REF}	V_{REF} provides the buffered output of the internal reference voltage VDDQ / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically an extremely high impedance, there should be little current drawn from V_{REF}. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1 µF to 0.01 µF is recommended. This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.
V_{TT}	V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VDDQ / 2. The LP2996A is designed to handle peak transient currents of up to ± 3 A with a fast transient response. The maximum continuous current is a function of V_{IN} and can be viewed in the *Typical Performance Characteristics* section. If a transient is expected to last above the maximum continuous current rating for a significant amount of time then the output capacitor should be sized large enough to prevent an excessive voltage drop. Despite the fact that the LP2996A is designed to handle large transient output currents it is not capable of handling these for long durations, under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal derating should always be used (please refer to the *Thermal Dissipation* section). If the junction temperature exceeds the thermal shutdown point than V_{TT} will tri-state until the part returns below the hysteretic trip-point.

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	AVIN to GND	−0.3	6	V
	PVIN to GND	–0.3	AVIN	
	VDDQ (3)	−0.3	6	V
	Junction Temperature		150	°C
	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)		1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Junction Temp. Range (1)	0		125	°C
AVIN to GND	2.2		5.5	V
PVIN Supply Voltage	0		AVIN	
SD Input Voltage	0		AVIN	

(1) At elevated temperatures, devices must be derated based on thermal resistance.

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6.4 Thermal Information

THERMAL METRIC(1)(2)(3)		SO PowerPAD-8 DDA	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.5	
ψ_{JT}	Junction-to-top characterization parameter	15.9	
ψ_{JB}	Junction-to-board characterization parameter	36.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7
(3) Thermal Resistances were simulated on a 4 layer, JEDEC board.

6.5 Electrical Characteristics

Specifications are for T_J = 25°C and apply over the full Operating Temperature Range (T_J = 0°C to +125°C)(1). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	V_{REF} voltage (DDR I)	VIN = VDDQ = 2.3 V	1.135	1.158	1.185	V
		VIN = VDDQ = 2.5 V	1.235	1.258	1.285	
		VIN = VDDQ = 2.7 V	1.335	1.358	1.385	
	V_{REF} voltage (DDR II)	PVIN = VDDQ = 1.7 V	0.837	0.860	0.887	
		PVIN = VDDQ = 1.8 V	0.887	0.910	0.937	
		PVIN = VDDQ = 1.9 V	0.936	0.959	0.986	
	V_{REF} Voltage (DDR III)	PVIN = VDDQ = 1.35V	0.669	0.684	0.699	
		PVIN = VDDQ = 1.5V	0.743	0.758	0.773	
		PVIN = VDDQ = 1.6V	0.793	0.808	0.823	
Z_{VREF}	V_{REF} Output Impedance	I_{REF} = –30 to +30 µA		2.5		kΩ
V_{TT}	V_{TT} Output Voltage (DDR I) (3)	I_{OUT} = 0 A				V
		VIN = VDDQ = 2.3 V	1.120	1.159	1.190	
		VIN = VDDQ = 2.5 V	1.210	1.259	1.290	
		VIN = VDDQ = 2.7 V	1.320	1.359	1.390	
		I_{OUT} = +/– 1.5 A				
		VIN = VDDQ = 2.3 V	1.125	1.159	1.190	
		VIN = VDDQ = 2.5 V	1.225	1.259	1.290	
		VIN = VDDQ = 2.7 V	1.325	1.359	1.390	
	V_{TT} Output Voltage (DDR II) (3)	I_{OUT} = 0 A, AVIN = 2.5 V				V
		PVIN = VDDQ = 1.7 V	0.822	0.856	0.887	
		PVIN = VDDQ = 1.8 V	0.874	0.908	0.939	
		PVIN = VDDQ = 1.9 V	0.923	0.957	0.988	
		I_{OUT} = +/– 0.5A, AVIN = 2.5 V				
		PVIN = VDDQ = 1.7 V	0.820	0.856	0.890	
		PVIN = VDDQ = 1.8 V	0.870	0.908	0.940	
		PVIN = VDDQ = 1.9 V	0.920	0.957	0.990	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).
(2) VIN is defined as VIN = AVIN = PVIN.
(3) V_{TT} load regulation is tested by using a 10 ms current pulse and measuring V_{TT}.

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Electrical Characteristics (continued)

Specifications are for T_J = 25°C and apply over the full Operating Temperature Range (T_J = 0°C to +125°C)(1). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V_{TT} Output Voltage (DDR III) (3)	I_{OUT} = 0A, AVIN = 2.5 V				V
		PVIN = VDDQ = 1.35V	0.656	0.677	0.698	
		PVIN = VDDQ = 1.5 V	0.731	0.752	0.773	
		PVIN = VDDQ = 1.6 V	0.781	0.802	0.823	
		I_{OUT} = +0.2A, AVIN = 2.5V PVIN = VDDQ = 1.35V	0.667	0.688	0.710	
		I_{OUT} = -0.2A, AVIN = 2.5V PVIN = VDDQ = 1.35V	0.641	0.673	0.694	
		I_{OUT} = +0.4 A, AVIN = 2.5 V PVIN = VDDQ = 1.5 V	0.740	0.763	0.786	
		I_{OUT} = –0.4 A, AVIN = 2.5 V PVIN = VDDQ = 1.5 V	0.731	0.752	0.773	
		I_{OUT} = +0.5A, AVIN = 2.5 V PVIN = VDDQ = 1.6 V	0.790	0.813	0.836	
		I_{OUT} = -0.5 A, AVIN = 2.5 V PVIN = VDDQ = 1.6 V	0.781	0.802	0.823	
VOS_{Vtt}	V_{TT} Output Voltage Offset (V_{REF} – V_{TT}) for DDR I (3)	I_{OUT} = 0 A	–30	0	30	mV
		I_{OUT} = –1.5 A	–30	0	30	
		I_{OUT} = 1.5 A	–30	0	30	
	V_{TT} Output Voltage Offset (V_{REF} – V_{TT}) for DDR II (3)	I_{OUT} = 0 A	–30	0	30	
		I_{OUT} = –0.5 A	–30	0	30	
		I_{OUT} = 0.5 A	–30	0	30	
	V_{TT} Output Voltage Offset (V_{REF} – V_{TT}) for DDR III (3)	I_{OUT} = 0 A	–30	0	30	
		I_{OUT} = ±0.2 A	–30	0	30	
		I_{OUT} = ±0.4 A	–30	0	30	
		I_{OUT} = ±0.5 A	–30	0	30	
I_Q	Quiescent Current (4)	I_{OUT} = 0 A		320	500	µA
Z_{VDDQ}	VDDQ Input Impedance			100		kΩ
I_{SD}	Quiescent current in shutdown (4)	SD = 0 V		115	150	µA
I_{Q_SD}	Shutdown leakage current	SD = 0 V		2	5	
V_{IH}	Minimum Shutdown High Level		1.9			V
V_{IL}	Maximum Shutdown Low Level				0.8	
Iv	V_{TT} leakage current in shutdown	SD = 0 V V_{TT} = 1.25 V		1	10	µA
I_{SENSE}	V_{SENSE} Input current			13		nA
T_{SD}	Thermal Shutdown (5)			165		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			10		

(4) Quiescent current defined as the current flow into AVIN.
(5) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

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6.6 Typical Performance Characteristics

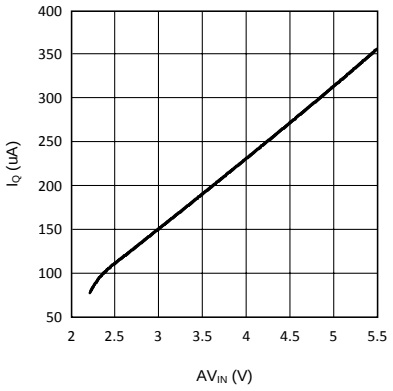


Figure 1. IQ vs AV_{IN} In SD

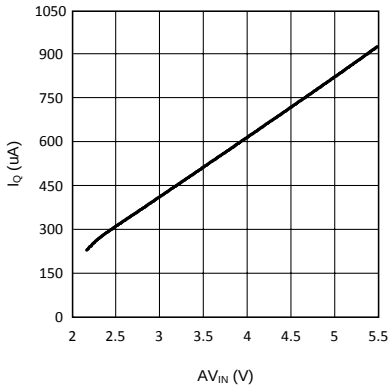


Figure 2. IQ vs Av_{IN}

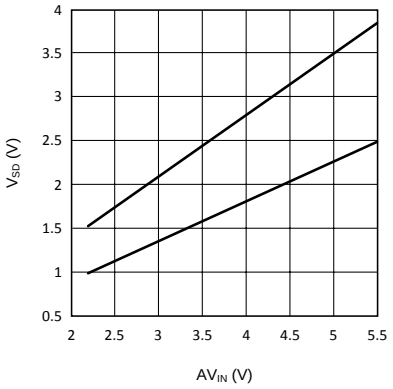


Figure 3. V_{IH} and V_{IL}

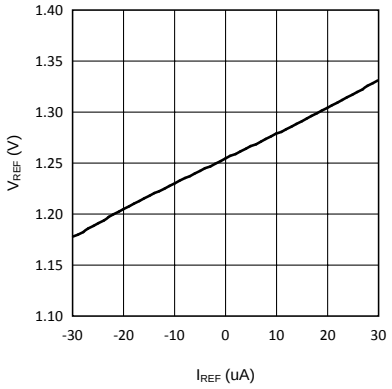


Figure 4. V_{REF} vs I_{REF}

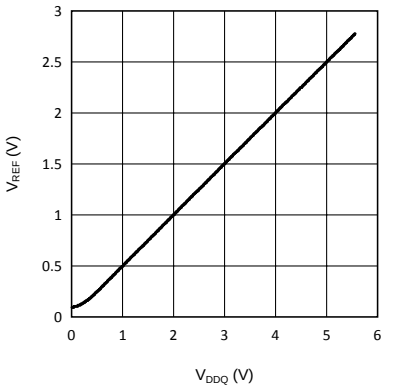


Figure 5. V_{REF} vs V_{DDQ}

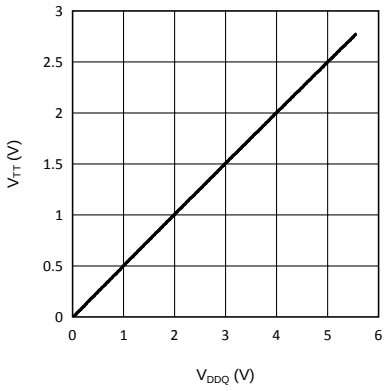


Figure 6. V_{TT} vs V_{DDQ}

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Typical Performance Characteristics (continued)

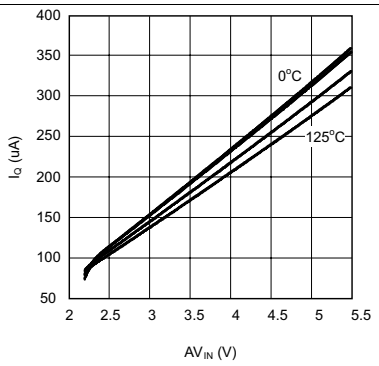


Figure 7. IQ vs AF_{IN} in SD Temperature

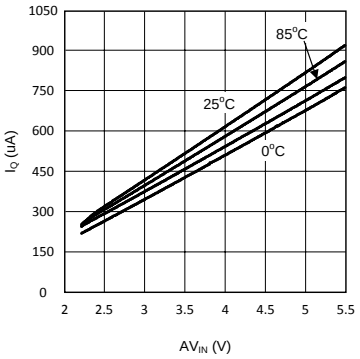


Figure 8. IQ vs AV_{IN} Temperature

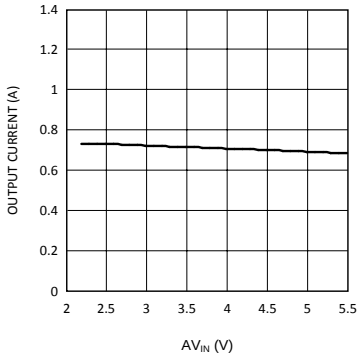


Figure 9. Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5 V, PV_{IN} = 1.8 V)

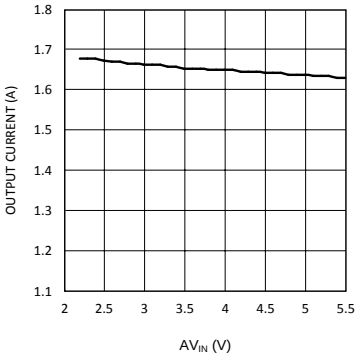


Figure 10. Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5 V, PV_{IN} = 2.5 V)

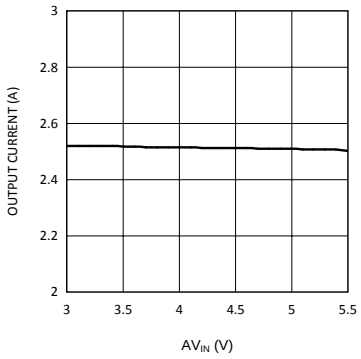


Figure 11. Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5 V, PV_{IN} = 3.3 V)

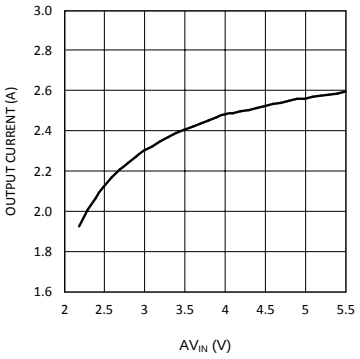


Figure 12. Maximum Sinking Current vs AV_{IN} (V_{DDQ} = 2.5 V)

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Typical Performance Characteristics (continued)

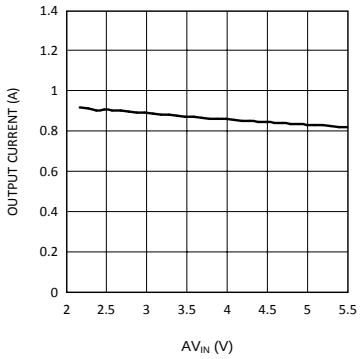


Figure 13. Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 1.8 V, PV_{IN} = 1.8 V)

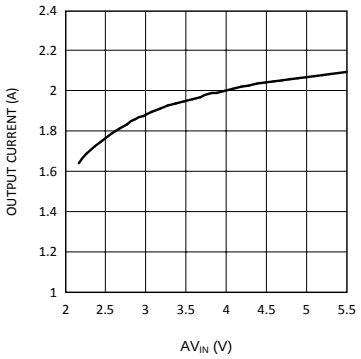


Figure 14. Maximum Sinking Current vs AV_{IN} (V_{DDQ} = 1.8 V)

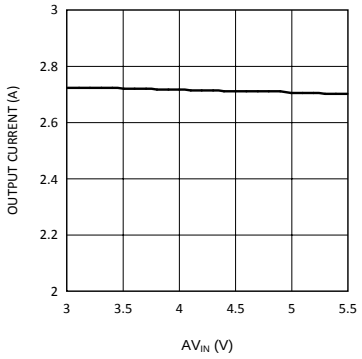


Figure 15. Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 1.8 V, PV_{IN} = 3.3 V)

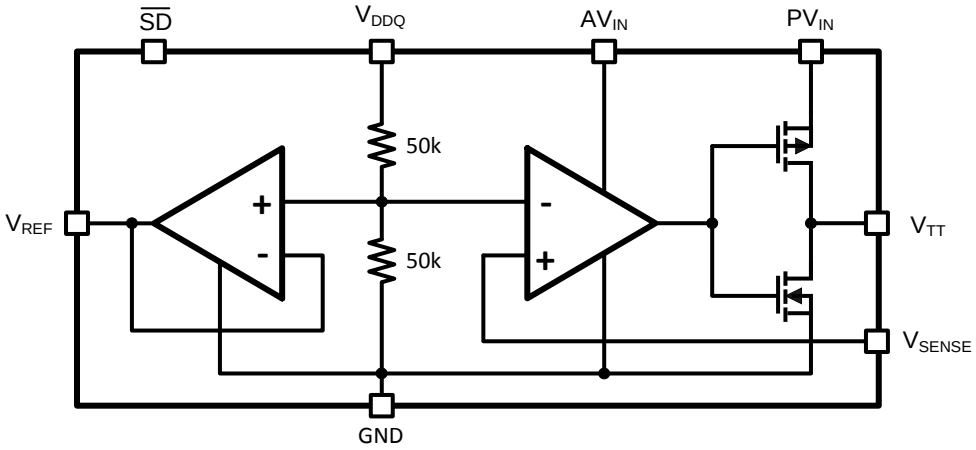
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7 Detailed Description

7.1 Overview

The LP2996A linear regulator is designed to meet the JEDEC SSTL-2 specifications for termination of DDR-SDRAM. The device also supports DDR2, DDR3 and DDR3L VTT bus termination with V_{DDQ} min of 1.35V. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination.

7.2 Functional Block Diagram



7.3 Feature Description

The LP2996A is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-2. The output, V_{TT} is capable of sinking and sourcing current while regulating the output voltage equal to VDDQ / 2. The output stage has been designed to maintain excellent load regulation while preventing shoot through. The LP2996A also incorporates two distinct power rails that separates the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the LP2996A to provide a termination solution for DDR2-SDRAM, DDR3-SDRAM and DDR3L-SDRAM memory. For wide temperature designs, the LP2998/8Q is recommended for all DDR applications.

7.4 Device Functional Modes

The LP2996A can also be used to provide a termination voltage for other logic schemes such as SSTL-3 or HSTL. Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one R_S series resistor from the chipset to the memory and one R_T termination resistor. Typical values for R_S and R_T are 25 Ω, although these can be changed to scale the current requirements from the LP2996A. This implementation can be seen below in Figure 16.

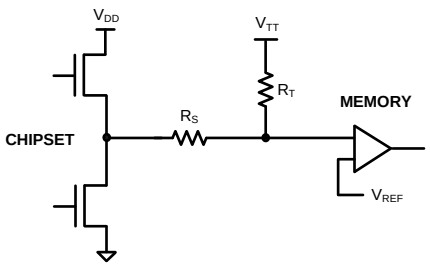


Figure 16. SSTL-Termination Scheme

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8 Applications and Implementation

8.1 Application Information

8.1.1 Input Capacitor

The LP2996A does not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 50 µF. Ceramic capacitors can also be used, a value in the range of 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2996A is placed close to the bulk capacitance from the output of the 2.5 V DC-DC converter. If the two supply rails (AVIN and PVIN) are separated then the 47 uF capacitor should be placed as close to possible to the PVIN rail. An additional 0.1 uF ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

8.1.2 Output Capacitor

The LP2996A has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). This allows the flexibility to use any capacitor desired. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of V_{TT}. As a general recommendation the output capacitor should be sized above 100 µF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are highlighted below:

AL - It should be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP2996A. To improve the ESR several AL electrolytics can be combined in parallel for an overall reduction. An important note to be aware of is the extent at which the ESR will change over temperature. Aluminum electrolytic capacitors can have their ESR rapidly increase at cold temperatures.

Ceramic - Ceramic capacitors typically have a low capacitance, in the range of 10 to 100 µF range, but they have excellent AC performance for bypassing noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance it is recommended to use ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. A dielectric of X5R or better is recommended for all ceramic capacitors.

Hybrid - Several hybrid capacitors such as OS-CON and SP are available from several manufacturers. These offer a large capacitance while maintaining a low ESR. These are the best solution when size and performance are critical, although their cost is typically higher than any other capacitor.

8.1.3 Thermal Dissipation

Since the LP2996A is a linear regulator any current flow from V_{TT} will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise (T_{Rmax}) can be calculated given the maximum ambient temperature (T_{Amax}) of the application and the maximum allowable junction temperature (T_{Jmax}).

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (1)$$

From this equation, the maximum power dissipation (P_{Dmax}) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA} \quad (2)$$

The θ_{JA} of the LP2996A will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow.

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Application Information (continued)

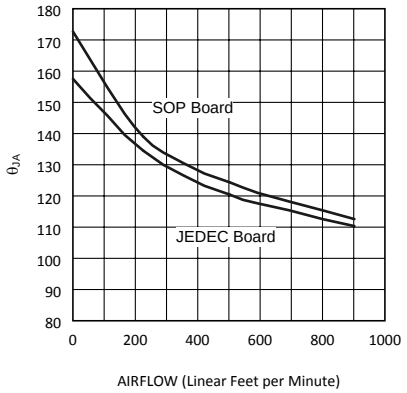


Figure 17. Θ_{JA} vs Airflow

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout it is possible to reduce the θ_{JA} further than the nominal values shown in Figure 17.

Layout is also extremely critical to maximize the output current with the SO PowerPAD package. By simply placing vias under the DAP the θ_{JA} can be lowered significantly.

Additional improvements in lowering the θ_{JA} can also be achieved with a constant airflow across the package. Maintaining the same conditions as above and utilizing the 2x2 via array, Figure 18 shows how the θ_{JA} varies with airflow.

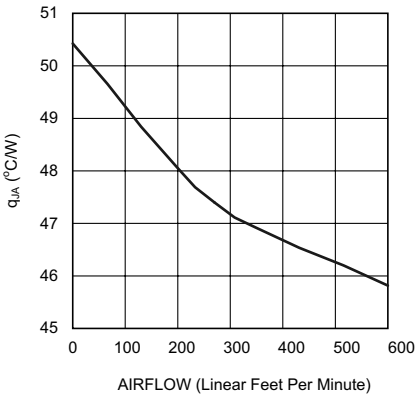


Figure 18. Θ_{JA} vs Airflow Speed (Jedec Board with 4 Vias)

Optimizing the θ_{JA} and placing the LP2996A in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at V_{TT}, either sinking or sourcing, and quiescent current at AVIN and VDDQ. During the active state (when shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT}$$

where (3)

$$P_{AVIN} = I_{AVIN} * V_{AVIN} \quad (4)$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ} \quad (5)$$

To calculate the maximum power dissipation at V_{TT} both conditions at V_{TT} need to be examined, sinking and sourcing current. Although only one equation will add into the total, V_{TT} cannot source and sink current simultaneously.

$$P_{VTT} = V_{VTT} \times I_{LOAD} \text{ (Sinking) or} \quad (6)$$

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Application Information (continued)

$$P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD} \text{ (Sourcing} \quad (7)$$

The power dissipation of the LP2996A can also be calculated during the shutdown state. During this condition the output V_{TT} will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AVIN and the constant impedance that is seen at the VDDQ pin.

$$P_D = P_{AVIN} + P_{VDDQ} \quad (8)$$

$$P_{AVIN} = I_{AVIN} \times V_{AVIN} \quad (9)$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ} \quad (10)$$

8.2 Typical Application

Several different application circuits are shown below to illustrate some of the options that are possible in configuring the LP2996A. Graphs of the individual circuit performance can be found in the Typical Performance Characteristics section in the beginning of the datasheet. These curves illustrate how the maximum output current is affected by changes in AVIN and PVIN.

8.2.1 Typical Application Circuit

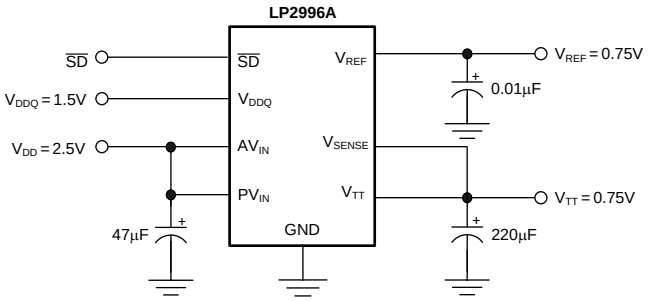


Figure 19. Typical Application Circuit

8.2.2 DDR-III Applications

With the separate VDDQ pin and an internal resistor divider it is possible to use the LP2996A in applications utilizing DDR-III memory. The output stage is connected to the 1.5 V rail and the AVIN pin can be connected to a 2.2 V - 5.5 V rail.

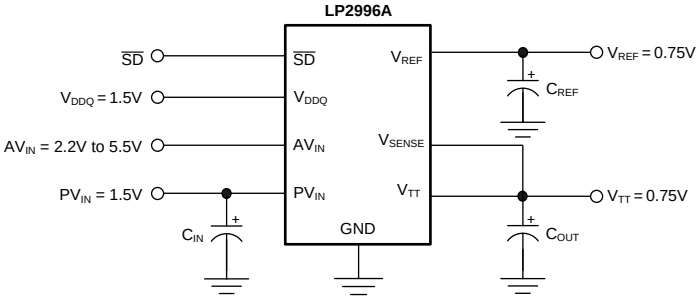


Figure 20. Recommended DDR-III Termination

If it is not desirable to use the 1.5 V - 2.5 V rail it is possible to connect the output stage to a 3.3 V rail. Care should be taken to not exceed the maximum junction temperature as the thermal dissipation increases with lower V_{TT} output voltages. For this reason it is not recommended to power PVIN off a rail higher than the nominal 3.3 V. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

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Typical Application (continued)

8.2.3 DDR-II Applications

With the separate VDDQ pin and an internal resistor divider it is possible to use the LP2996A in applications utilizing DDR-II memory. Figure 24 and Figure 25 show several implementations of recommended circuits with output curves displayed in the Typical Performance Characteristics. Figure 24 shows the recommended circuit configuration for DDR-II applications. The output stage is connected to the 1.8 V rail and the AVIN pin can be connected to either a 3.3 V or 5 V rail. For DDR-III and DDR-III low power designs in wider temperature applications, the LP2998/Q is recommended.

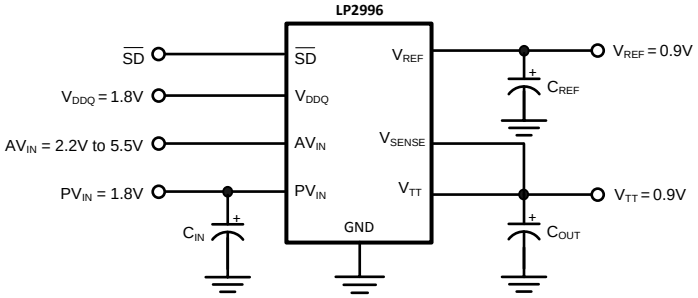


Figure 21. Recommended DDR-II Termination

If it is not desirable to use the 1.8 V rail it is possible to connect the output stage to a 3.3 V rail. Care should be taken to not exceed the maximum junction temperature as the thermal dissipation increases with lower V_{TT} output voltages. For this reason it is not recommended to power PVIN off a rail higher than the nominal 3.3 V. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

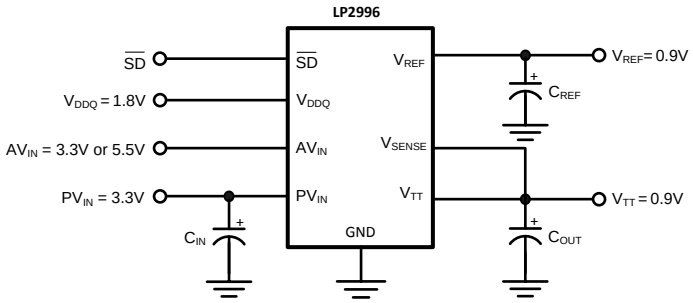


Figure 22. DDR-II Termination with Higher Voltage Rails

8.2.4 SSTL-2 Applications

For the majority of applications that implement the SSTL-2 termination scheme it is recommended to connect all the input rails to the 2.5 V rail. This provides an optimal trade-off between power dissipation and component count and selection. An example of this circuit can be seen in Figure 23.

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Typical Application (continued)

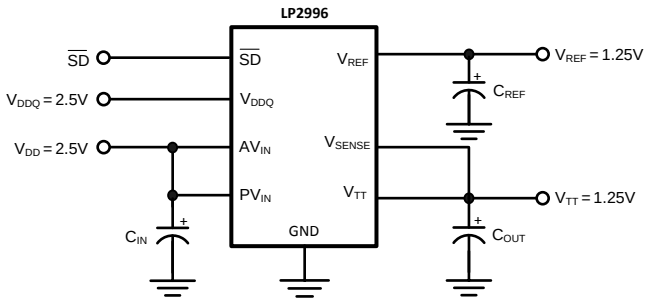


Figure 23. Recommended SSTL-2 Implementation

If power dissipation or efficiency is a major concern then the LP2996A has the ability to operate on split power rails. The output stage (PVIN) can be operated on a lower rail such as 1.8 V and the analog circuitry (AVIN) can be connected to a higher rail such as 2.5 V, 3.3 V or 5 V. This allows the internal power dissipation to be lowered when sourcing current from V_{TT}. The disadvantage of this circuit is that the maximum continuous current is reduced because of the lower rail voltage, although it is adequate for all motherboard SSTL-2 applications. Increasing the output capacitance can also help if periods of large load transients will be encountered.

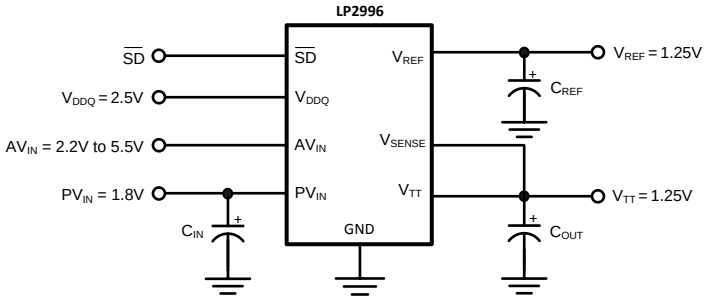


Figure 24. Lower Power Dissipation SSTL-2 Implementation

The third option for SSTL-2 applications in the situation that a 1.8 V rail is not available and it is not desirable to use 2.5 V, is to connect the LP2996A power rail to 3.3 V. In this situation AVIN will be limited to operation on the 3.3 V or 5 V rail as PVIN can never exceed AVIN. This configuration has the ability to provide the maximum continuous output current at the downside of higher thermal dissipation. Care should be taken to prevent the LP2996A from experiencing large current levels which cause the junction temperature to exceed the maximum. Because of this risk it is not recommended to supply the output stage with a voltage higher than a nominal 3.3 V rail.

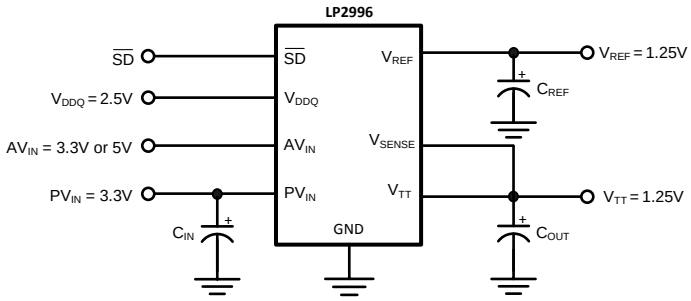


Figure 25. SSTL-2 Implementation with Higher Voltage Rails

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Typical Application (continued)

8.2.5 Level Shifting

If standards other than SSTL-2 are required, such as SSTL-3, it may be necessary to use a different scaling factor than 0.5 times V_{DDQ} for regulating the output voltage. Several options are available to scale the output to any voltage required. One method is to level shift the output by using feedback resistors from V_{TT} to the V_{SENSE} pin. This has been illustrated in Figure 26 and Figure 27. Figure 26 shows how to use two resistors to level shift V_{TT} above the internal reference voltage of VDDQ/2. To calculate the exact voltage at V_{TT} the following equation can be used.

$$V_{TT} = VDDQ/2 \ (1 + R1/R2) \quad (11)$$

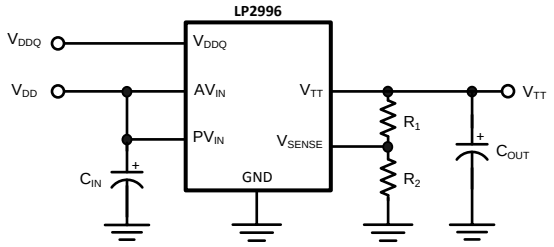


Figure 26. Increasing VTT by Level Shifting

Conversely, the R2 resistor can be placed between V_{SENSE} and V_{DDQ} to shift the V_{TT} output lower than the internal reference voltage of VDDQ/2. The equations relating VTT and the resistors can be seen below:

$$V_{TT} = VDDQ/2 \ (1 - R1/R2) \quad (12)$$

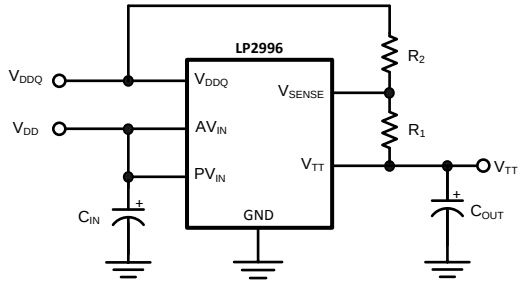


Figure 27. Decreasing VTT by Level Shifting

8.2.5.1 Output Capacitor Selection

For applications utilizing the LP2996A to terminate SSTL-2 I/O signals the typical application circuit shown in Figure 27 can be implemented.

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where V_{TT} is distributed across a long plane it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. Figure 28 shown below depicts an example circuit where 2 bulk output capacitors could be situated at both ends of the V_{TT} plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.

In most PC applications an extensive amount of decoupling is required because of the long interconnects encountered with the DDR-SDRAM DIMMs mounted on modules. As a result bulk aluminum electrolytic capacitors in the range of 1000uF are typically used.

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Typical Application (continued)

8.2.6 HSTL Applications

The LP2996A can be easily adapted for HSTL applications by connecting V_{DDQ} to the 1.5 V rail. This will produce a V_{TT} and V_{REF} voltage of approximately 0.75 V for the termination resistors. AVIN and PVIN should be connected to a 2.5 V rail for optimal performance.

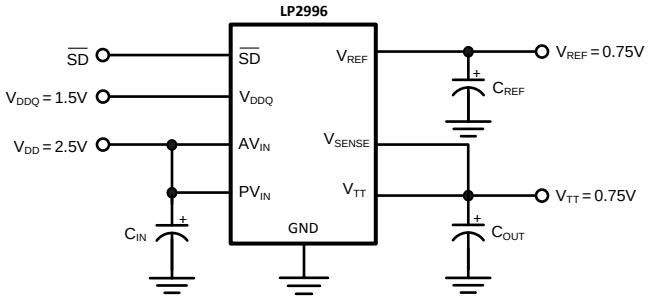


Figure 28. HSTL Application

8.2.7 QDR Applications

Quad data rate (QDR) applications utilize multiple channels for improved memory performance. However, this increase in bus lines has the effect of increasing the current levels required for termination. The recommended approach in terminating multiple channels is to use a dedicated LP2996A for each channel. This simplifies layout and reduces the internal power dissipation for each regulator. Separate V_{REF} signals can be used for each DIMM bank from the corresponding regulator with the chipset reference provided by a local resistor divider or one of the LP2996A signals. Because V_{REF} and V_{TT} are expected to track and the part to part variations are minor, there should be little difference between the reference signals of each LP2996A.

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9 Power Supply Recommendations

There are several recommendations for the LP2996A input power supply. An input capacitor is not required but is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 50 µF. Ceramic capacitors can also be used, a value in the range of 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2996A is placed close to the bulk capacitance from the output of the 2.5 V DC-DC converter. If the two supply rails (AVIN and PVIN) are separated then the 47 uF capacitor should be placed as close to possible to the PVIN rail. An additional 0.1 uF ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

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10 Layout

10.1 Layout Guidelines

1. The input capacitor for the power rail should be placed as close as possible to the PVIN pin.
2. V_{SENSE} should be connected to the V_{TT} termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
3. V_{DDQ} can be connected remotely to the V_{DDQ} rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the V_{SENSE} trace to avoid noise pickup from switching I/O signals. A 0.1uF ceramic capacitor located close to the $_{SENSE}$ can also be used to filter any unwanted high frequency signal. This can be an issue especially if long $_{SENSE}$ traces are used.
6. V_{REF} should be bypassed with a 0.01 µF or 0.1 µF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the V_{REF} pin.

10.2 Layout Examples

The LP2996A layout is very similar to the LP2998/Q layout. This is because the main difference between the two IC's is the wider temperature range, -40°C to 125°C, which the LP2998/Q offers. As such, the below example shows the layout from a LP2998EVM. These layout examples can be used to evaluate the LP2996A.

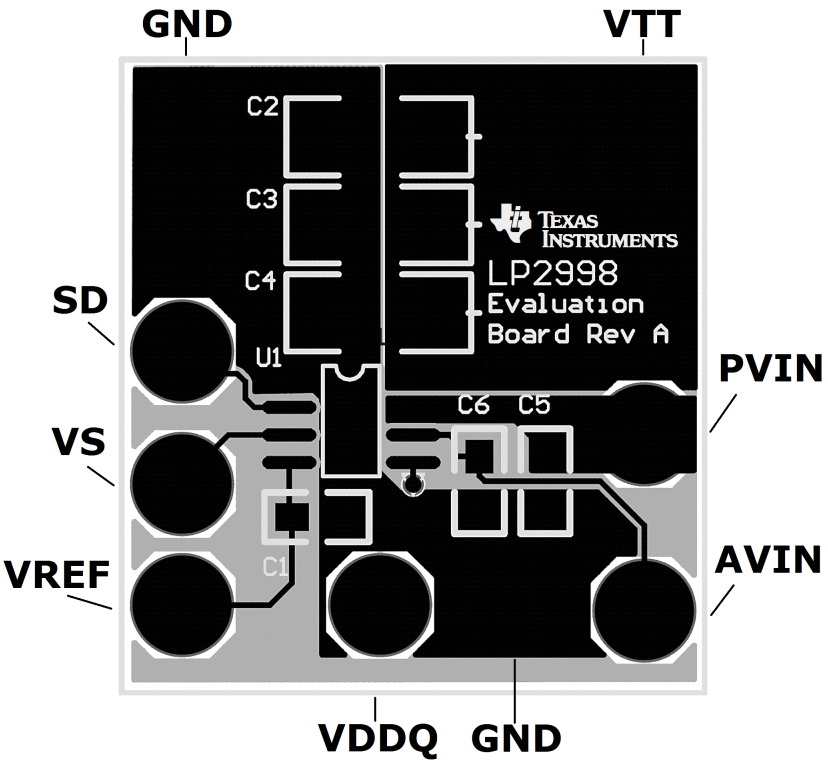


Figure 29. LP2998EVM SO PowerPAD Layout Example (Front)

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Layout Examples (continued)

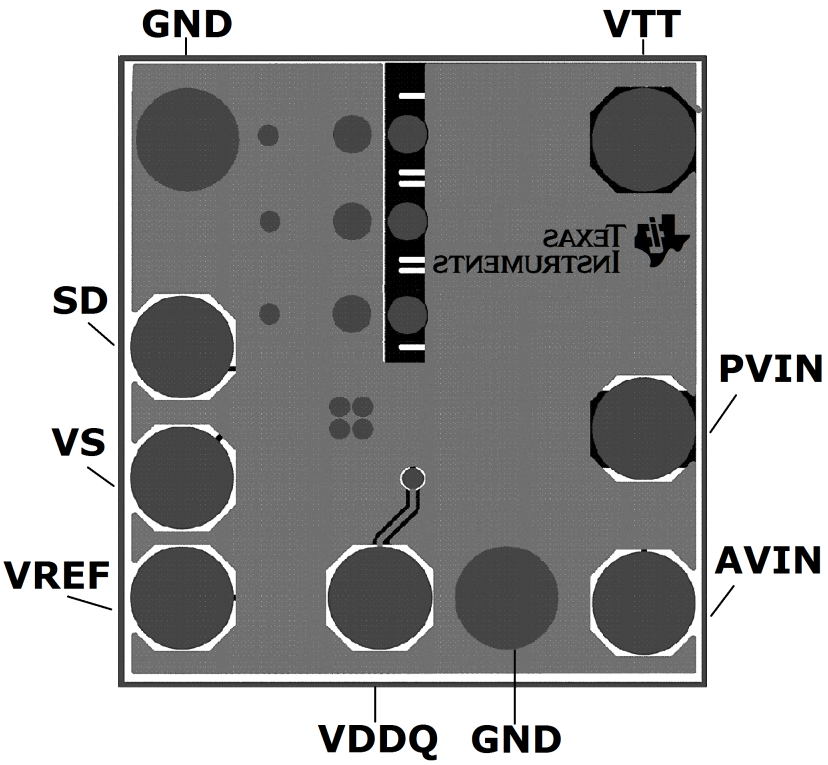


Figure 30. LP2998EVM SO PowerPAD Layout Example (Back)

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11 器件和文档支持

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11.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2996AMR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	0 to 125	LP2996 AMR	Samples
LP2996AMRE/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	0 to 125	LP2996 AMR	Samples
LP2996AMRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	0 to 125	LP2996 AMR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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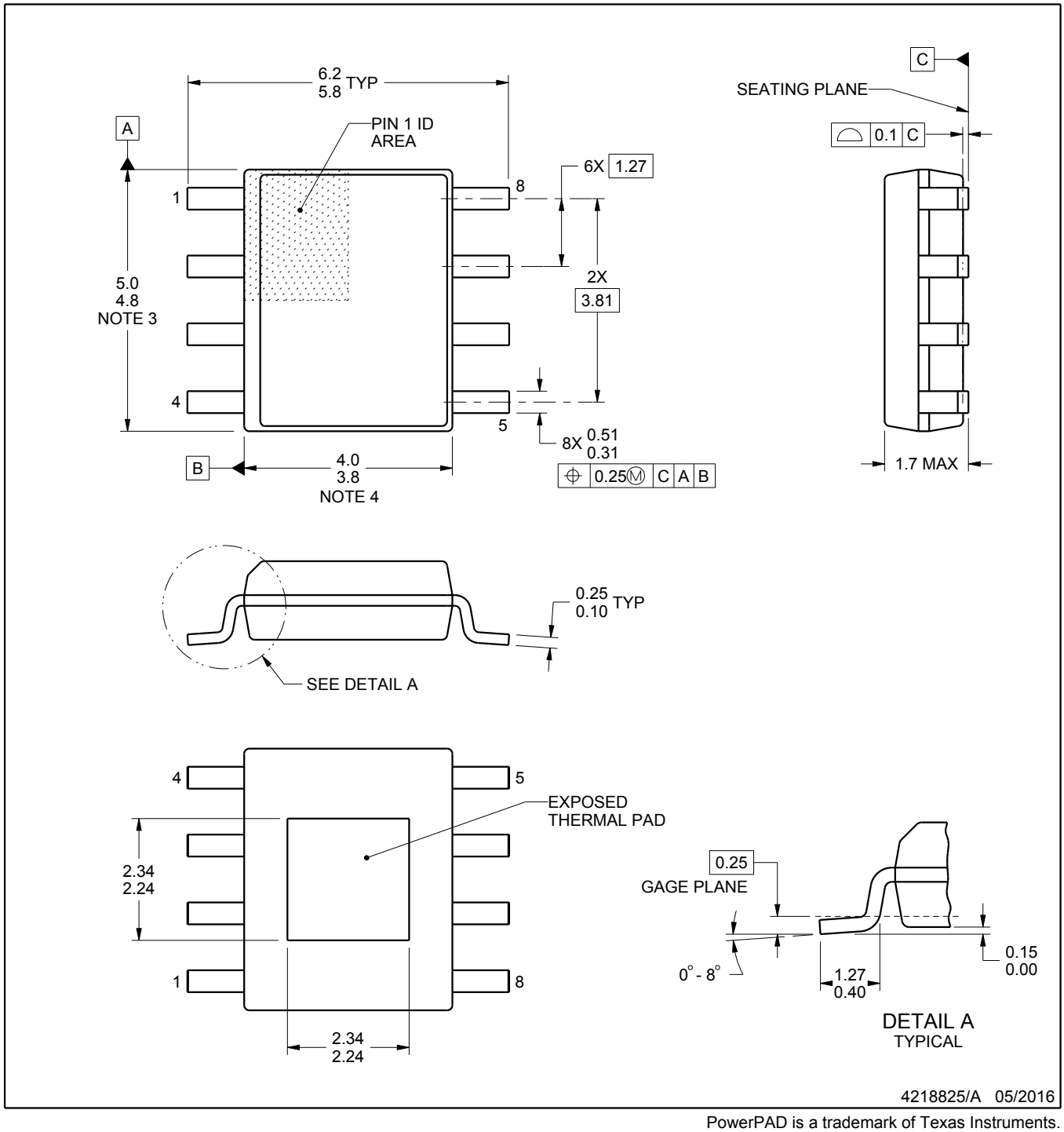
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PACKAGE OUTLINE

DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

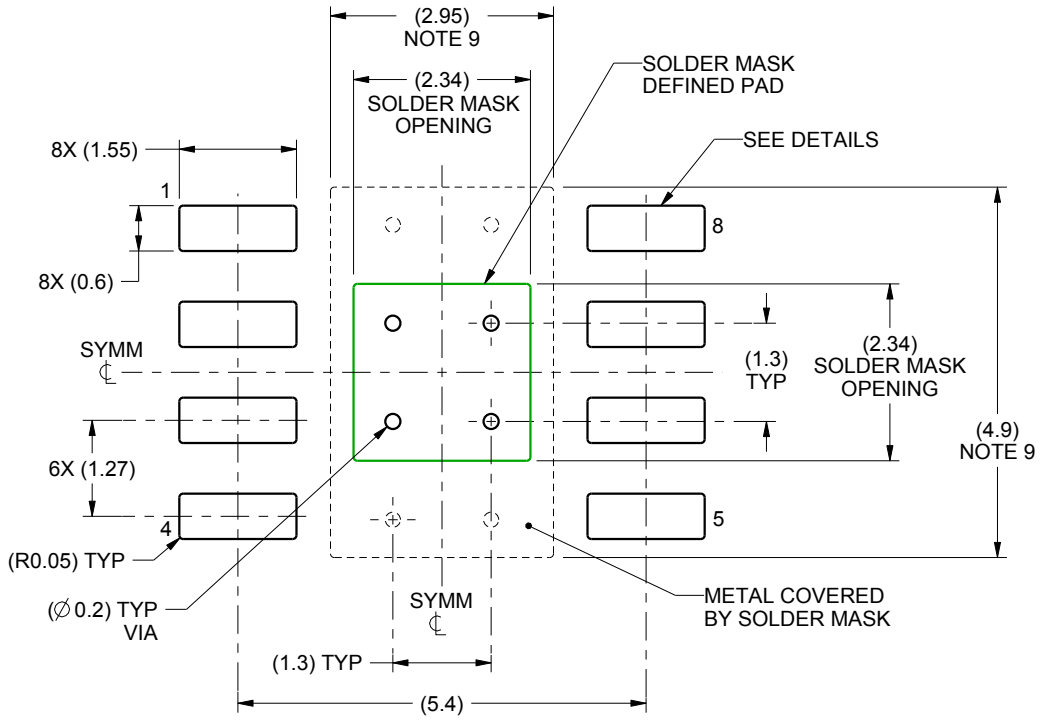
PLASTIC SMALL OUTLINE



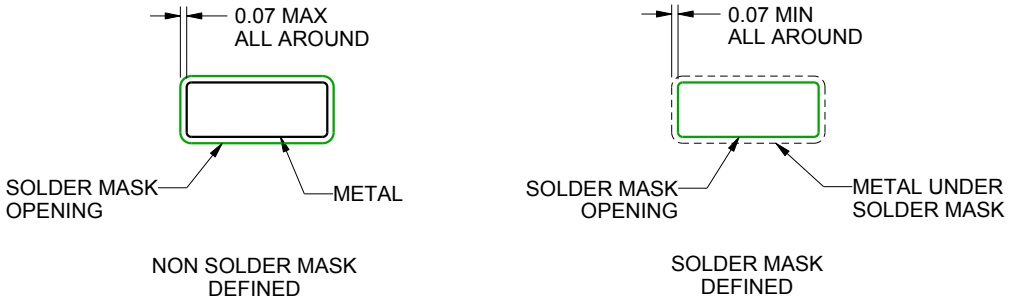
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X

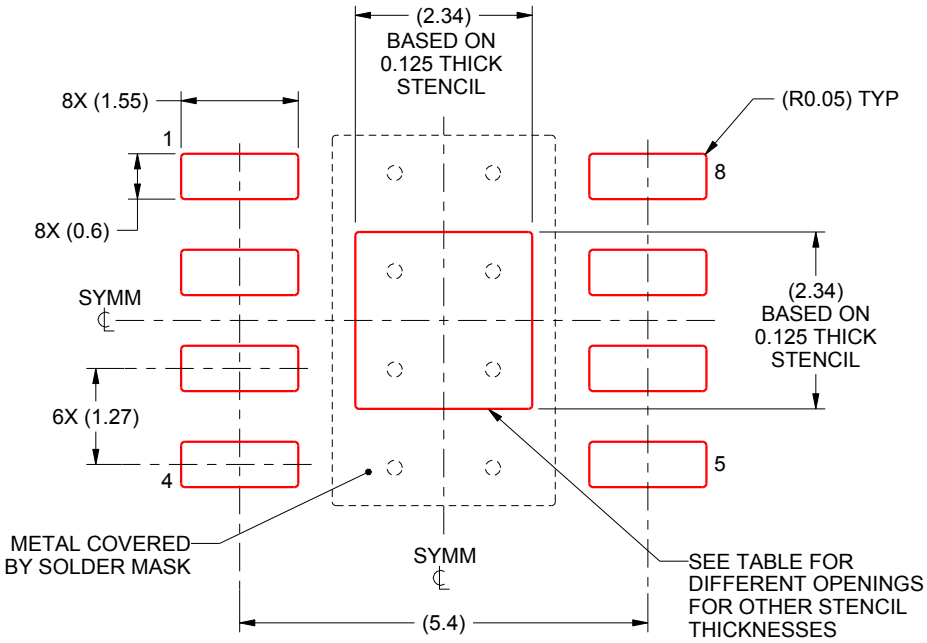


SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



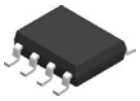
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

4218825/A 05/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

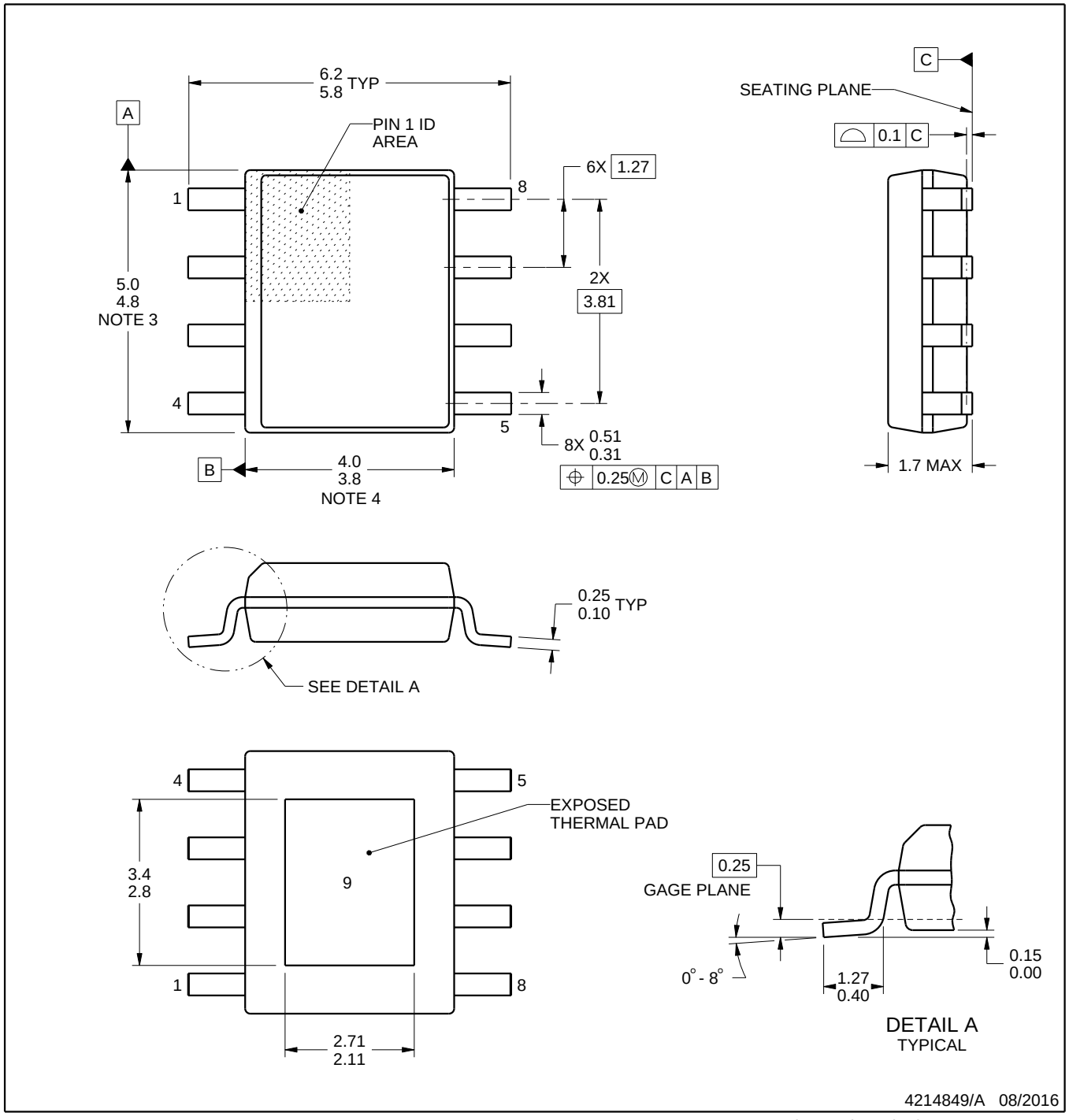


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

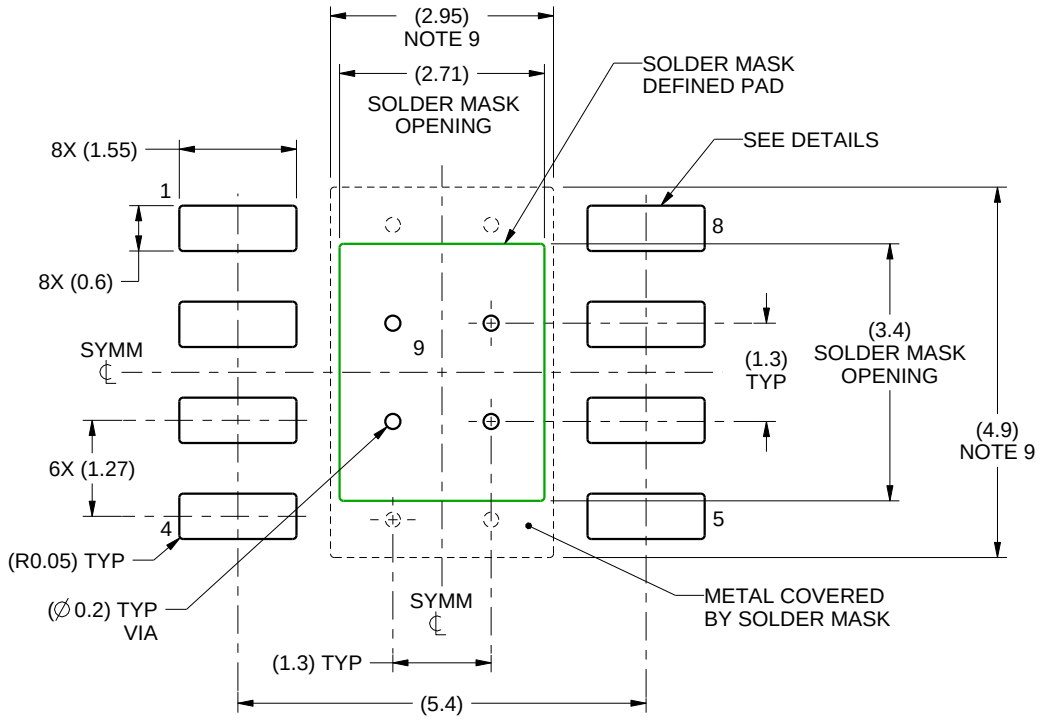
PLASTIC SMALL OUTLINE



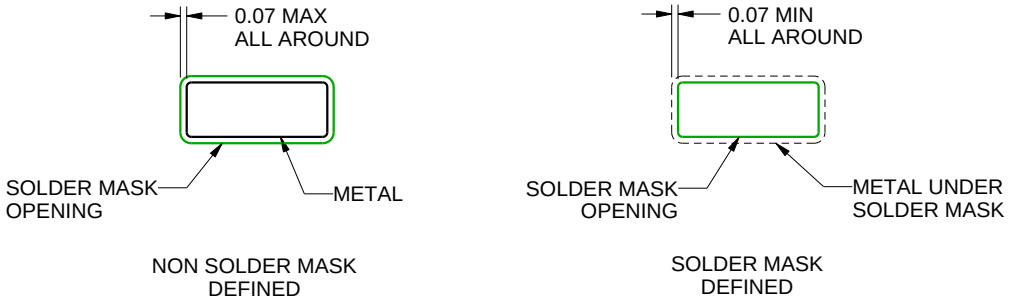
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

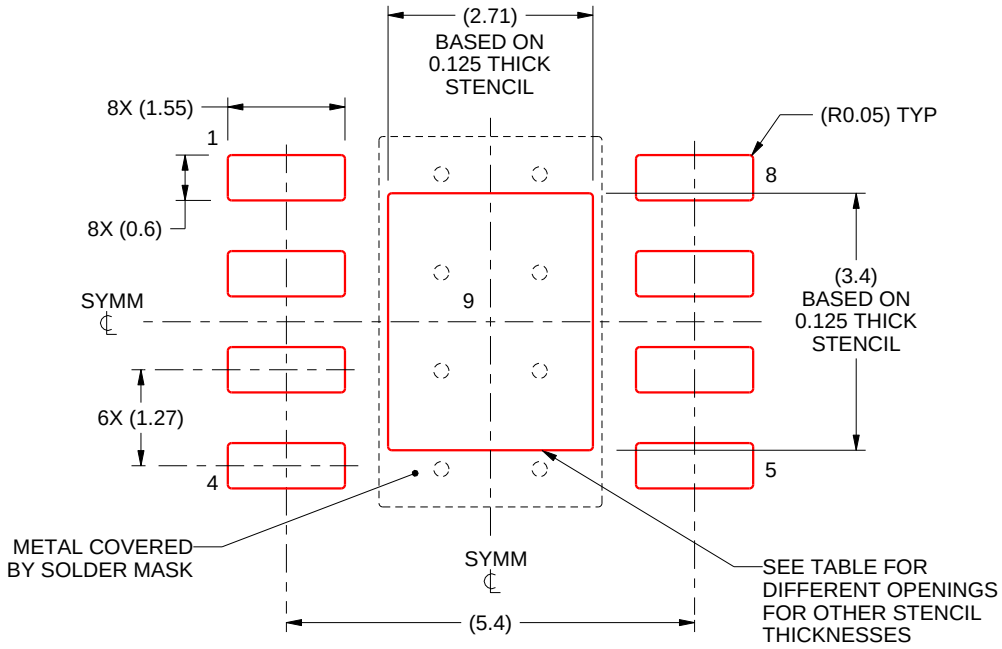
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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