UT54ACS244E

Octal Buffers & Line Drivers

March 2015
www.aeroflex.com/Logic
Datasheet

FEATURES

- Three-state outputs drive bus lines or buffer memory address registers
- 0.6µm CRH CMOS Process
  - Latchup immune
- High speed
- Low power consumption
- Wide power supply operating range of 3.0V to 5.5V
- Available QML Q or V processes
- 20-lead flatpack
- UT54ACS244E - SMD 5962-96570

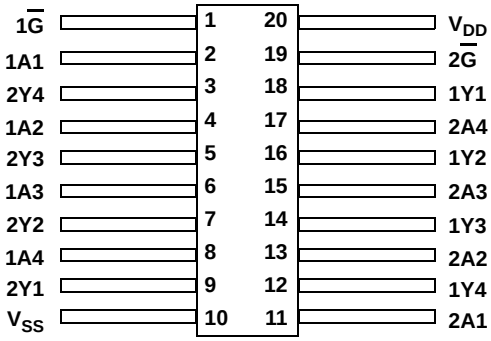
DESCRIPTION

The UT54ACS244E is a performance and voltage enhanced version of the UT54ACS244 non-inverting octal buffers and line drivers which improve the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device is characterized over full military temperature range of -55°C to +125°C.

PINOUT

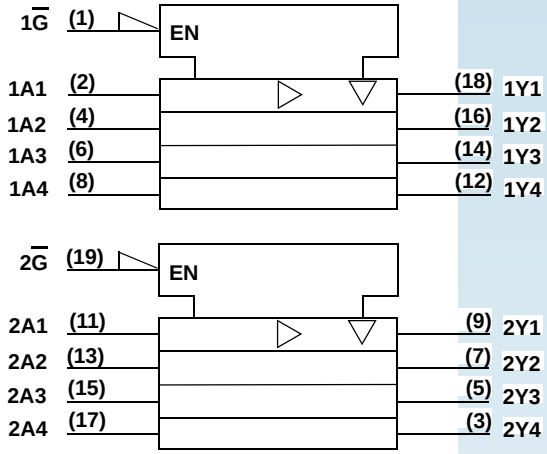
20-Lead Flatpack
Top View



FUNCTION TABLE

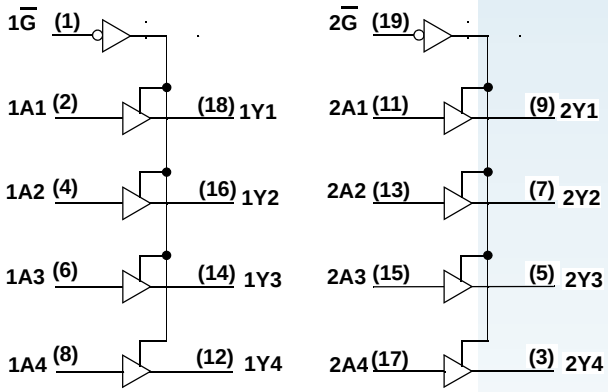
INPUTS		OUTPUT
$\overline{1G}$, $\overline{2G}$	A	Y
L	L	L
L	H	H
H	X	Z

LOGIC SYMBOL



Note:
1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	108	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-0.3 to V_{DD} + 0.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15	°C/W
I_I	DC input current	±10	mA
P_D[2]	Maximum package power dissipation permitted @ Tc = +125°C	3.2	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Per MIL-STD-883, method 1012.1, Section 3.4.1, $P_D = (T_{j(max)} - T_{c(max)}) / \Theta_{jc}$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	°C

DC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS244E[7]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V [6], -55°C < T_C <+125°C);

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage [1]	V_{DD} = 3.0V to 5.5V		$0.3V_{DD}$	V
V_{IH}	High-level input voltage [1]	V_{DD} = 3.0V to 5.5V	$0.7V_{DD}$		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage [3]	I_{OL} = 100µA V_{DD} = 3.0V to 5.5V		0.25	V
V_{OH}	High-level output voltage [3]	I_{OH} = -100µA V_{DD} = 3.0V to 5.5V	V_{DD} - .025		V
I_{OS1}	Short-circuit output current [2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 4.5V to 5.5V	-300	+300	mA
I_{OS2}	Short-circuit output current [2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 3.0V to 3.6V	-150	+150	mA
I_{OL1}	Low level output current [10]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 4.5V to 5.5V	+12		mA
I_{OL2}	Low level output current [10]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 3.0V to 3.6V	+8		mA
I_{OH1}	High level output current [10]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 4.5V to 5.5V	-12		mA
I_{OH2}	High level output current[10]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 3.0V to 3.6V	-8		mA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS}	-30	30	µA
P_{total1}	Power dissipation[2, 8, 9]	C_L=50pF V_{DD} from 4.5V to 5.5V		1.5	mW/ MHz
P_{total2}	Power dissipation[2, 8, 9]	C_L=50pF V_{DD} from 3.0V to 3.6V		0.75	mW/ MHz

I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS} V_{DD} from 3.6V to 5.5V		25	µA
C_{IN}	Input capacitance [5]	*f* = 1MHz V_{DD} = 0V		15	pF
C_{OUT}	Output capacitance [5]	*f* = 1MHz V_{DD} = 0V		15	pF

Notes:
1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. Guaranteed by characterization, but not tested.

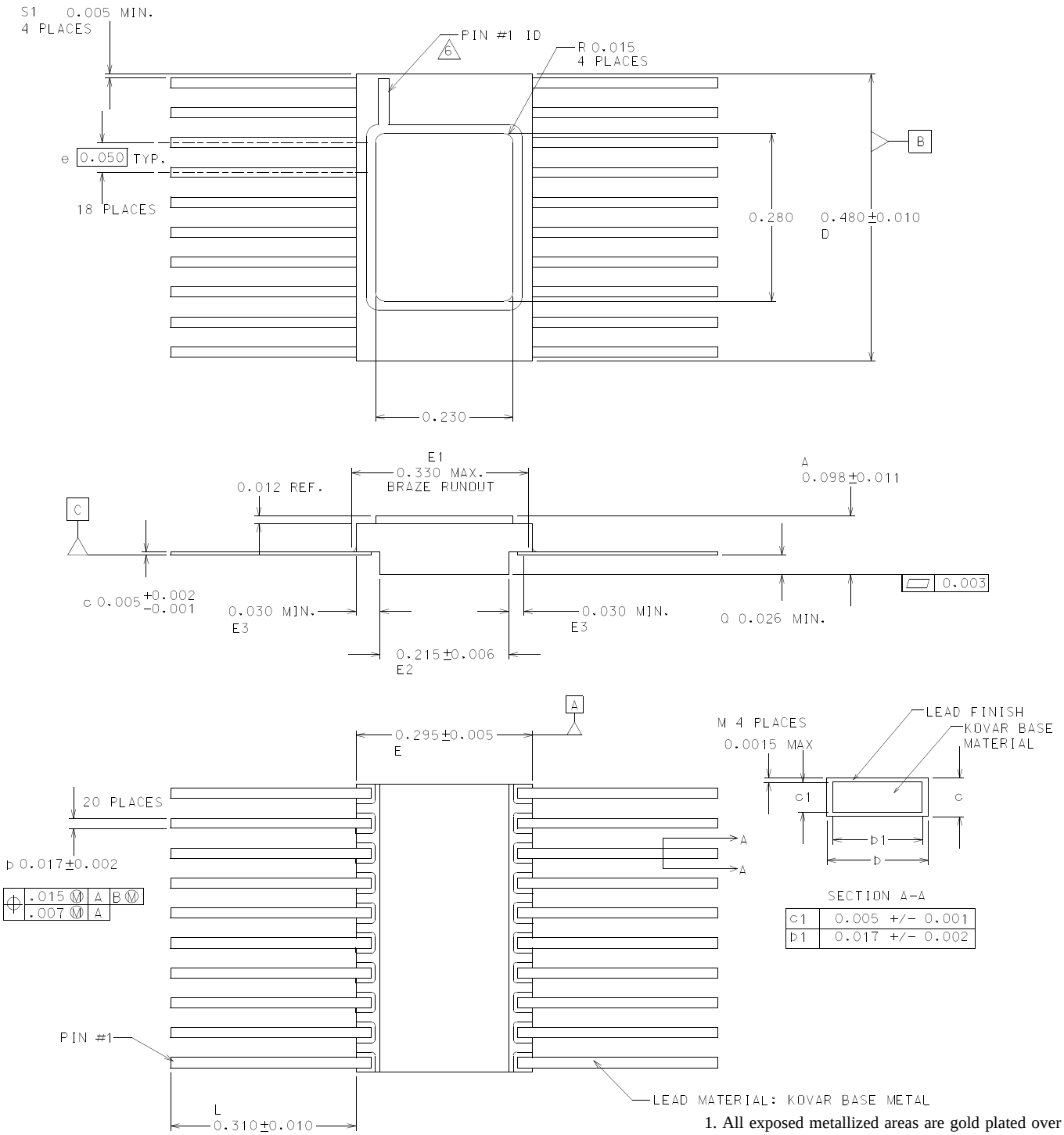
AC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS244E[2]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V [1], -55°C < T_C < +125°C);

SYMBOL	PARAMETER	Condition	V_{DD}	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Input to Yn	CL = 50pF	4.5V to 5.5V	1	6.5	ns
			3.0V to 3.6V	1	9.5	
t_{PHL}	Input to Yn	CL = 50pF	4.5V to 5.5V	1	7.5	ns
			3.0V to 3.6V	1	10.5	
t_{PZL}	$\overline{G}$ low to Yn active	CL = 50pF	4.5V to 5.5V	1	6	ns
			3.0V to 3.6V	1	8	
t_{PZH}	$\overline{G}$ low to Yn active	CL = 50pF	4.5V to 5.5V	1	7	ns
			3.0V to 3.6V	1	9.5	
t_{PLZ}	$\overline{G}$ high to Yn three-state	CL = 50pF	4.5V to 5.5V	1	6	ns
			3.0V to 3.6V	1	7.5	
t_{PHZ}	$\overline{G}$ high to Yn three-state	CL = 50pF	4.5V to 5.5V	1	9.5	ns
			3.0V to 3.6V	1	11	

Notes:
1. Maximum allowable relative shift equals 50mV.
2. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.

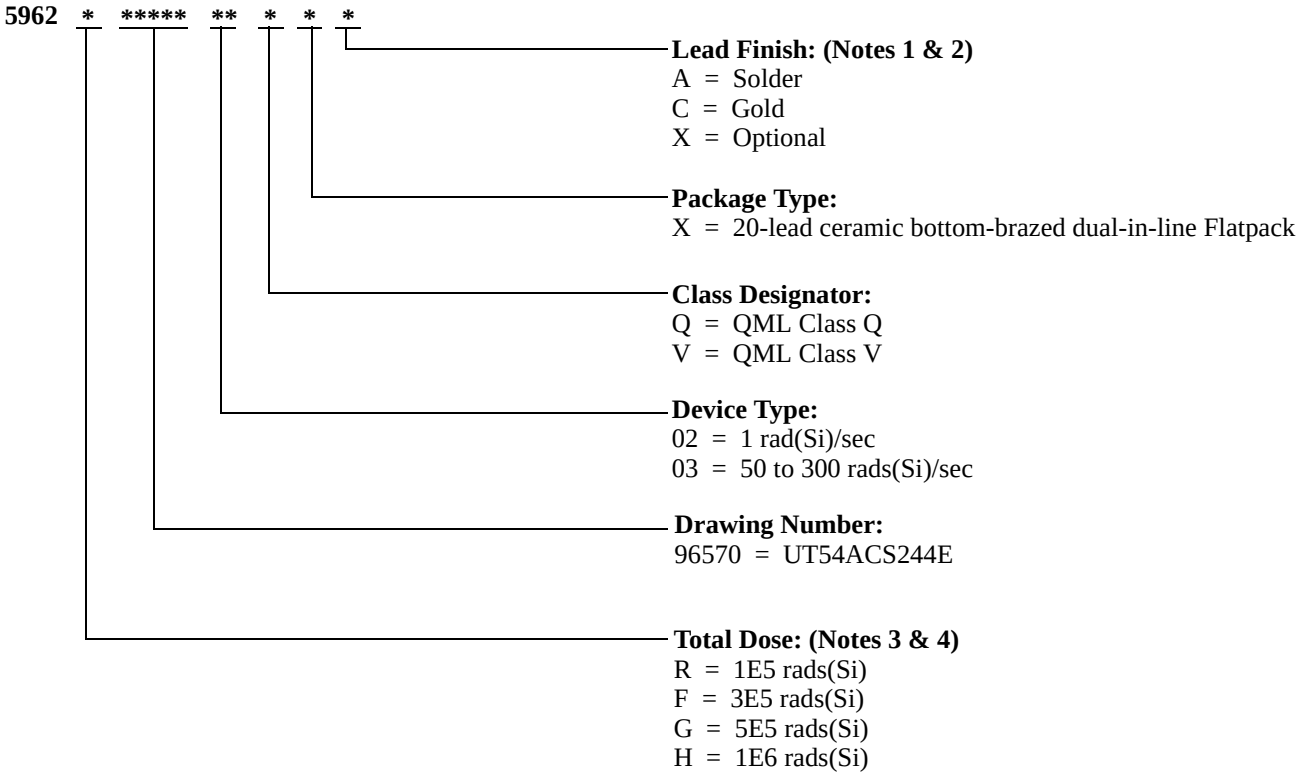
Packaging



1. All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbol is in accordance with MIL-PRF-38533.
5. Lead position and colanarity are not measured.

Figure 1. 20-lead Flatpack

Ordering Information: UT54ACS244E: SMD



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

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Datasheet Revision History

Revision Date	Description of Change
March 2015 Version 1.0.0	**Initial Release of Datasheet**