IXYS

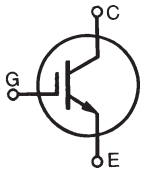
Advance Technical Information

High Voltage IGBT

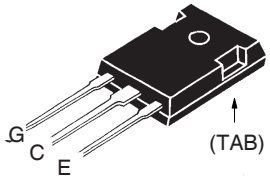
IXGH10N300

V_{CES} = 3000V
I_{C90} = 10A
$V_{CE(sat)}$ ≤ 3.5V

For Capacitor Discharge Applications



TO-247 AD



G = Gate C = Collector
E = Emitter TAB = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	3000	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	3000	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	18	A
I_{C90}	T_C = 90°C	10	A
I_{CM}	T_C = 25°C, 1ms	40	A
SSOA	V_{GE} = 20V, T_{VJ} = 125°C, R_G = 50Ω	I_{CM} = 32	A
(RBSOA)	Clamped Inductive Load	@ ≤ 1250	V
P_C	T_C = 25°C	100	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M_d	Mounting Torque	1.13/10	Nm/lb.in.
Weight		6	g

Features

- High Peak Current Capability
- Low Saturation Voltage
- Low Gate Drive Requirement
- Molding Epoxies Meet UL 94 V-0 Flammability Classification

Applications

- Capacitor Discharge
- Pulser Circuits

Advantages

- High Power Density
- Easy to Mount

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	3000			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			25	μA
	T_J = 125°C			500	μA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 10A, V_{GE} = 15V			3.5	V
	I_C = 30A			5.2	V

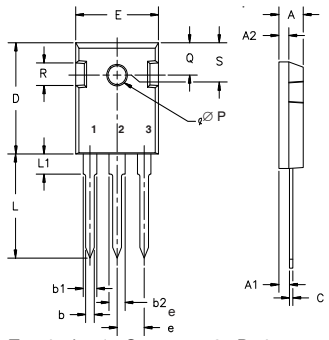
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Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 20A, V_{CE} = 10V, Note 1	3.6	6.0	S
$I_{C(ON)}$	V_{GE} = 15V, V_{CE} = 15V, Note 1		54	A
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		560	pF
C_{oes}			24	pF
C_{res}			8	pF
$Q_{g(on)}$	I_C = 10A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		32.0	nC
Q_{ge}			7.5	nC
Q_{gc}			12.0	nC
$t_{d(on)}$	**Resistive Switching Times**		72	ns
t_r	I_C = 20A, V_{GE} = 15V		227	ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 50Ω		154	ns
t_f			530	ns
R_{thJC}				1.25 °C/W
R_{thCK}			0.21	°C/W

Note

1. Pulse Test, t ≤ 300μs; Duty Cycle, d ≤ 2%.
2. Additional provisions for lead-to-lead voltage isolation are required at V_{CE} > 1200V.

TO-247 (IXGH) Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ 25ºC

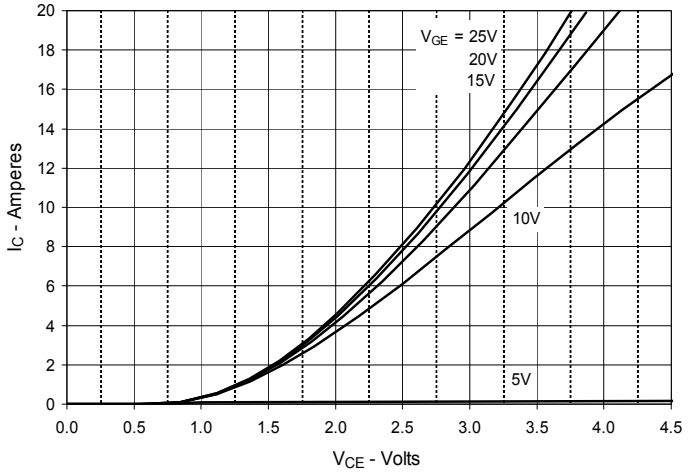


Fig. 2. Extended Output Characteristics @ 25ºC

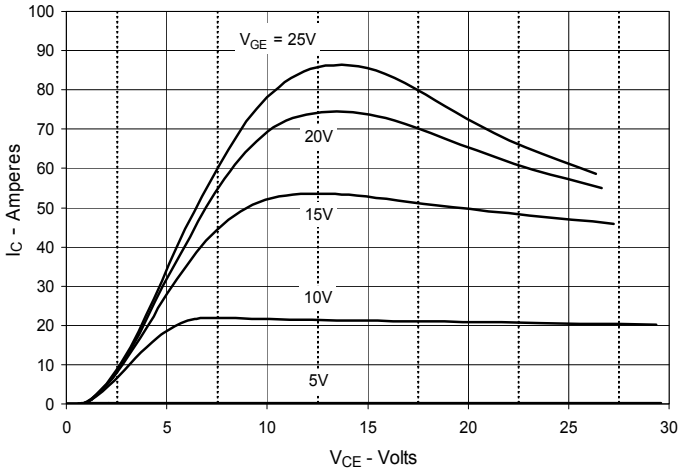


Fig. 3. Output Characteristics @ 125ºC

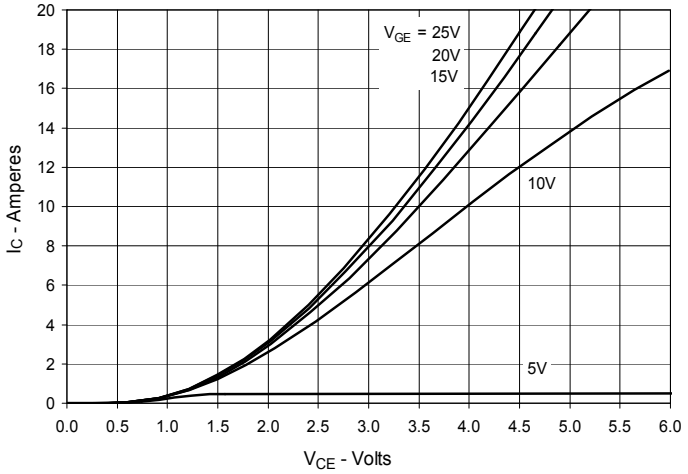


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

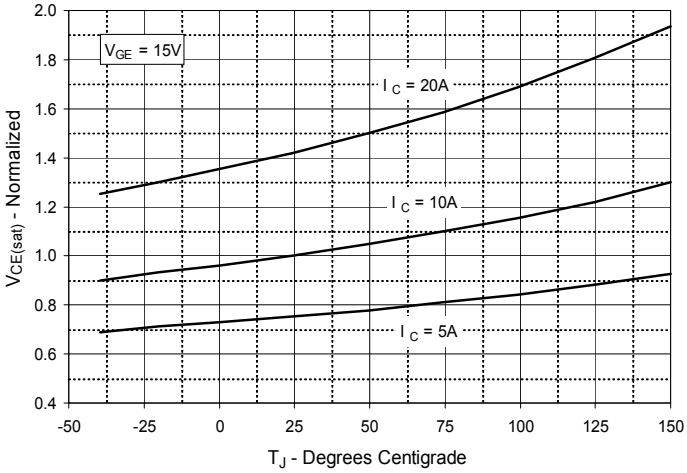


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

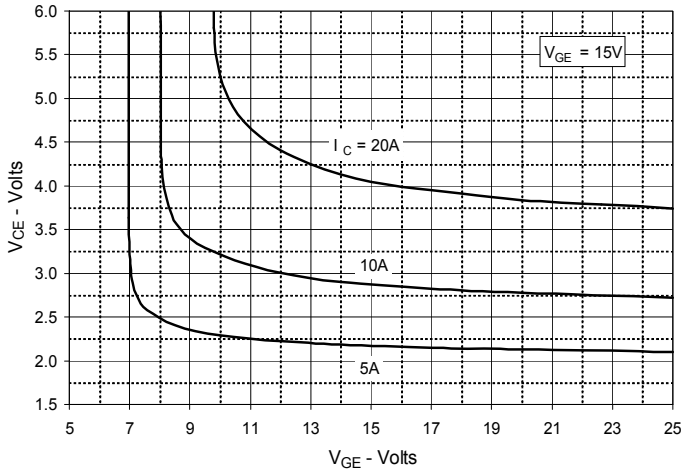
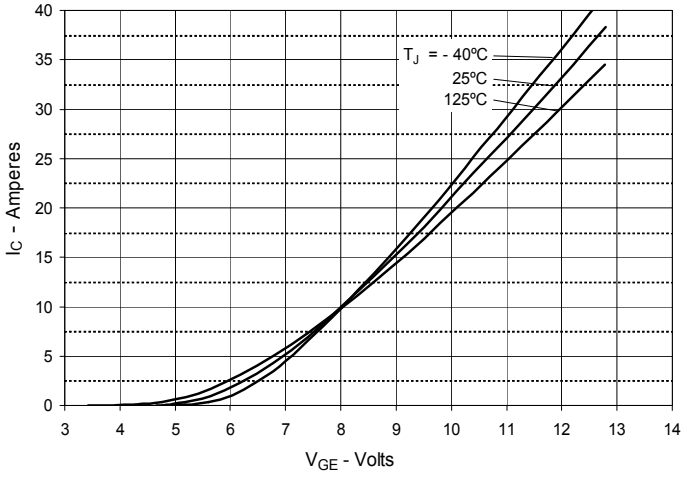


Fig. 6. Input Admittance



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Fig. 7. Transconductance

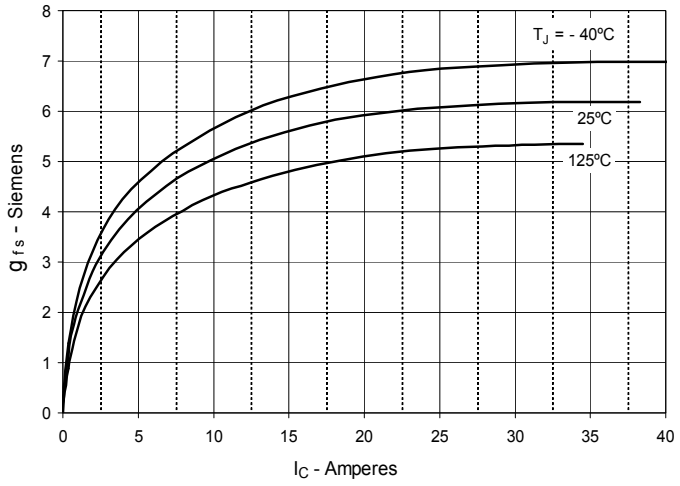


Fig. 8. Gate Charge

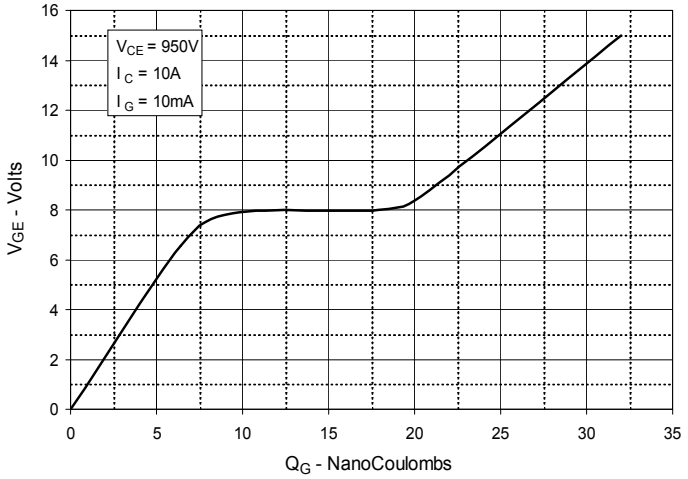


Fig. 9. Reverse-Bias Safe Operating Area

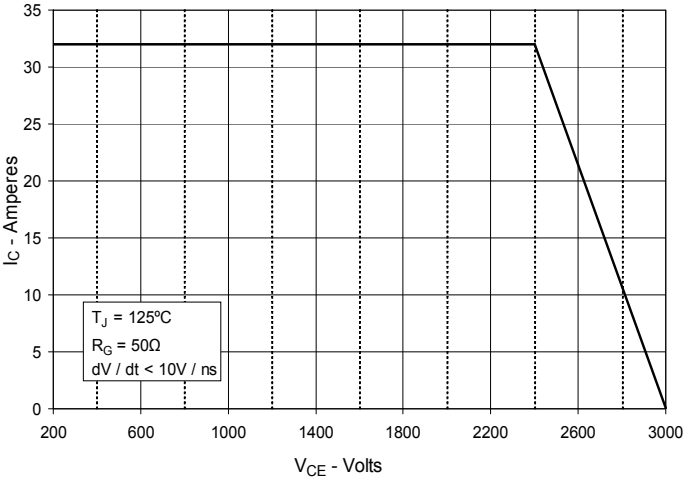


Fig. 10. Capacitance

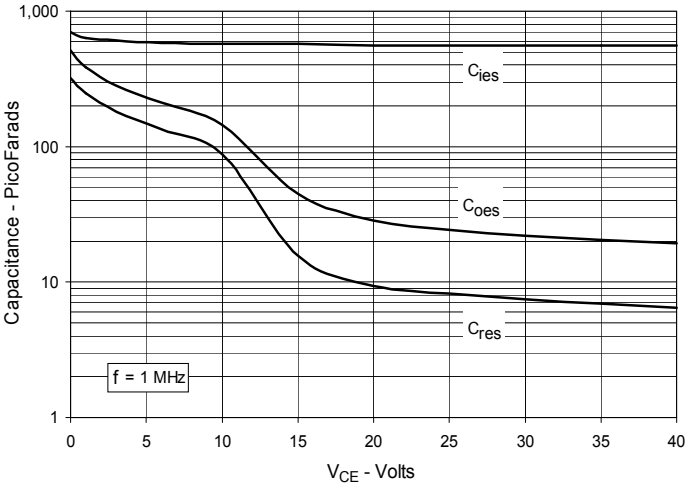
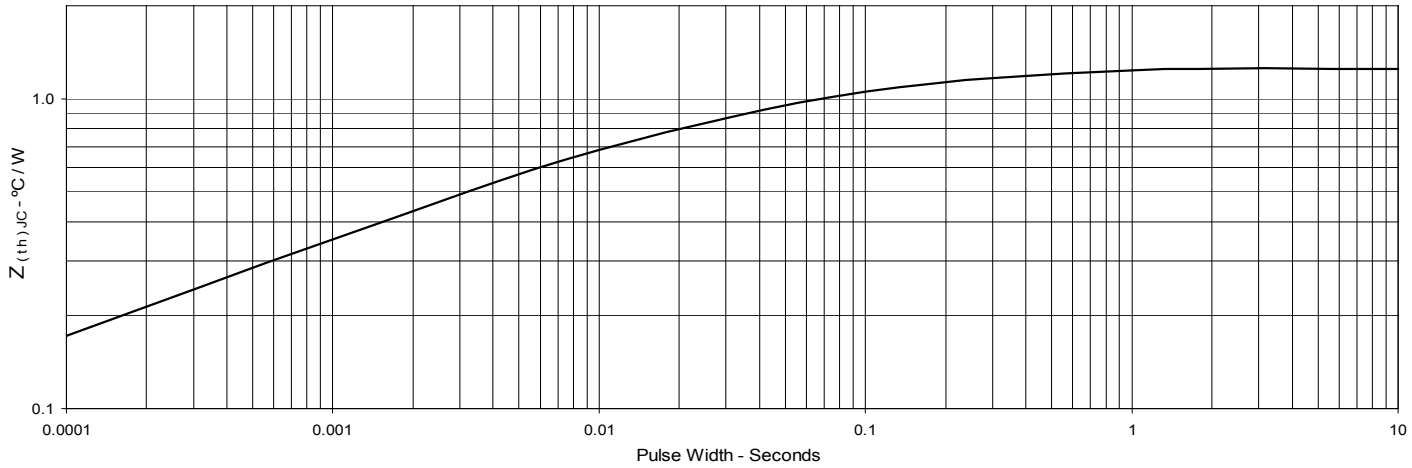


Fig. 11. Maximum Transient Thermal Impedance



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

Fig. 12. Resistive Turn-on Rise Time vs. Junction Temperature

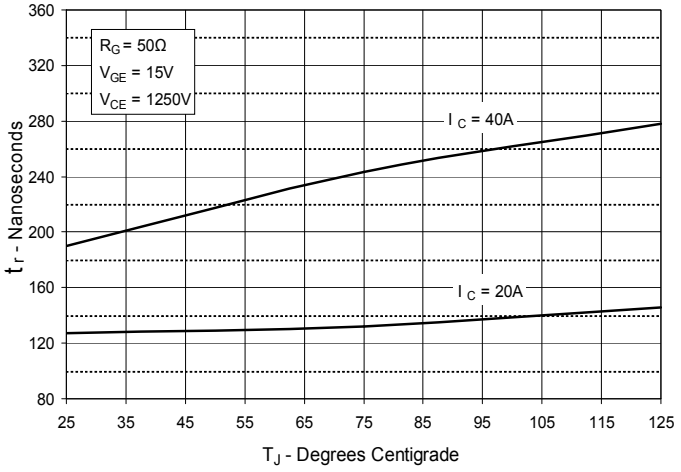


Fig. 13. Resistive Turn-on Rise Time vs. Collector Current

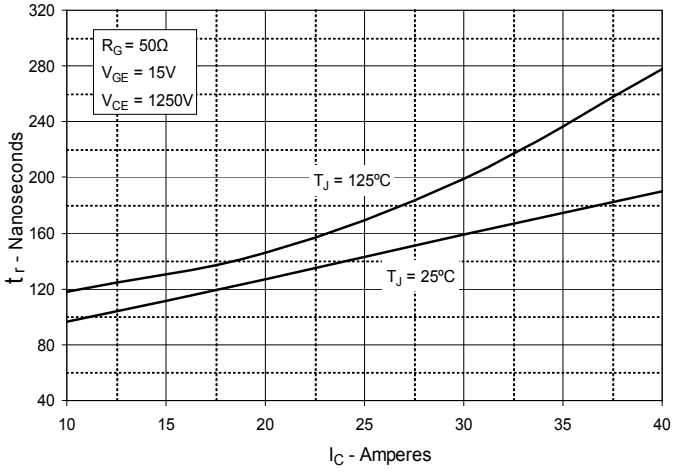


Fig. 14. Resistive Turn-on Switching Times vs. Gate Resistance

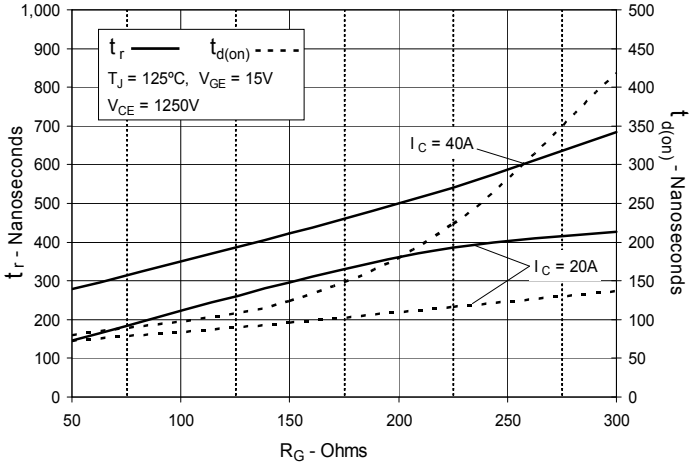


Fig. 15. Resistive Turn-off Switching Times vs. Junction Temperature

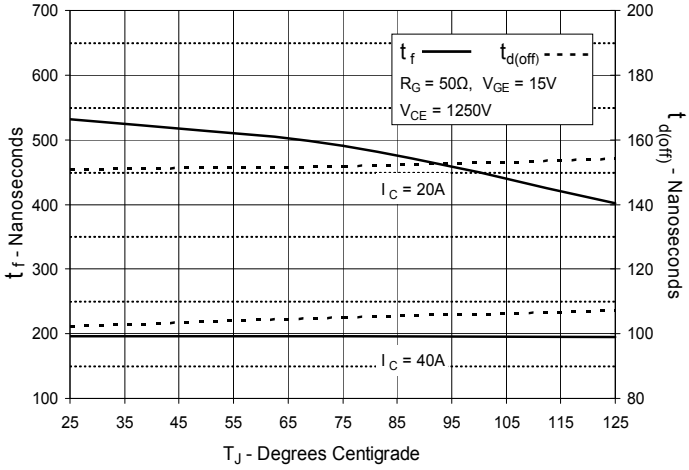


Fig. 16. Resistive Turn-off Switching Times vs. Collector Current

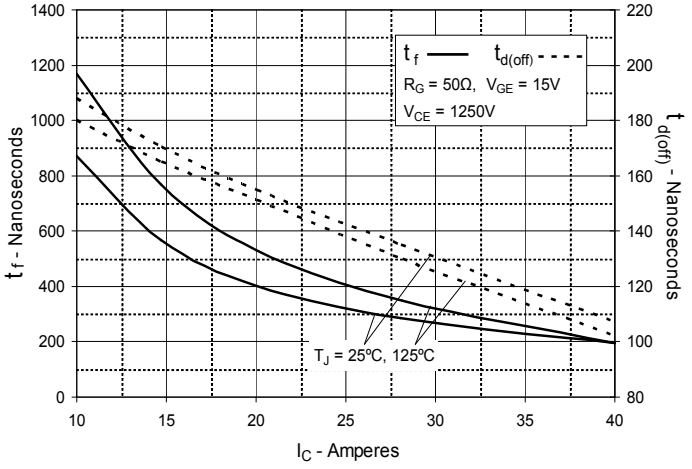
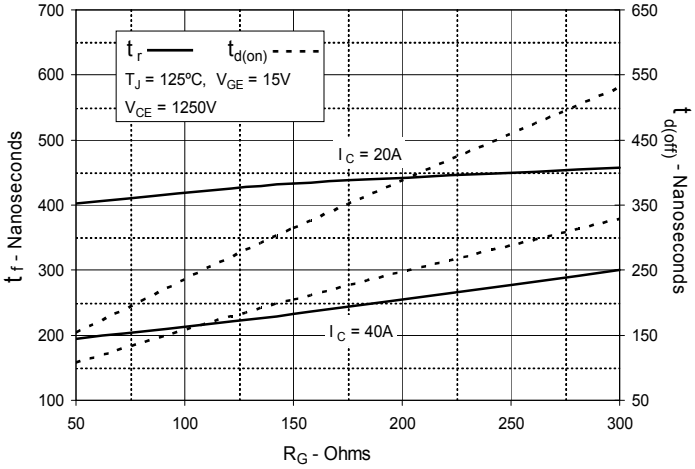


Fig. 17. Resistive Turn-off Switching Times vs. Gate Resistance



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