International
IOR Rectifier

PD-91715C

# IRFE230
# JANTX2N6798U
# JANTXV2N6798U

## REPETITIVE AVALANCHE AND dv/dt RATED HEXFET® TRANSISTORS SURFACE MOUNT (LCC-18)

## REF:MIL-PRF-19500/557
## 200V, N-CHANNEL

### Product Summary

| Part Number | $BV_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| IRFE230 | 200V | 0.40Ω | 5.5A |




LCC-18

The leadless chip carrier (LCC) package represents the logical next step in the continual evolution of surface mount technology. Desinged to be a close replacement for the TO-39 package, the LCC will give designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the LCC package to meet the specific needs of the power market by increasing the size of the bottom source pad, thereby enhancing the thermal and electrical performance. The lid of the package is grounded to the source to reduce RF interference.

### Features:

- Surface Mount
- Small Footprint
- Alternative to TO-39 Package
- Hermetically Sealed
- Dynamic dv/dt Rating
- Avalanche Energy Rating
- Simple Drive Requirements
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

### Absolute Maximum Ratings

| | Parameter | | Units |
|---|---|---|---|
| $I_D$ @ $V_{GS}$ = 10V, $T_C$ = 25°C | Continuous Drain Current | 5.5 | A |
| $I_D$ @ $V_{GS}$ = 10V, $T_C$ = 100°C | Continuous Drain Current | 3.5 | |
| $I_{DM}$ | Pulsed Drain Current ① | 22 | |
| $P_D$ @ $T_C$ = 25°C | Max. Power Dissipation | 25 | W |
| | Linear Derating Factor | 0.20 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 110 | mJ |
| $I_{AR}$ | Avalanche Current ① | 5.5 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 2.5 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 6.3 | V/ns |
| $T_J$ | Operating Junction | -55 to 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | |
| | Pckg. Mounting Surface Temp. | 300 (for 5 S) | |
| | Weight | 0.42 (typical) | g |

For footnotes refer to the last page

## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 200 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $\Delta BV_{DSS}/\Delta T_J$ | Temperature Coefficient of Breakdown Voltage | — | 0.27 | — | V/°C | Reference to 25°C, $I_D$ = 1.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance | — | — | 0.40 | Ω | $V_{GS}$ = 10V, $I_D$ = 3.5A ④ |
| | | — | — | 0.46 | | $V_{GS}$ = 10V, $I_D$ = 5.5A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $g_{fs}$ | Forward Transconductance | 3.4 | — | — | S | $V_{DS}$ = 15V, $I_{DS}$ = 3.5A ④ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | — | 25 | µA | $V_{DS}$ = 160V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ =160V<br>$V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | — | 100 | nA | $V_{GS}$ = 20V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | — | — | -100 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | — | — | 42 | nC | $V_{GS}$ = 10V, $I_D$ = 5.5A,<br>$V_{DS}$ =100V |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 5.3 | | |
| $Q_{gd}$ | Gate-to-Drain ('Miller') Charge | — | — | 28 | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | — | 30 | ns | $V_{DD}$ = 100V, $I_D$ = 5.5A,<br>$V_{GS}$ = 10V, $R_G$ = 7.5Ω |
| $t_r$ | Rise Time | — | — | 50 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | — | 50 | | |
| $t_f$ | Fall Time | — | — | 40 | | |
| $L_S + L_D$ | Total Inductance | — | 6.1 | — | nH | Measured from the center of drain pad to center of source pad |
| $C_{iss}$ | Input Capacitance | — | 740 | | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V<br>f = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 240 | — | | |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 74 | — | | |

## Source-Drain Diode Ratings and Characteristics

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 5.5 | A | |
| $I_{SM}$ | Pulse Source Current (Body Diode) ① | — | — | 22 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.4 | V | $T_j$ = 25°C, $I_S$ = 5.5A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | — | 500 | ns | $T_j$ = 25°C, $I_F$ = 5.5A, di/dt ≤ 100A/µs |
| $Q_{RR}$ | Reverse Recovery Charge | — | — | 6.0 | µC | $V_{DD}$ ≤ 50V ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S$ + $L_D$. | | | | |

## Thermal Resistance

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{thJC}$ | Junction to Case | — | — | 5.0 | °C/W | |
| $R_{thJ\text{-}PCB}$ | Junction to PC Board | — | — | 19 | | Soldered to a copper clad PC board |

**Note: Corresponding Spice and Saber models are available on International Rectifier website.**

For footnotes refer to the last page

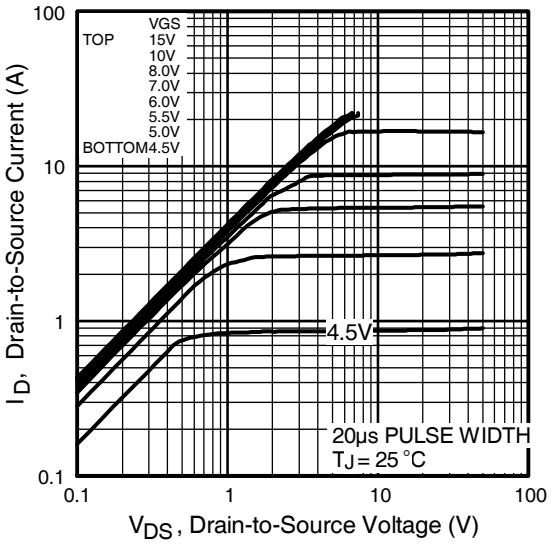



**Fig 1.** Typical Output Characteristics

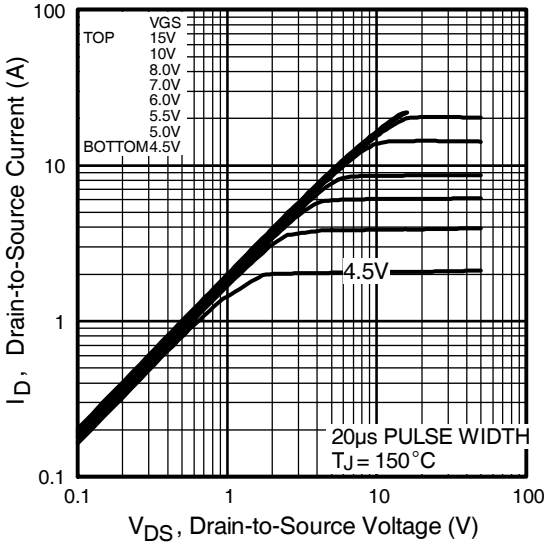



**Fig 2.** Typical Output Characteristics

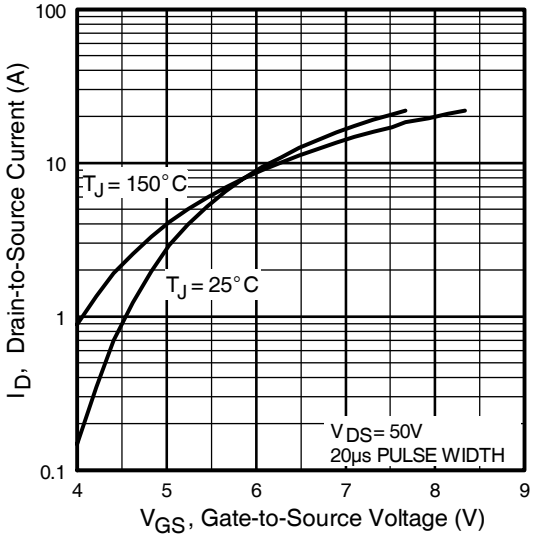



**Fig 3.** Typical Transfer Characteristics

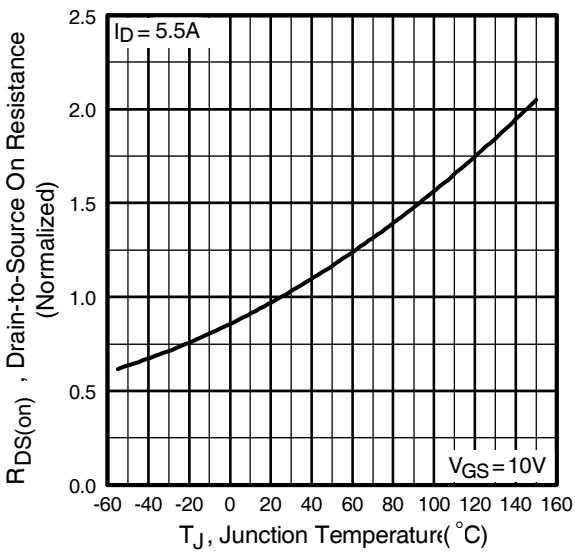



**Fig 4.** Normalized On-Resistance
Vs. Temperature

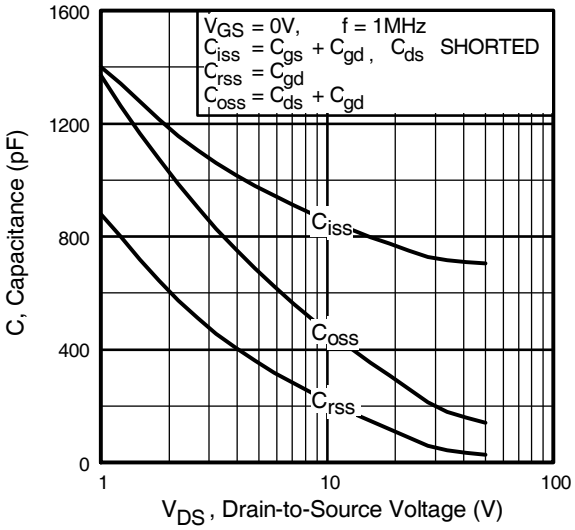



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

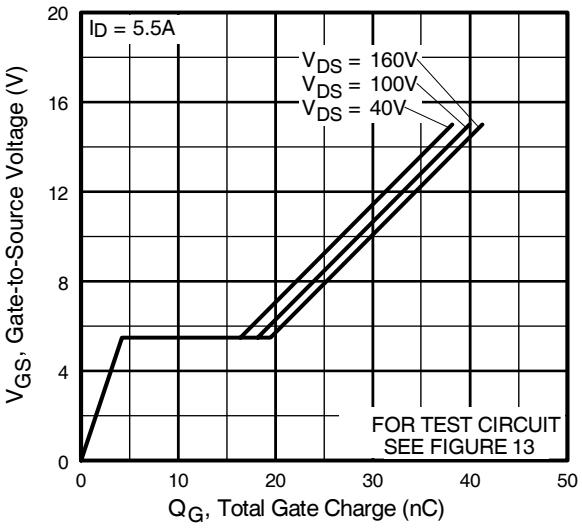



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

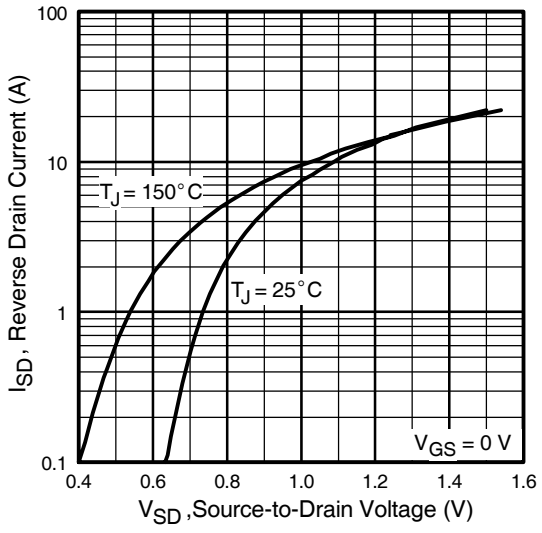



**Fig 7.** Typical Source-Drain Diode Forward Voltage

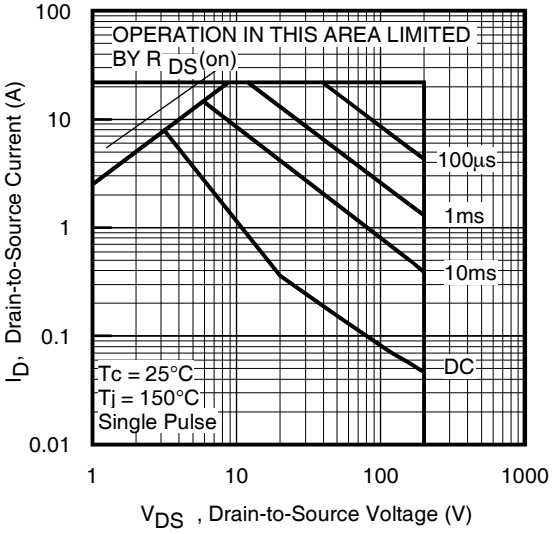



**Fig 8.** Maximum Safe Operating Area

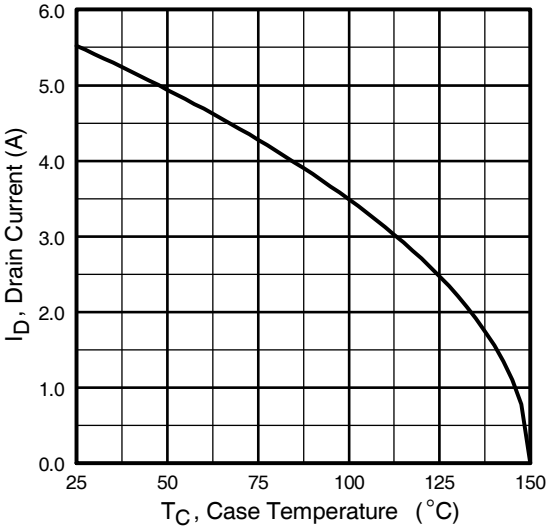



**Fig 9.** Maximum Drain Current Vs. Case Temperature

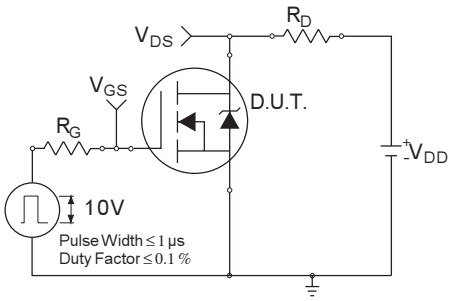



**Fig 10a.** Switching Time Test Circuit

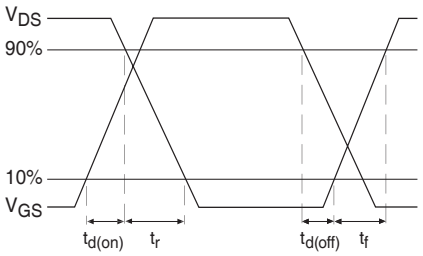



**Fig 10b.** Switching Time Waveforms

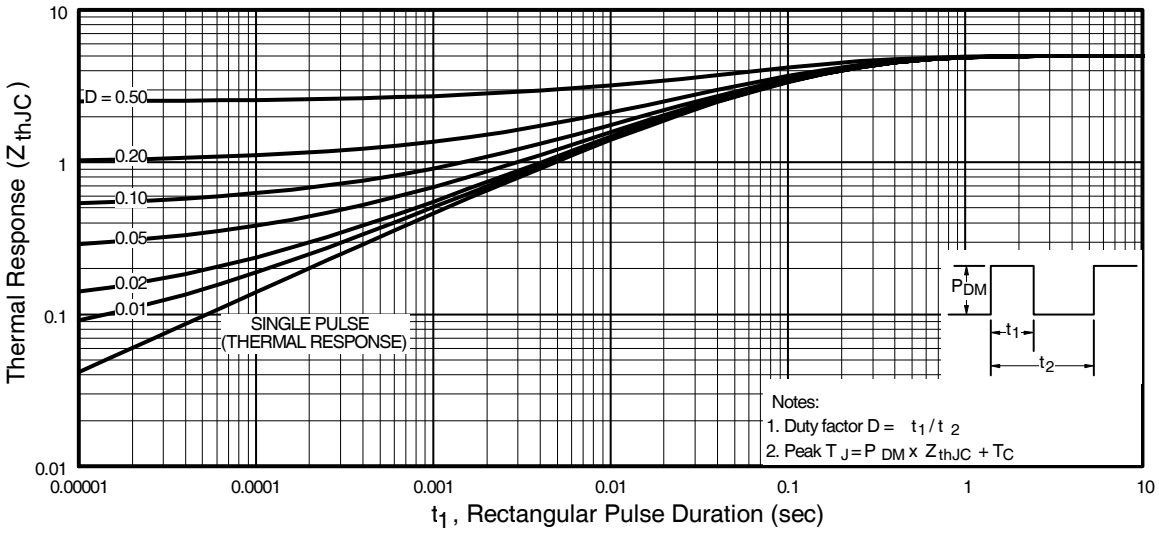



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

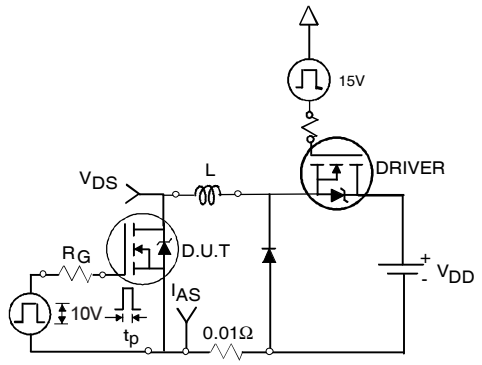



**Fig 12a.** Unclamped Inductive Test Circuit

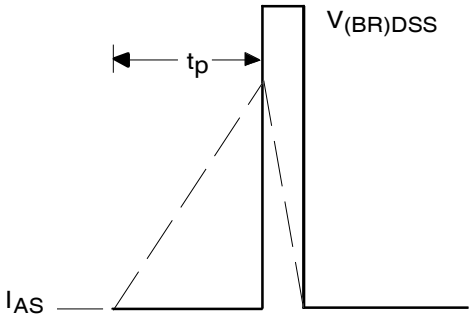



**Fig 12b.** Unclamped Inductive Waveforms

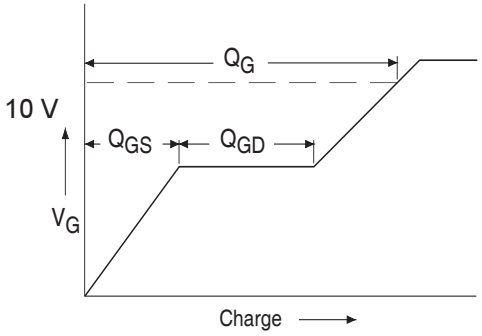



**Fig 13a.** Basic Gate Charge Waveform

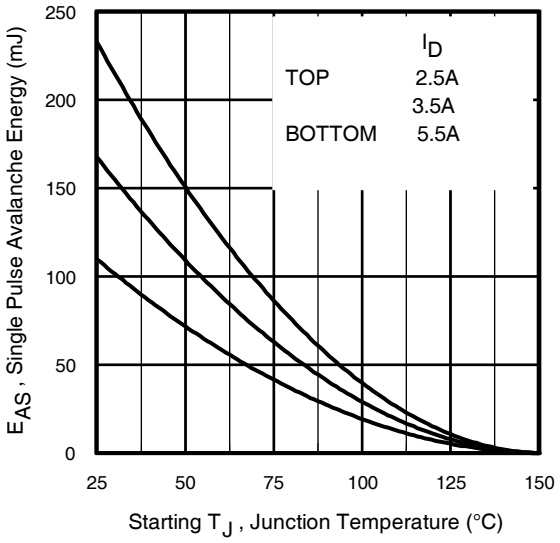



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

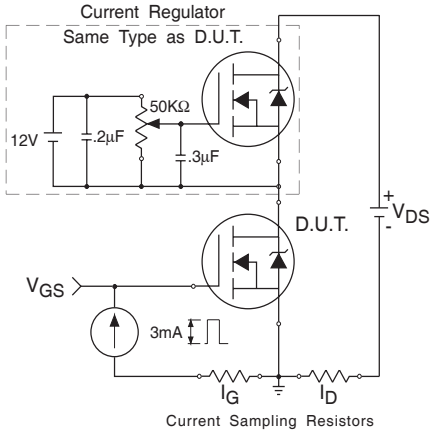



**Fig 13b.** Gate Charge Test Circuit

## Footnotes:

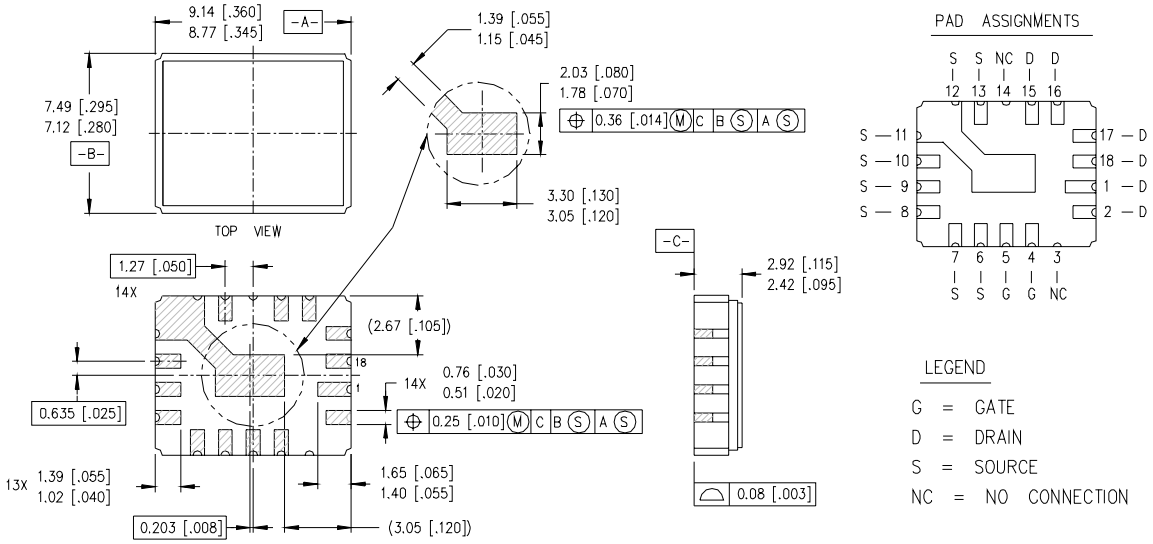
① Repetitive Rating; Pulse width limited by maximum junction temperature.

② $V_{DD}$ = 50V, Starting $T_J$ = 25°C, L= 7.3mH Peak $I_{AS}$ = 5.5A, $V_{GS}$ =10V, $R_G$= 25Ω

③ $I_{SD} \leq$ 5.5A, di/dt ≤99A/μs, $V_{DD} \leq$ 200V, $T_J \leq$ 150°C, Suggested RG =7.5 Ω

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

## Case Outline and Dimensions — LCC-18




NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

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*Data and specifications subject to change without notice. 01/2015*