Features

- Transient protection for gigabit ethernet lines-to-lines
- Provide transient protection for the protected differential line pair to
  IEC 61000-4-2 (ESD) ±30kV (air/contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 45A (8/20μs)
- DFN3020P10E package
- Specific pin out for easy board layout
- Fast turn-on and low clamping voltage
- Low capacitance for high speed interfaces
- For low operating voltage applications: 2.5V
- Low leakage current
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- WAN/LAN device
- 10/100/1000 ethernet
- Switching systems
- Computers
- Instruments

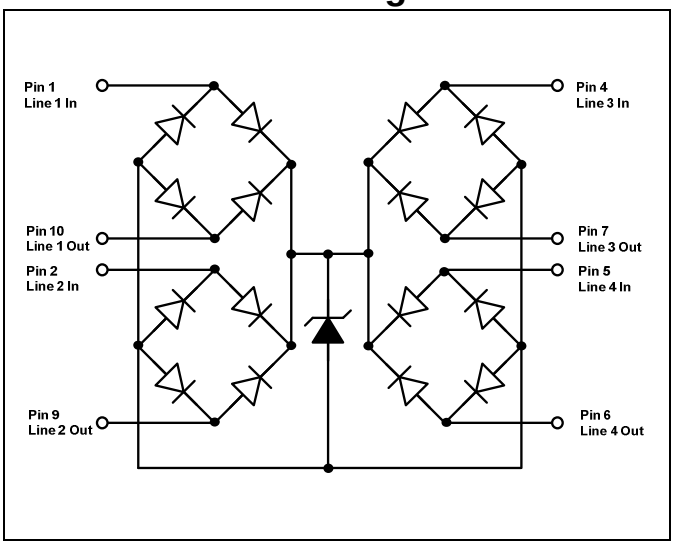
Description

AZ3225-08F is a design which includes surge rated diode arrays to protect high speed data interfaces in an electronic system. The AZ3225-08F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

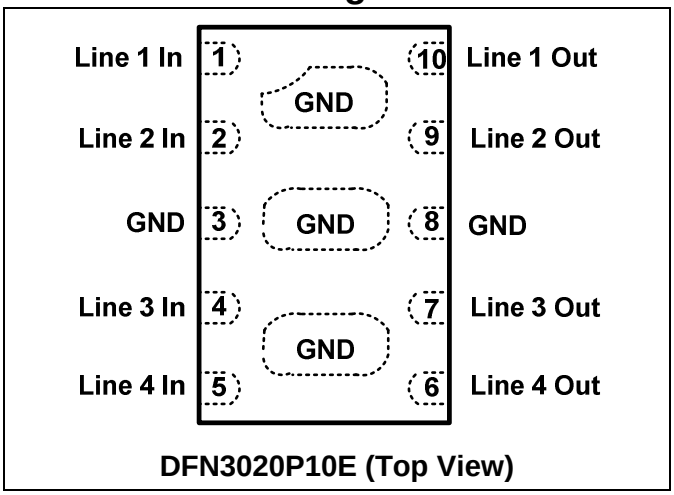
AZ3225-08F is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the signal lines, protecting any downstream components.

AZ3225-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN3020P10E (Top View)

Specifications

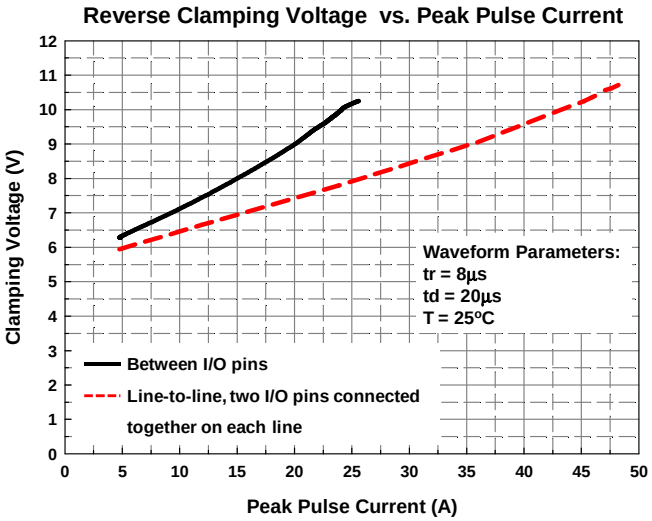
Absolute Maximum Ratings (T_A= 25°C, unless otherwise specified)			
Parameter	**Symbol**	**Rating**	**Unit**
Peak Pulse Current (t_p =8/20μs) (Note 1)	I_{PP}	45	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

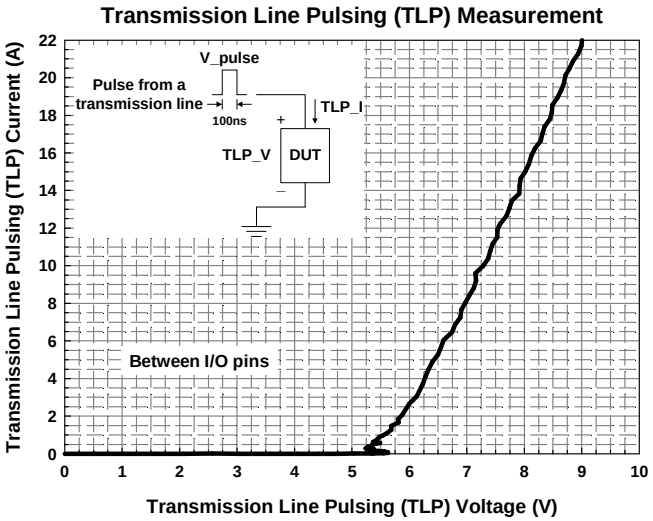
Electrical Characteristics						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Reverse Stand-Off Voltage	V_{RWM}	Between I/O pins, T=25 °C.			2.5	V
Channel Leakage Current	I_{Leak}	V_{RWM} = 2.5V, T=25 °C, between I/O pins.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, between I/O pins.	3		7	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP}=5A, t_p=8/20μs, T=25 °C, between I/O pins.			7	V
		I_{PP}=25A, t_p=8/20μs, T=25 °C, between I/O pins.			11.5	V
		I_{PP}=45A, t_p=8/20μs, T=25 °C, line-to-line, two I/O pins connected together on each line (Note 1).			11.5	V
ESD Clamping Voltage (Note 2)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, contact mode, between I/O pins.		8		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, T=25 °C, contact mode, between I/O pins.		0.18		Ω
Channel Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1MHz, T=25 °C, between I/O pins.		1.2	1.5	pF

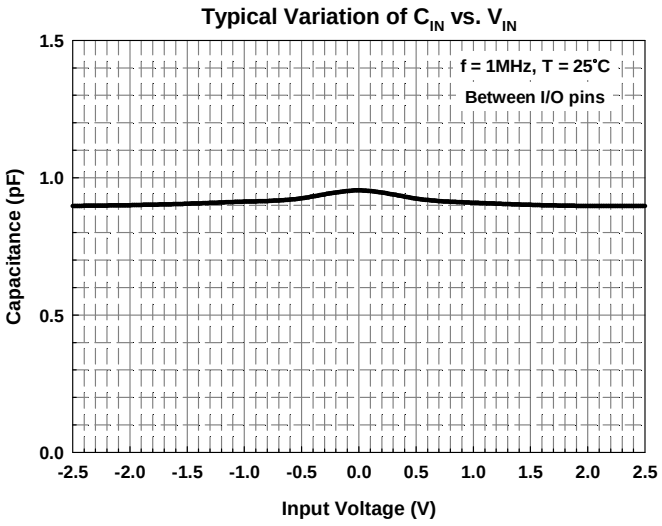
Note 1: Ratings with two pins connected together per the recommended configuration (i.e. pin-1 connected to pin-10, pin-2 connected to pin-9, pin-4 connected to pin-7, and pin-5 connected to pin-6).

Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics







Applications Information

The AZ3225-08F is designed to protect four high speed data lines operating at 2.5 volts to against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The AZ3225-08F designed with a flow through pin configuration is shown in Fig. 1. Fig. 2 shows a typical PCB layout example with AZ3225-08F for ESD/EFT/Lightning protection. In the Gigabit Ethernet application, pin-1, -2, -4, and pin-5 should be connected to pin-10, -9, -7, and pin-6 respectively. The traces should be unbroken and run under the device as shown. To get minimum parasitic inductance, the path length should keep as short as possible. Pin-3, -8 and the three center tabs are electrically connected, which should be left floating (i.e. not connected to ground) in the Ethernet application. Fig. 3 shows a typical Gigabit Ethernet protection circuit with AZ3225-08F.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ3225-08F.
- Place the AZ3225-08F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path should be kept as short as possible.
- NEVER route critical signals near board edges and near the lines which the ESD transience easily injects to.

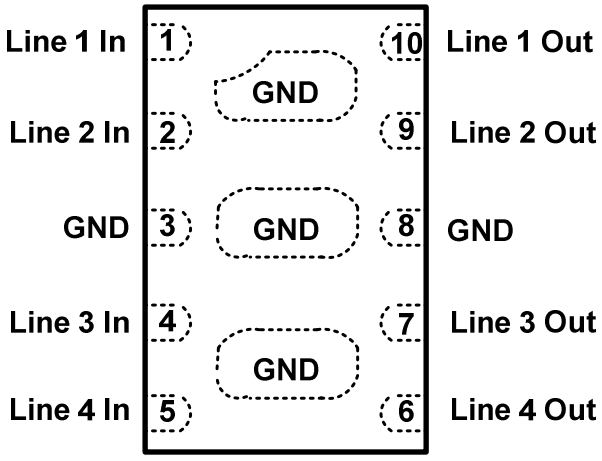


Fig. 1 Pin configuration of AZ3225-08F.

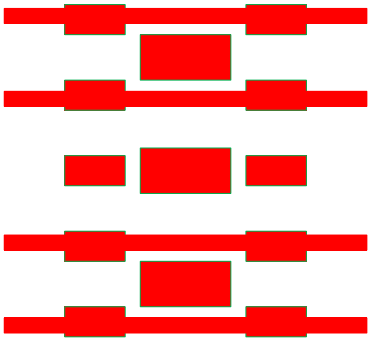


Fig. 2 Layout example of AZ3225-08F.

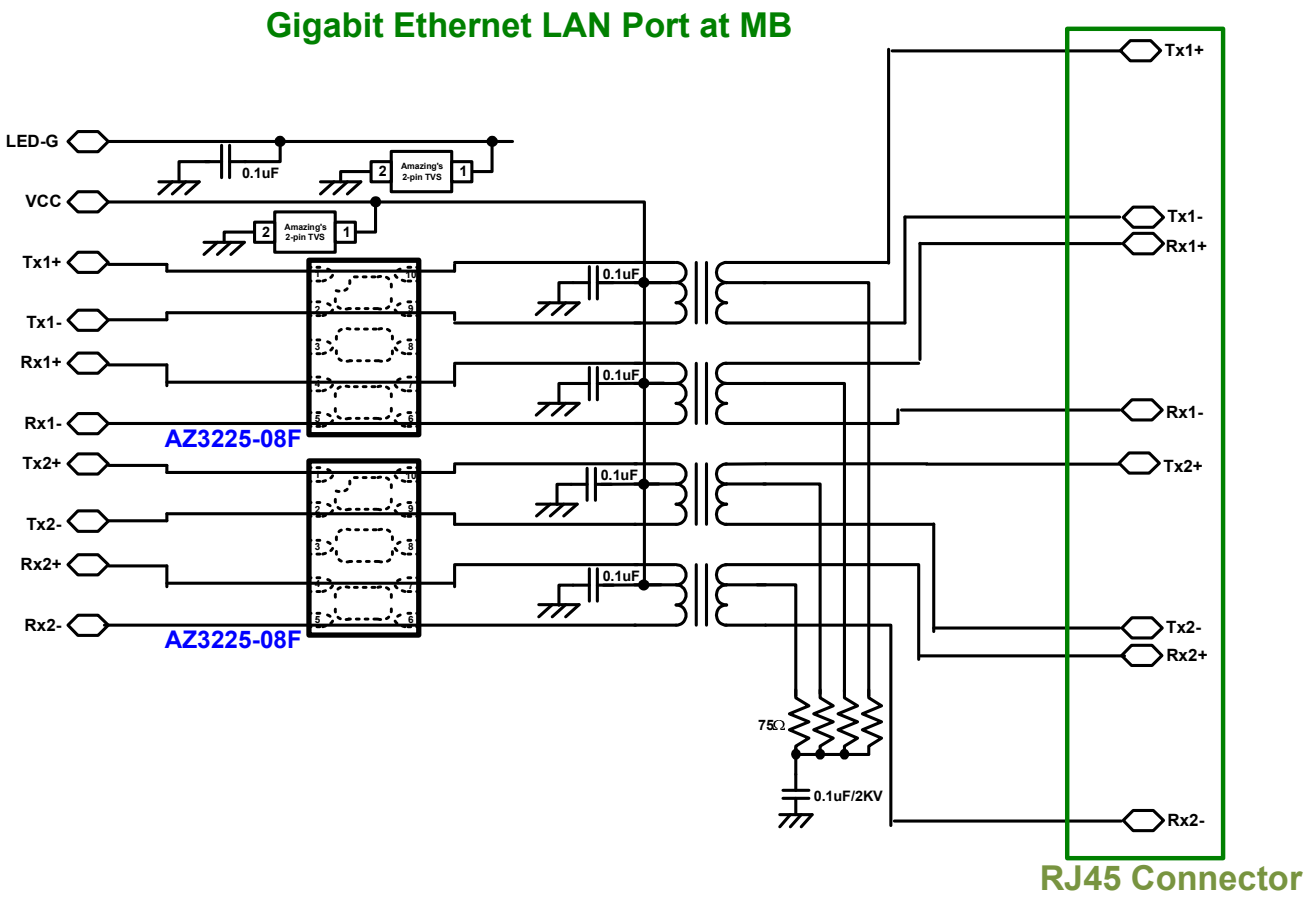
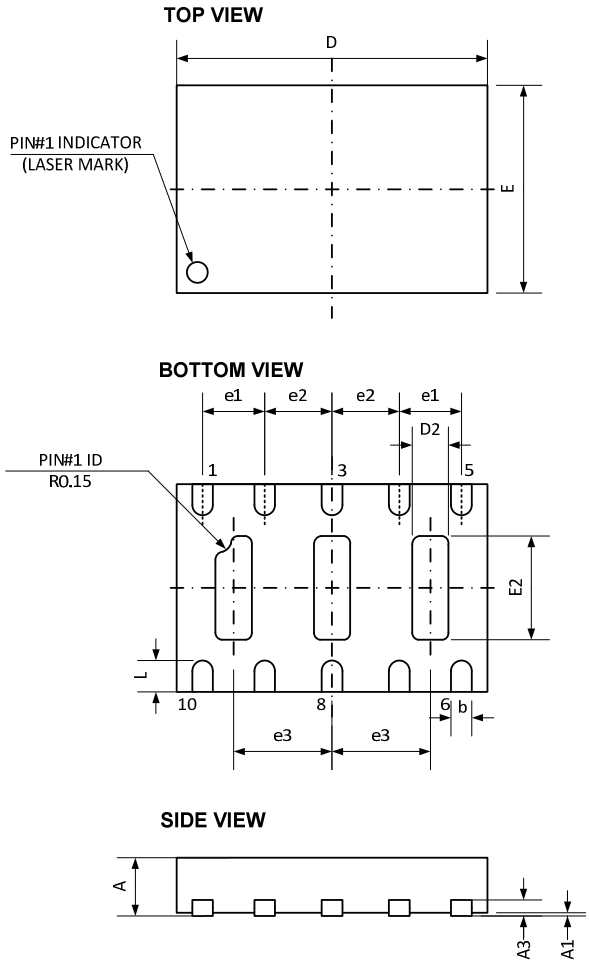


Fig. 3
Gigabit Ethernet surge protection circuit with AZ3225-08F.

Mechanical Details

DFN3020P10E

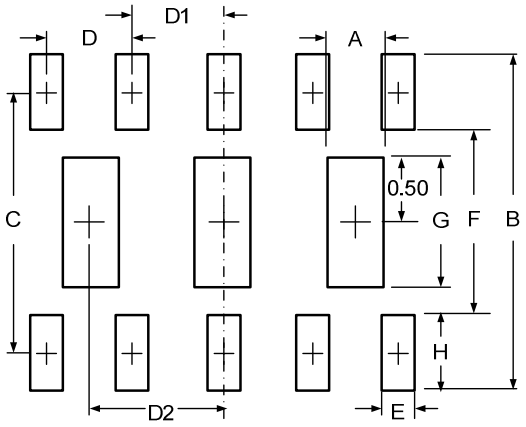
Package Diagrams



Package Dimensions

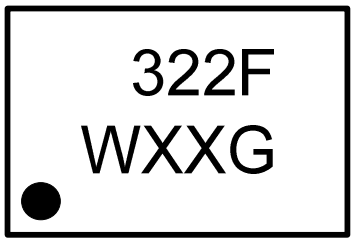
Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.510	0.550	0.600
A1	0.000	0.020	0.050
A3		0.153 REF	
b	0.150	0.200	0.250
D	2.900	3.000	3.100
E	1.900	2.000	2.100
e1		0.600 BSC	
e2		0.650 BSC	
e3		0.950 BSC	
D2	0.250	0.350	0.450
E2	0.950	1.000	1.050
L	0.250	0.300	0.350

Land Layout



Dimensions	
Index	Millimeters
A	0.40
B	2.56
C	1.98
D	0.60
D1	0.65
D2	0.95
E	0.25
F	1.40
G	1.00
H	0.58

Marking Code



322F = Device Code
W = Date Code
XX = Control Code

Part Number	Marking Code
AZ3225-08F.R7G (Green Part)	322F WXXG

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ3225-08F.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

Revision History

Revision	Modification Description
Revision 2019/11/28	Formal Release