

DS100BR410

Low Power Quad Channel Repeater with 10.3125 Gbps Equalizer and De-Emphasis Driver

General Description

The DS100BR410 is an extremely low power, high performance quad-channel repeater for high-speed serial links with data rates up to 10.3125 Gbps. The device performs both receive equalization and transmit de-emphasis on each of its 4 channels to compensate for channel loss, allowing maximum flexibility of physical placement within a system.

The receiver's continuous time linear equalizer (CTLE) is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium such as backplane trace or cable. The transmitter features adjustable V_{OD} (output amplitude voltage level) and de-emphasis driver to compensate for PCB trace loss.

With a low power consumption and control to turn-off unused channels, the DS100BR410 is part of National's PowerWise family of energy efficient devices.

The programmable settings can be applied via pin mode or SMBus mode interface.

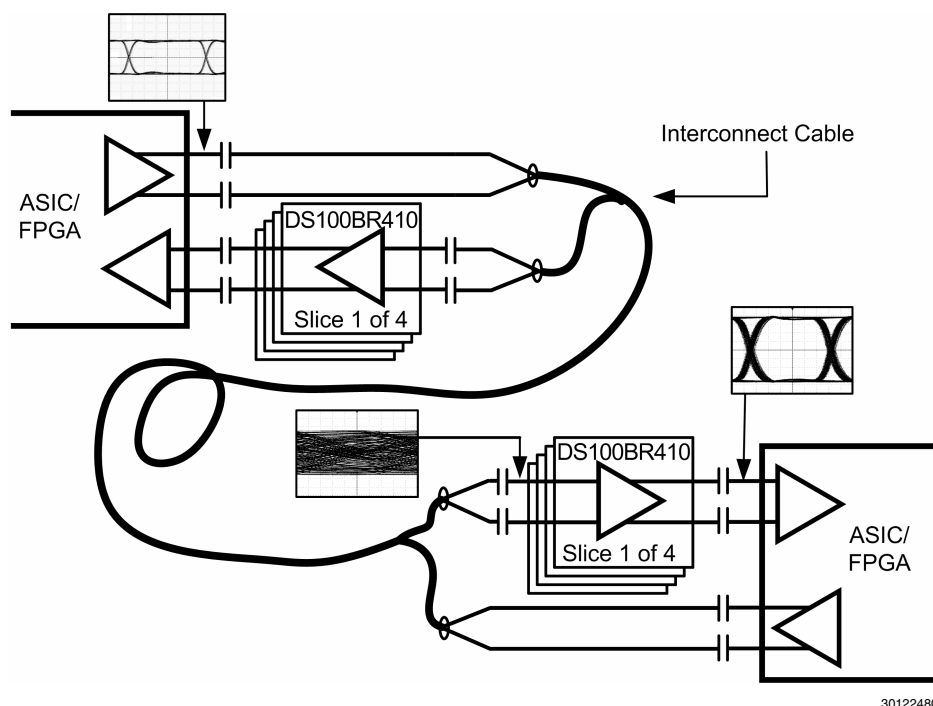
Features

- Quad channel repeater for up to 10.3125 Gbps
- Low power consumption, with option to power down unused channels
- Adjustable receive equalization
- Adjustable transmit de-emphasis
- Adjustable transmit V_{OD} (up to 1200 mVp-p)
- IDLE detection — squelch function auto mutes the output for SATA/SAS OOB signal
- <0.22 UI of residual DJ at 10.3125 Gbps with 12 meters cable
- Programmable via pin selection or SMBus interface
- Single supply operation at 2.5 V \pm 5%
- -40°C to +85°C Operation
- \geq 7 kV HBM ESD Rating
- High speed signal flow-thru pinout package: 48-pin LLP (7 mm x 7 mm, 0.5 mm pitch)

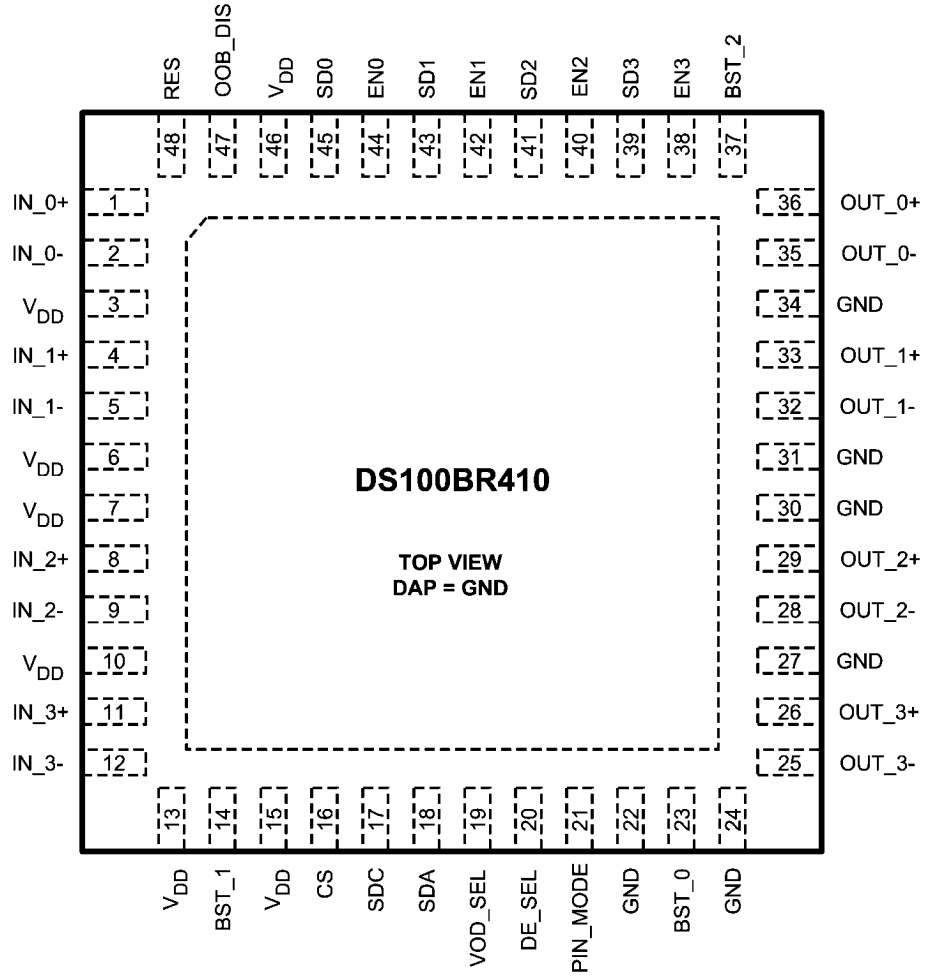
Applications

- High-speed active copper cable modules
- FR-4 Backplanes
- 10GE, 8GFC, 10GFC, 10G SONET, SAS, SATA, and InfiniBand

Typical Application Diagram



Connection Diagram



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Ordering Information

NSID	Package Description	Quantity	Package	Spec
DS100BR410SQE	48-pin LLP (7mm X 7mm X 0.8mm, 0.5mm pitch)	250 in Tape & Reel	SQA48A	NOPB
DS100BR410SQ	48-pin LLP (7mm X 7mm X 0.8mm, 0.5mm pitch)	1000 in Tape & Reel	SQA48A	NOPB
DS100BR410SQX	48-pin LLP (7mm X 7mm X 0.8mm, 0.5mm pitch)	2500 in Tape & Reel	SQA48A	NOPB

Pin Descriptions

Pin Name	Pin #	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
IN_0+	1	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor connects IN_0+ to IN_0-.
IN_0-	2		
IN_1+	4	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor connects IN_1+ to IN_1-.
IN_1-	5		
IN_2+	8	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor connects IN_2+ to IN_2-.
IN_2-	9		
IN_3+	11	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor connects IN_3+ to IN_3-.
IN_3-	12		
OUT_0+	36	O, CML	Inverting and non-inverting CML differential outputs from the driver. An on-chip 100Ω terminating resistor connects OUT_0+ to OUT_0-.
OUT_0-	35		
OUT_1+	33	O, CML	Inverting and non-inverting CML differential outputs from the driver. An on-chip 100Ω terminating resistor connects OUT_1+ to OUT_1-.
OUT_1-	32		
OUT_2+	29	O, CML	Inverting and non-inverting CML differential outputs from the driver. An on-chip 100Ω terminating resistor connects OUT_2+ to OUT_2-.
OUT_2-	28		
OUT_3+	26	O, CML	Inverting and non-inverting CML differential outputs from the driver. An on-chip 100Ω terminating resistor connects OUT_3+ to OUT_3-.
OUT_3-	25		
2.5V LVC MOS CONTROL PINS			
BST_2	37	I, LVC MOS	BST_2, BST_1, and BST_0 select the equalizer boost level for all channels. BST_2 and BST_1 are internally pulled high. BST_0 is internally pulled low. See Table 1
BST_1	14		
BST_0	23		
EN0	44	I, LVC MOS	Enable channel n input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
EN1	42		
EN2	40		
EN3	38		
PIN_MODE	21	I, LVC MOS	Pin mode control input. When held High, device is in Pin control mode. When held Low, device is in SMBus Control Mode PIN_MODE is internally pulled High.
SD0	45	O, LVC MOS	Signal detect n output. Output is High when signal is detected. Output is Low when signal is NOT detected.
SD1	43		
SD2	41		
SD3	39		
OOB_DIS	47	I, LVC MOS	OOB disable control input. When held High, OOB is disabled. When held Low, OOB is enabled. Out Of Band (OOB) for SATA/SAS applications is active. OOB_DIS is internally pulled Low.
Analog Input Pins (4-level Inputs)			
VOD_SEL	19	I, analog	Differential Output Voltage Select Input Tie to V_{DD} , $V_{OD} = 1.2$ Vp-p Leave Open, $V_{OD} = 1.0$ Vp-p Resistor (20 kΩ) to GND, $V_{OD} = 800$ mVp-p Tie to GND, $V_{OD} = 600$ mVp-p
DE_SEL	20	I, analog	De-Emphasis Select Input Tie to $V_{DD} = -9$ dB Leave Open = -6 dB Resistor (20 kΩ) to GND = -3 dB Tie to GND = 0 dB

Pin Name	Pin #	I/O, Type	Description
SERIAL MANAGEMENT BUS (SMBus) INTERFACE			
SDA	18	I/O, LVCMOS	Data Input / Open Drain Output External pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant.
SDC	17	I, LVCMOS	Clock Input Pin is 3.3 V LVCMOS tolerant.
CS	16	I, LVCMOS	Chip Select When high, access to the SMBus registers are enabled. When low, access to the SMBus registers are disabled. Please refer to "SMBus configuration Registers" section for detail information. Pin is 3.3 V LVCMOS tolerant.
POWER			
V _{DD}	3, 6, 7, 10, 13, 15, 46	Power	V _{DD} = 2.5 V ± 5%
GND	22, 24, 27, 30, 31, 34	Power	Ground reference.
DAP	PAD	Power	Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board with at least 4 via to lower the ground impedance and improve the thermal performance of the package.
RES	48	NC	Reserved – Do not connect

Note: I = Input O = Output, LVCMOS pins are 2.5 V levels only, **only SMBus pins SDA, SDC and CS are 3.3V tolerant.**

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	-0.5V to +2.75V
2.5 I/O Voltage (LVCMOS and Analog Input)	-0.5V to +2.75V
3.3 LVCMOS I/O Voltage (SDA, SDC, CS)	-0.5V to +4.0V
CML Input Voltage ($IN_{n+/-}$)	-0.5V to +2.75V
CML Output Voltage ($OUT_{n+/-}$)	-0.5V to +2.75V
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
ESD Rating	
HBM, STD - JESD22-A114F	≥7 kV

MM, STD - JESD22-A115-A	≥200 V
CDM, STD - JESD22-C101-D	≥1250 V
Thermal Resistance	
θ_{JA} , No Airflow, 4 layer JEDEC, 9 thermal vias	27.6 °C/W

For soldering specifications: see product folder at www.national.com
www.national.com/ms/MS/MS-SOLDERING.pdf

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DD} to GND	2.375	2.5	2.625	V
Ambient Temperature	-40	25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges with default register settings unless other specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER						
PD	Power Supply Consumption	Device Output Enabled (EN[3:0] = High), VOD_SEL = open (1.0 Vp-p)		220	275	mW
		Device Output Disable (EN[3:0] = Low)		25	40	mW
PS _{NT}	Supply Noise Tolerance (Note 4)	50 Hz to 100 Hz		100		mV _{p-p}
		100 Hz to 10 MHz		40		mV _{p-p}
		10 MHz to 5.0 GHz		10		mV _{p-p}
2.5 LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		1.75		V_{DD}	V
V_{IL}	Low Level Input Voltage		-0.3		0.7	V
V_{OH}	High Level Output Voltage	$I_{OH} = -3mA$	2.0			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 3mA$			0.4	V
I_{IN}	Input Leakage Current	$V_{IN} = V_{DD}$			+10	μA
		$V_{IN} = GND$	-10			μA
I_{IN-P}	Input Leakage Current with Internal Pull-Down/Up Resistors	$V_{IN} = V_{DD}$, with internal pull-down resistors			+65	μA
		$V_{IN} = GND$, with internal pull-up resistors	-50			μA
SIGNAL DETECT						
SDH	Signal Detect ON Threshold Level	Default input signal level to assert SD pin, 10.3125 Gbps		130		mV _{p-p}
SDL	Signal Detect OFF Threshold Level	Default input signal level to de-assert SD, 10.3125 Gbps		60		mV _{p-p}

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CML RECEIVER INPUTS (IN_{n+}, IN_{n-})						
V _{TX}	Source Transmit Launch Signal Level (IN diff)	AC-Coupled Requirement, Differential measurement at point A. Figure 1	600		1600	mV _{P-P}
R _{LI}	Differential Input Return Loss - SDD11	100 MHz – 6 GHz, with fixture's effect de-embedded		-15		dB
CML DRIVER OUTPUTS (OUT_{n+}, OUT_{n-})						
V _{OD}	Output Differential Voltage Level (Note 6), Figure 2	Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled, VOD_SEL = open (1.0 Vp-p), DE_SEL = GND	750	970	1150	mV _{P-P}
		Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled, VOD_SEL = V _{DD} (1.2 Vp-p), DE_SEL = GND		1140		mV _{P-P}
V _{OD_DE}	De-Emphasis Levels (Note 6 , Note 7)	DE_SEL = 20kΩ to GND, VOD_SEL = V _{DD} (1.2 Vp-p)		-3		dB
		DE_SEL = open, VOD_SEL = V _{DD} (1.2 Vp-p)		-6		dB
		DE_SEL = V _{DD} , VOD_SEL = V _{DD} (1.2 Vp-p)		-9		dB
t _R , t _F	Transition Time	20% to 80% of differential output voltage, measured within 1" from output pins. Figure 2	30	38	45	ps
R _{LO}	Differential Output Return Loss - SDD22	100 MHz – 6 GHz, with fixture's effect de-embedded. IN+ = static high.		-15		dB
t _{PLHD}	Differential Low to High Propagation Delay	Propagation delay measurement at 50% crossing between input to output, 100 Mbps. Figure 3		240		ps
t _{PHLD}	Differential High to Low Propagation Delay			240		ps
t _{CCSK}	Inter Pair Channel to Channel Skew	Difference in 50% crossing between channels		7		ps
t _{PPSK}	Part to Part Output Skew	Difference in 50% crossing between outputs		20		ps
RJ	Random Jitter	V _{TX} = 1.0 Vp-p, BST_[2:0] = 000, (Note 6 , Note 8)		0.3		ps _{rms}

Symbol	Parameter	Conditions	Min	Typ	Max	Units
EQUALIZATION						
DJ1	Residual Deterministic Jitter at 10.3125 Gbps	$V_{TX} = 1.0 V_{P-P}$, 12 meter 30 AWG cable, EQ = 03F'h (BST[2:0] = 111), PRBS-7 (27-1) pattern. (<i>Note 5</i>)		0.10	0.22	UI_{P-P}
DJ2	Residual Deterministic Jitter at 6.0 Gbps	$V_{TX} = 1.0 V_{P-P}$, 12 meter 30 AWG cable, EQ = 07F'h, PRBS-7 (27-1) pattern. (<i>Note 5</i>)		0.07	0.12	UI_{P-P}
SIGNAL DETECT and ENABLE TIMING						
t_{ZISD}	Input OFF to ON detect — SD Output High Response Time	Response time measurement at V_{IN} to SD output, $V_{IN} = 800 mV_{P-P}$,		35		ns
t_{IZSD}	Input ON to OFF detect — SD Output Low Response Time	100 Mbps, 40" of 6 mil microstrip FR4. <i>Figure 4</i>		400		ns
t_{OZOED}	EN High to Output ON Response Time	Response time measurement at EN input to V_O , $V_{IN} = 800 mV_{P-P}$,		150		ns
t_{ZOED}	EN Low to Output OFF Response Time	100 Mbps, 40" of 6 mil microstrip FR4. <i>Figure 5</i>		5		ns

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: Typical values represent most likely parametric norms at $V_{DD} = 2.5V$, $T_A = 25^\circ C.$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 3: Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

Note 4: Specification is guaranteed by characterization at optimal boost setting and is not tested in production.

Note 5: Deterministic jitter is measured at the differential outputs (point C of Figure 1), minus the deterministic jitter before the test channel (point A of Figure 1). Random jitter is removed through the use of averaging or similar means.

Note 6: Measured with clock-like {11111 00000} pattern.

Note 7: The de-emphasis level of -3 dB, -6 dB, -9 dB are for $V_{OD} = 1.2 V_{p-p}$. At lower V_{OD} level, the de-emphasis levels are reduced.

Note 8: Random jitter contributed by the equalizer is defined as $\sqrt{J_{OUT}^2 - J_{IN}^2}$. J_{OUT} is the random jitter at equalizer outputs in ps-rms, see point C of Figure 1; J_{IN} is the random jitter at the input of the equalizer in ps-rms, see point B of Figure 1.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified. (*Note 2*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		V_{DD}	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-BUS}$	Input Leakage Per Bus Segment	(<i>Note 11</i>)	-200		+200	μ A
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		μ A
C_I	Capacitance for SDA and SDC	(<i>Note 11, Note 12</i>)			10	pF
R_{TERM}	External Termination Resistance pull to $V_{DD} = 2.5V \pm 5\%$ OR $3.3V \pm 10\%$	$V_{DD3.3}$ (<i>Note 11, Note 12</i>)		2000		Ω
		$V_{DD2.5}$ (<i>Note 11, Note 12</i>)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS – (See <i>Figure 6</i>)						
F_{SMB}	Bus Operating Frequency		10		100	kHz
T_{BUF}	Bus Free Time Between Stop and Start Condition		4.7			μ s
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP} , Max	4.0			μ s
$T_{SU:STA}$	Repeated Start Condition Setup Time		4.7			μ s
$T_{SU:STO}$	Stop Condition Setup Time		4.0			μ s
$T_{HD:DAT}$	Data Hold Time		300			ns
$T_{SU:DAT}$	Data Setup Time		250			ns
T_{LOW}	Clock Low Period		4.7			μ s
T_{HIGH}	Clock High Period		4.0		50	μ s
t_F	Clock/Data Fall Time				300	ns
t_R	Clock/Data Rise Time				1000	ns
t_{POR}	Time in which a device must be operational after power-on reset				500	ms

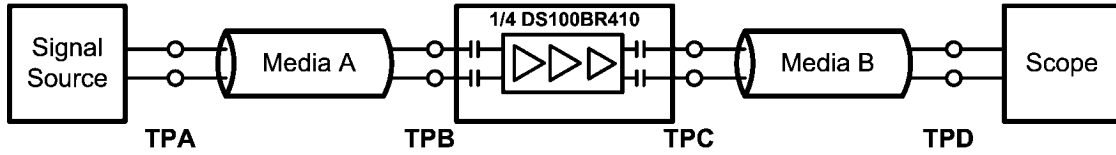
Note 9: Recommended value. Parameter not tested in production.

Note 10: Recommended maximum capacitance load per bus segment is 400pF.

Note 11: Maximum termination voltage should be identical to the device supply voltage.

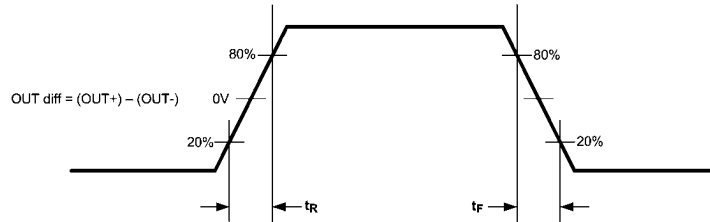
Note 12: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

AC Waveforms and Test Circuits



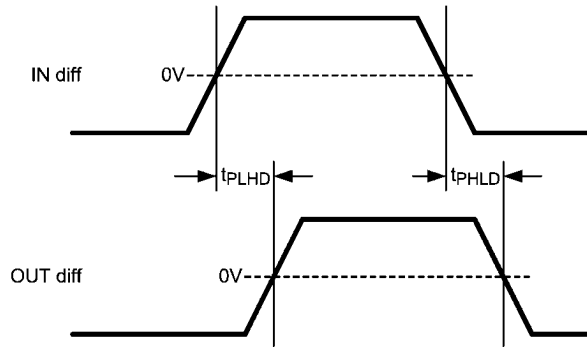
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FIGURE 1. Test Setup Diagram



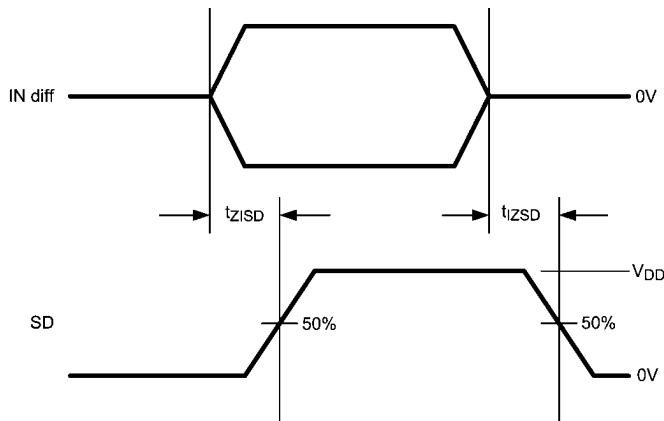
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FIGURE 2. Output Transition Times



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FIGURE 3. Propagation Delay Timing Diagram



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FIGURE 4. Signal Detect (SD) Delay Timing Diagram

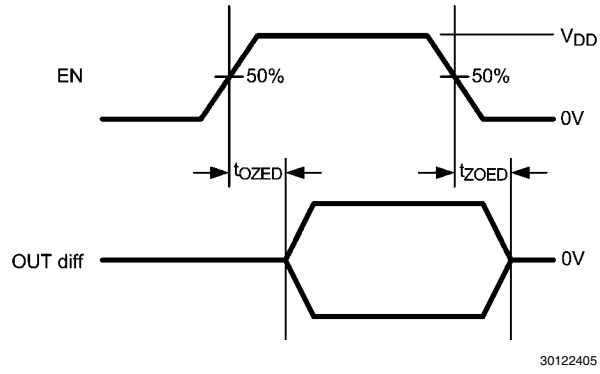


FIGURE 5. Enable (EN) Delay Timing Diagram

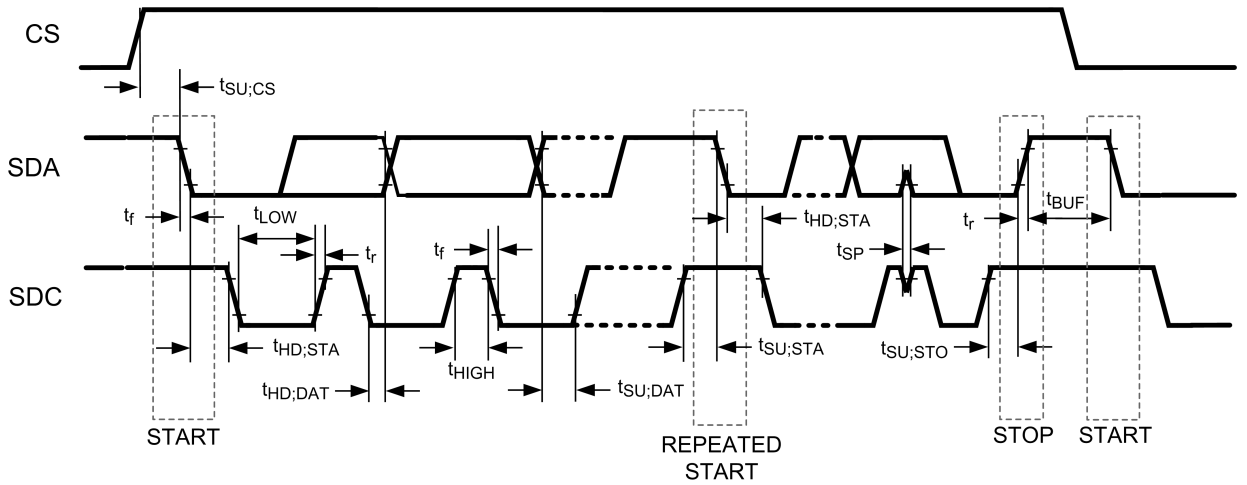


FIGURE 6. SMBus Timing Parameters

Functional Description

DS100BR410 Functional Descriptions

The DS100BR410 is a Low Power Quad Channel Repeater with Equalizer and De-Emphasis Driver optimized for operation up to 10.3125 Gbps for backplane and cable applications.

DATA CHANNELS

The DS100BR410 provides four data channels. Each data channel consists of an equalizer stage, a limiting amplifier, a DC offset correction block, and a CML driver as shown in [Figure 7](#).

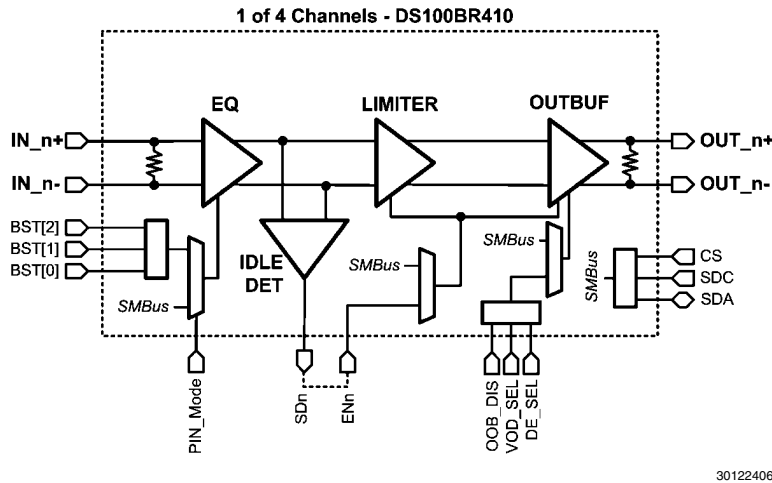


FIGURE 7. Simplified Block Diagram

EQUALIZER BOOST CONTROL

Each data channel support eight programmable levels of equalization boost. The state of the PIN_MODE control input determines how the boost settings are controlled. If PIN_MODE is held High, then the equalizer boost setting is controlled by the Boost Set pins (BST_[2:0]) in accordance with [Table 1](#). If this programming method is chosen, then the boost setting selected on the Boost Set pins is applied to all channels. When PIN_MODE is held Low, the equalizer boost level is controlled through the SMBus. This programming method is accessed via the appropriate SMBus registers (see [Table 4](#)). Using this approach, equalizer boost settings can be programmed for each channel individually. PIN_MODE is internally pulled High, therefore if left open, the boost settings are controlled by the Boost Set pins (BST_[2:0]). The eight levels of boost settings enables the DS100BR410 to address a wide range of media loss and data rates.

TABLE 1. Boost / EQ Pin Mode Configuration

Inputs			SMBus Register Bits	Result @ 5 GHz
BST_2	BST_1	BST_0	[8:0]	
0	0	0	00000000	2.7 dB
0	0	1	00000001	7.3 dB
0	1	0	00000011	12.2 dB
0	1	1	00000111	16.6 dB
1	0	0	00001111	20.6 dB
1	0	1	00011111	24.8 dB

Inputs			SMBus Register Bits	Result @ 5 GHz
BST_2	BST_1	BST_0	[8:0]	
1	1	0	00010111	27.6 dB (default)
1	1	1	00011111	28.9 dB

SIGNAL DETECT

The DS100BR410 features a signal detect circuit on each data channel. The status of the signal of each channel can be determined by either reading the Signal Detect bit (SDn) in the SMBus registers (see [Table 4](#)) or by the state of each SDn pin. An output logic high indicates the presence of a signal that has exceeded the ON threshold value (called SDH). An output logic Low means that the input signal has fallen below the OFF threshold value (called SDL). These values are programmed via the SMBus. If not programmed via the SMBus, the thresholds take on the default values. The Signal Detect threshold values can be changed through the SMBus. All threshold values specified are DC peak-to-peak differential signals (positive signal minus negative signal) at the input of the device.

OUTPUT LEVEL CONTROL

The output amplitude of the CML drivers can be controlled via the 4-level analog input VOD_SEL pin or via SMBus (see [Table 4](#)). The default V_{OD} level is 1.0 Vp-p.

TABLE 2. VOD_SEL Pin Configuration

VOD_SEL Pin	Result
Tie High - V _{DD}	1.2 Vp-p
Open* (default)	1.0 Vp-p
20 kΩ resistor to GND	800 mVp-p
Tie to GND	600 mVp-p

OUTPUT DE-EMPHASIS CONTROL

The output De-Emphasis may be controlled via the 4-level analog input DE_SEL pin or via SMBus (see [Table 4](#)).

TABLE 3. DE_SEL Pin Configuration

DE_SEL Pin	Result
Tie High - V_{DD}	-9 dB
Open* (default)	-6 dB
20 k Ω resistor to GND	-3 dB
Tie to GND	0 dB

AUTOMATIC ENABLE FEATURE

It may be desirable to place unused channels in power-saving Standby mode. This can be accomplished by connecting the Signal detect (SDn) pin to the Enable (ENn) pin for each channel (See [Figure 7](#)).

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. The use of the Chip Select signal is **required**. Holding the CS pin High enables the SMBus port allowing access to the configuration registers. Holding the CS pin Low disables the device's SMBus allowing communication from the host to other slave devices on the bus. In the STANDBY state, the System Management Bus remains active. When communication to other devices on the SMBus is active, the CS signal for the DS100BR410s must be driven Low.

The address byte for all DS100BR410s is AC'h. Based on the SMBus 2.0 specification, the DS100BR410 has a 7-bit slave address of 1010110'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 1100'b or AC'h.

The SDA, SDC and CS pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 k Ω to 5 k Ω depending on the voltage, loading and speed. The SDC and CS may also require an external pull-up resistor and it depends on the Host that drives the bus.

Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SDC is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SDC is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SDC is High indicates a message STOP condition.

IDLE: If SDC and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus Transactions

The device supports WRITE, Burst WRITE, READ, and Burst READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
3. The Device (Slave) drives the ACK bit ("0").
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit ("0").
6. The Host drive the 8-bit data byte.
7. The Device drives an ACK bit ("0").
8. The Host drives a STOP condition.
9. The Host de-selects the device by driving its SMBus CS signal Low.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
3. The Device (Slave) drives the ACK bit ("0").
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit ("0").
6. The Host drives a START condition.
7. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
8. The Device drives an ACK bit "0".
9. The Device drives the 8-bit data value (register contents).
10. The Host drives a NACK bit "1" indicating end of the READ transfer.
11. The Host drives a STOP condition.
12. The Host de-selects the device by driving its SMBus CS signal Low.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Information on the Registers

The status registers 01'h to 03'h provide information of the channel that is selected. The information provided are the OOB_DIS, EN, EQ Boost, VOD and DEM bits of the selected channel. By default, channel 0 is selected. In order to change the selected channel, write to reg_07 bit[5:4]. Write a 1 to reg_07 bit[0] is also needed to allow the registers 13'h to 1A'h to control the channel EN and EQ boost bits of each of the channels. Each channel can be individually enabled (EN) and set to a desired boost level with these registers. Please refer to [Table 4](#) for additional information.

TABLE 4. DS100BR410 Register Map

ADD (hex)	REG Name	Bit(s)	Field	Type	Default (binary)	Description
00	Device ID	7:4	Device ID	R	0010	Device ID Value
		3	SD_CH3	R		1: Signal detected on CH3 0: No signal
		2	SD_CH2	R		1: Signal detected on CH2 0: No signal
		1	SD_CH1	R		1: Signal detected on CH1 0: No signal
		0	SD_CH0	R		1: Signal detected on CH0 0: No signal
01	Status Register for OOB_DIS, EN and Boost_bit[8]	7	Reserved	R		
		6	OOB_DIS	R		OOB_DIS 1: OOB Disabled 0: OOB Enabled
		5	Reserved	R		
		4	EN	R		EN 1: Channel Enabled 0: Channel Disabled
		3:1	Reserved	R		
		0	Boost_bit[8]	R		Boost_bit[8]
02	Status Register for Boost_bit [7:0]	7:0	Boost_bit[7:0]	R		Boost_bit[7:0]
03	Status Register for VOD[5:4] and DEM[1:0]	7:6	Reserved	R		
		5:4	VOD[5:4]	R		VOD[5:4] 00 = 0.6 Vp-p 01 = 0.8 Vp-p 10 = 1.0 Vp-p 11 = 1.2 Vp-p
		3:2	Reserved	R		
		1:0	DEM[1:0]	R		DEM[1:0] 00 = 0 dB 01 = -3 dB 10 = -6 dB 11 = -9 dB
04	Reserved	7:0	Reserved	R	00	
05	Signal Detect Assert Threshold	7:6	SD_ON_CH3	R/W	00	Signal Detect ON Threshold
		5:4	SD_ON_CH2	R/W	00	00 = 130 mV
		3:2	SD_ON_CH1	R/W	00	01 = 125 mV
		1:0	SD_ON_CH0	R/W	00	10 = 150 mV 11 = 140 mV
06	Signal Detect De-assert Threshold	7:6	SD_OFF_CH3	R/W	00	Signal Detect OFF Threshold
		5:4	SD_OFF_CH2	R/W	00	00 = 60 mV
		3:2	SD_OFF_CH1	R/W	00	01 = 40 mV
		1:0	SD_FF_CH0	R/W	00	10 = 105 mV 11 = 90 mV

ADD (hex)	REG Name	Bit(s)	Field	Type	Default (binary)	Description
07	Port/Channel Select and Enable SMBus Registers	7:6	Reserved	R/W	00	
		5:4	Port/Channel Select for Status	R/W	00	Select port/channel [1:0] to report status in REG_01 to REG_03 00 = port0 (CH0) 01 = port1 (CH1) 10 = port2 (CH2) 11 = port3 (CH3)
		3:1	Reserved	R/W	000	
		0	SMBUS Channel EN and EQ boost	R/W	0	Channel EN and EQ Boost through pins or smbus REG_13 to REG_1A 0 = Channel EN[3:0] and EQ BST[2:0] boost set by external pins 1 = Allow channel EN and EQ boost to be set by SMBus Register bits: REG_13 to REG_1A
08	Driver V _{OD} Control	7	Reserved	R/W	0	
		6:4	Reserved	R/W	111	
		3:2	VOD Control	R/W	10	00 = 0.6 Vp-p 01 = 0.8 Vp-p 10 = 1.0 Vp-p 11 = 1.2 Vp-p
		1:0	Reserved	R/W	00	
09 – 10	Reserved	7:0	Reserved	R/W	00000000	
11	De-Emphasis Control	7:6	DEM_CH3	R/W	00	00 = 0 dB
		5:4	DEM_CH2	R/W	00	01 = -3 dB
		3:2	DEM_CH1	R/W	00	10 = -6 dB
		1:0	DEM_CH0	R/W	00	11 = -9 dB
12	OOB Signal Detect Control	7:3	Reserved	R/W	00000	
		2:1	Reserved	R/W	11	
		0	OOB Signal Detect Control	R/W	0	0 = OOB signal detect enabled 1 = OOB signal detect disabled
13	Channel 3 EN and EQ Control	7:5	Reserved	R/W	000	
		4	Channel Enable	R/W	1	0 = Disabled 1 = Enabled
		3:1	Reserved	R/W	000	
		0	Boost[8]	R/W	0	See Table 5
14	EQ Control Channel 3	7:0	Boost[7:0]	R/W	00000000	See Table 5
15	Channel 2 EN and EQ Control	7:5	Reserved	R/W	000	
		4	Channel Enable	R/W	1	0 = Disabled 1 = Enabled
		3:1	Reserved	R/W	000	
		0	Boost[8]	R/W	0	See Table 5
16	EQ Control Channel 2	7:0	Boost[7:0]	R/W	00000000	See Table 5
17	Channel 1 EN and EQ Control	7:5	Reserved	R/W	000	
		4	Channel Enable	R/W	1	0 = Disabled 1 = Enabled
		3:1	Reserved	R/W	000	
		0	Boost[8]	R/W	0	See Table 5
18	EQ Control Channel 1	7:0	Boost[7:0]	R/W	00000000	See Table 5

ADD (hex)	REG Name	Bit(s)	Field	Type	Default (binary)	Description
19	Channel 0 EN and EQ Control	7:5	Reserved	R/W	000	
		4	Channel Enable	R/W	1	0 = Disabled 1 = Enabled
		3:1	Reserved	R/W	000	
		0	Boost[8]	R/W	0	See Table 5
1A	EQ Control Channel 0	7:0	Boost[7:0]	R/W	00000000	See Table 5

TABLE 5. Boost / EQ SMBus Register: 16 levels - recommended settings

Boost Register Bits									Result
bit[8]	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	@ 5.5 GHz
0	0	0	0	0	0	0	0	0	000'h - 2.7 dB (BST_[2:0]=000)
0	0	0	0	0	0	0	0	1	001'h - 7.3 dB (BST_[2:0]=001)
0	0	0	0	0	0	0	1	0	002'h - 10.3 dB
0	0	0	0	0	0	0	1	1	003'h - 12.2 dB (BST_[2:0]=010)
0	0	0	0	0	0	1	1	1	007'h - 16.6 dB (BST_[2:0]=011)
0	0	0	0	1	0	1	0	1	015'h - 17 dB
0	0	0	0	0	1	0	1	1	00B'h - 19.2 dB
0	0	0	0	0	1	1	1	1	00F'h - 20.6 dB (BST_[2:0]=100)
0	0	1	0	1	0	1	0	1	055'h - 21.9 dB
0	0	0	0	1	1	1	1	1	01F'h - 24.8 dB (BST_[2:0]=101)
0	0	0	1	0	1	1	1	1	02F'h - 27.6 dB (BST_[2:0]=110)
0	0	0	1	1	1	1	1	1	03F'h - 28.9 dB (BST_[2:0]=111)
0	1	0	1	0	1	0	1	0	0AA'h - 31.3 dB
0	0	1	1	1	1	1	1	1	07F'h - 33.3 dB
0	1	0	1	1	1	1	1	1	0BF'h - 35.7 dB
0	1	1	1	1	1	1	1	1	0FF'h - 37 dB

Applications Information

GENERAL RECOMMENDATIONS

The DS100BR410 is a high performance circuit capable of delivering excellent performance up to 10.3125 Gbps. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

UNUSED CHANNEL

It is recommended to disable the unused channel (EN[3:0] = LOW). The power consumption of the device is reduced when the channel is disabled.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The high speed CML inputs and outputs must have a controlled differential impedance of 100Ω . It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

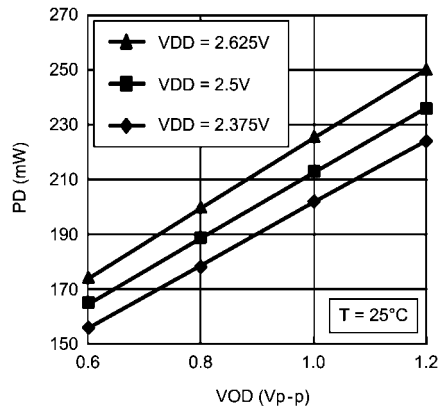
Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each via hole. To further improve the signal quality, a ground via placed

close to the signal via for a low inductance return current path is recommended. When the via structure is associated with stripline trace and a thick board, further optimization such as back drilling is often used to reduce the high frequency effects of via stubs on the signal path. To minimize cross-talk coupling, it is recommended to have $>3X$ gap spacing between the differential pairs. For example, if the trace width is 5 mils with 5 mils spacing – 100Ω differential impedance (closely coupled). The gap spacing between the differential pairs should be >15 mils.

POWER SUPPLY BYPASSING

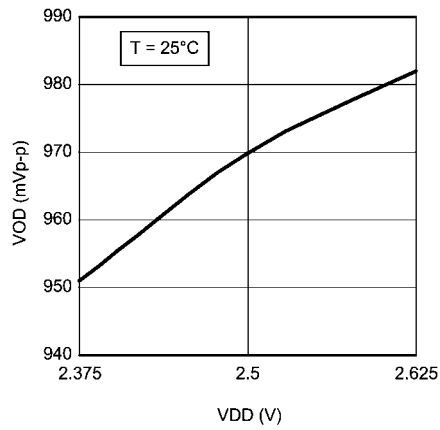
Two approaches are recommended to ensure that the DS100BR410 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A $0.1\mu\text{F}$ or $0.01\mu\text{F}$ bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS100BR410. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of $2.2\mu\text{F}$ to $10\mu\text{F}$ should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

Typical Performance Curves Characteristics



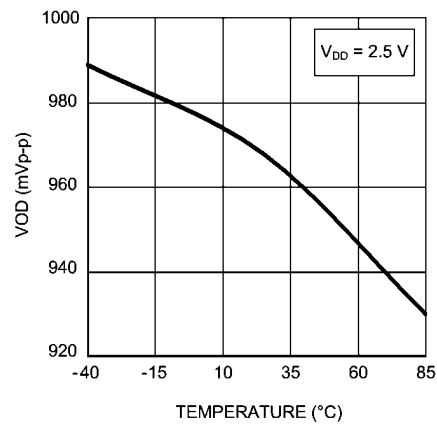
30122428

FIGURE 8. Power Dissipation (PD) vs. Output Differential Voltage (VOD)



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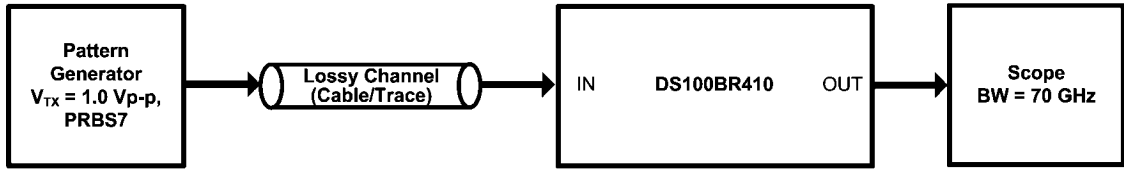
FIGURE 9. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Supply Voltage (VDD)



30122430

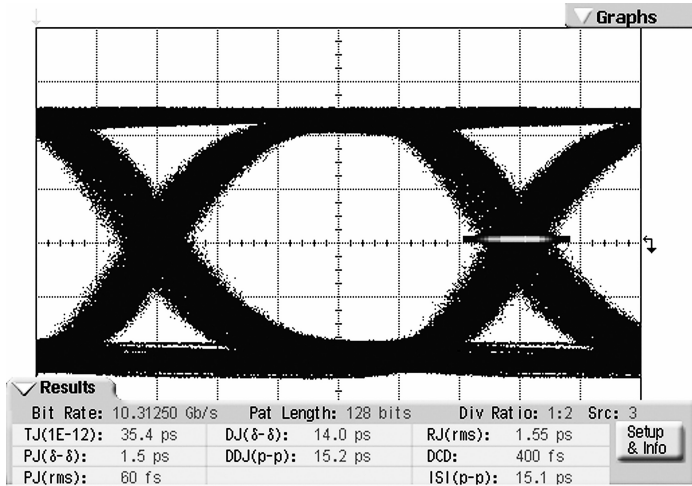
FIGURE 10. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Temperature

Typical Performance Eye Diagrams Characteristics



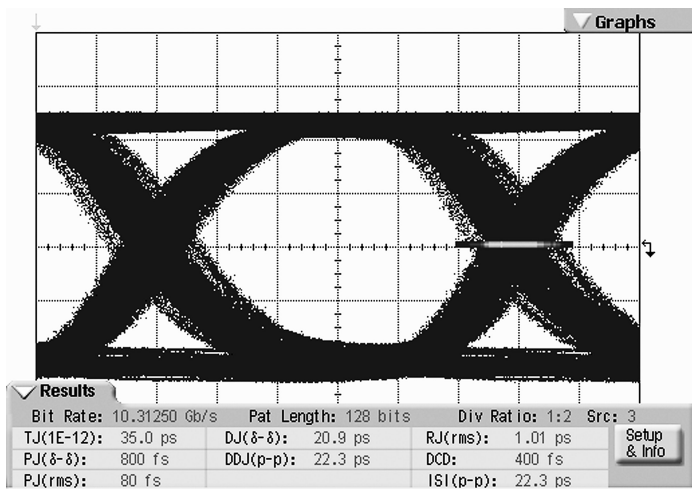
30122431

FIGURE 11. Test Setup Connections Diagram



30122432

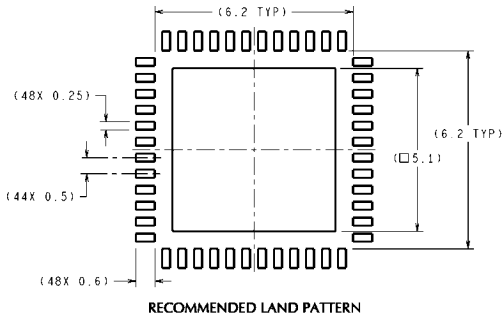
FIGURE 12. 12 meters, 30-AWG Cable at 10.3125 Gbps, BST[2:0] = 111, DE_SEL = 0 dB



30122433

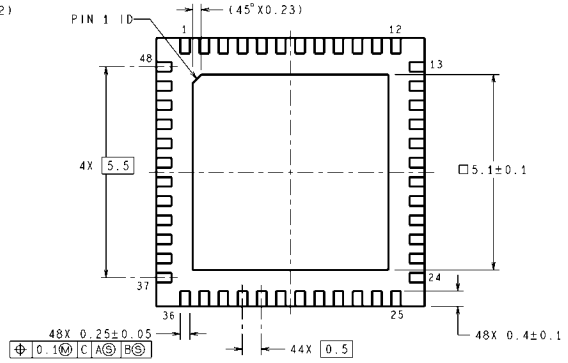
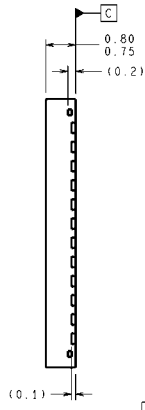
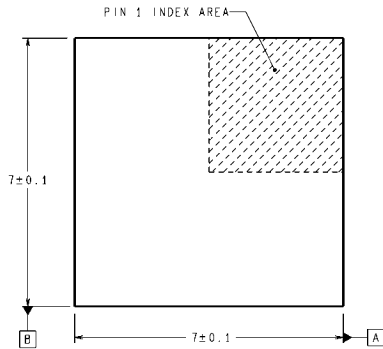
FIGURE 13. 40 inches, 6-mil FR4 Trace at 10.3125 Gbps, BST[2:0] = 101, DE_SEL = 0 dB

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN



SQA48A (Rev B)

48-pin LLP Package (7 mm x 7 mm x 0.8 mm, 0.5 mm pitch)
Package Number SQA48A

Notes

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