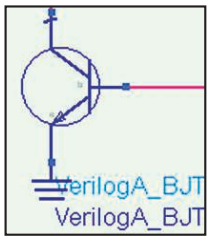
Keysight EEsof EDA

W2303 Verilog-A Element
W2304 Verilog-AMS Element

Verilog-A custom non-linear models can be developed and used in all ADS circuit simulators.

```
Verilog-A definition of SPICE Gummel-Poon

$RCSfile: bjt.va,v $ $Revision: 1.9 $ $Date: 2005/01/27 22:51:59 $

*/

`include "constants.vams"
`include "disciplines.vams"
`include "compact.vams"

`define INCLUDE_LEAD_INDUCTANCE
`define INCLUDE_DELAY
`define THREE_TERMINALS

`define PI_SQ_24 14.5902504445
`define PI_SQ_144 2.43170840742

`define ZERO_TO_INF(paramValue, varName, infinity) \
   if (paramValue == 0.0) \
      varName = infinity;\
   else \
      varName = paramValue

`ifdef THREE_TERMINALS
module VerilogA_BJT(c,b,e);
`else
module VerilogA_BJT(c,b,e,s);
`endif
```



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Introduction

The W2303 Verilog-A and W2304 Verilog-AMS elements are analog and analog-mixed signal behavioral modeling and simulation environments for the Advanced Design System (ADS). ADS is the flagship product from Keysight Technologies' EEsof EDA, the technology and innovation leader in high-frequency mixed-signal electronic design automation (EDA).

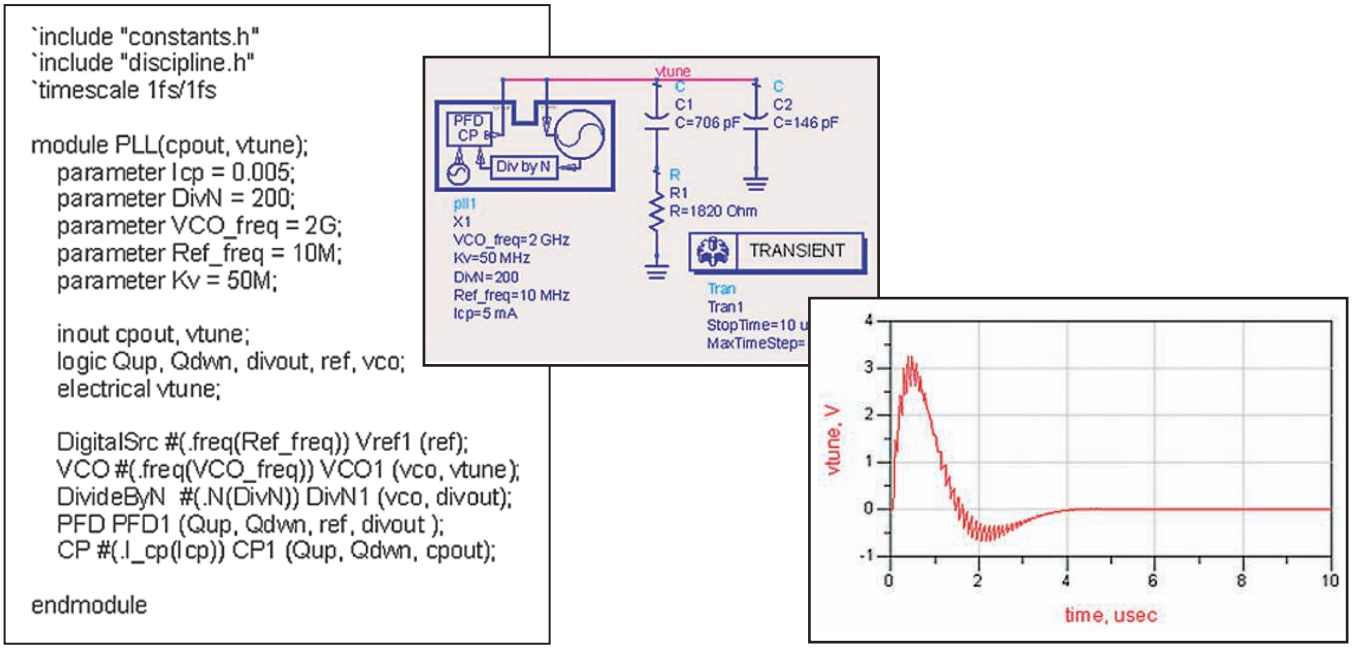
ADS is the only design simulation platform that enables the co-design of IC, package, and board in high-frequency and high-speed applications. It seamlessly integrates system, circuit, and full 3D electromagnetic simulation with Keysight Technologies' test instrumentation, resulting in repeatable, first-pass electronic design success.

The W2303 Verilog-A Element enables analog behavioral modeling with the industry standard Verilog-A language within ADS. Used for applications ranging from transistors to MEMs, the Verilog-A models are compiled for speed and can be simulated and optimized with any of the time-, frequency- or envelope-domain system and circuit simulators in ADS. The user-defined models using standard Verilog-A equation constructs are intelligently compiled in ADS to use the fast and robust convergence algorithms already engineered for built-in ADS models, thus eliminating the special formulation of behavioral equations for specific simulators to converge. A comprehensive library of valuable Verilog-A source codes are supplied for new and built-in ADS models to allow fast new model development or to efficiently customize the underlying model equations. Customized Verilog-A models can contain parameters that can be extracted from measurements in Keysight's powerful IC-CAP (Integrated Circuit Characterization and Analysis Program) parameter extraction and device modeling software environment that also controls instrumentation and probe stations.

The W2304 Verilog-AMS Element is a superset of W2303 by adding the support of analog-mixed signal models such as hi-speed SERDES (Serializer-Deserializer) and PLL (phase-locked loops) for high-speed and RF communication applications. It also enables and manages the co-simulation of Verilog-AMS models in ADS Transient- Convolution simulator W2302 with third party digital simulator such as Cadence NCSim or Mentor ModelSim to analyze the analog, digital and mixed-signal aspects of a circuit and system design simultaneously. Verilog-AMS co-simulation requires only the ADS Transient-Convolution simulator (W2302). It does not require Keysight Ptolemy.

The W2303 and W2304 Verilog-A/AMS Elements include:

- Support for industry-standard Verilog-A and Verilog-AMS model development in ADS, with run-time speed and convergence comparable to built-in ADS models.
- Simulation and optimization in ADS time-, frequency- and envelope-domain system and circuit simulators, with full access to powerful internal convergence algorithms.
- At least 10x less lines of code compared with C-language-based models.
- Fully portable model development for use in all Verilog-A/AMS compatible simulators, distributable through design kits.
- Verilog-A/AMS model parameters extracted from measurements in the Keysight ICCAP device modeling environment.
- Verilog-AMS models that can be co-simulated in the ADS Transient-Convolution
- simulator along with 3rd party digital simulators such as Cadence NCSim and Mentor Modelsim.
- Verilog-A source codes for new models.
- Verilog-A Source codes for built-in devices.



Verilog-AMS custom analog-mixed-signal models can be developed and co-simulated in ADS Transient-Convolution simulator with third party digital simulators such as NCSim and Modelsim.

New models for which Verilog-A models are included	
Model Name	Description
aTFT	Shur-RPI amorphous silicon thin film transistor MOSFET model
BSIMSOI	Version 3.1 of the BSIMSOI model family
EKV	Version 2.6 of the EKV MOSFET model
HICUM_L0	Level 0 version of the HICUM BJT model, a simplified version of the full HICUM model
HiSIM	STARC/Hiroshima University surface potential based MOSFET model
Parker_Skellern	The Parker-Skellern MESFET model for medium power applications
pTFT	Shur-RPI polysilicon thin film transistor MOSFET model

ADS built-in devices for which Verilog-A source codes are included	
Model Name	Description
Angelov	Angelov GaAs FET model
BJT	SPICE Gummel-Poon BJT model
BSIM3	UC Berkeley BSIM3 (version 3.22)
BSIM4	UC Berkeley BSIM4 (version 4.3)
Curtice	Curtice Quadratic GaAs FET model
Diode	SPICE diode
JFET	SPICE silicon junction FET
JunCap	Philips JunCap diode
MESFET	SPICE Metal Semiconductor FET model
MEXTRAM	Philips Most Exquisite Transistor model for BJT devices
MOS9	Philips MOS Model 9
MOS11	Philips MOS Model 11
TOM1	Triquint's Own Model 1
TOM3	Triquint's Own Model 3
VBIC	Vertical Bipolar InterCompany BJT model, as released

Unlike other behavioral modeling environments where intimate knowledge of the target simulator algorithms are required, the ADS Verilog-A/AMS behavioral modeling compilers intelligently enable the complete functionality and convergence capabilities developed originally for built-in models to be applied to user-defined models. Compared to C-language-based models, Verilog-A/AMS models require 10x less coding. Together with the rich set of Verilog-A device source codes to start from, you are guaranteed the most efficient language-based behavioral modeling capability possible.

Use this link **for more information about Verilog-A**.

Use this link **for more information about Verilog-AMS**.

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