DS100MB203

10.3125 Gbps Dual Lane 2:1/1:2 Mux/Buffer with Equalization and De-Emphasis

General Description

The DS100MB203 is a dual port 2:1 multiplexer and 1:2 switch or fan-out buffer with signal conditioning suitable for 10GE, 10G-KR (802.3ap), Fibre Channel, PCIe, Infiniband, SATA/SAS and other high speed bus applications with data rates up to 10.3125 Gbps. The receiver's 4-stage advanced continuous time linear equalizer (CTLE) provides necessary boost to compensate up to 40" FR-4 or 20m cable (AWG-24) at 10.3125 Gbps - This on-chip feature eliminates the need for external signal conditioners. The transmitter features a programmable amplitude voltage levels to be selectable from 600 mVp-p to 1300 mVp-p and De-Emphasis of up to 12 dB.

The DS100MB203 can be configured to support PCIe, SAS/SATA, 10G-KR or other signaling protocols. Based on the selected operating mode, the DS100MB203 seamlessly adapts the signal conditioning levels and management of control signals (SAS/SATA OOB, PCIe BEACONs & IDLE). While in 10G-KR (802.3ap) or PCIe (Gen-3 only) mode the DS100MB203 transparently allows the host controller and the end point to optimize the full link by adjusting transmit equalizer coefficients using back channel signaling. These features guarantee interoperability at both the electrical and system level, while reducing design complexity.

With a low power consumption of 390 mW total (typ) and option to turn-off unused channels, the DS100MB203 enables energy efficient system design. A single supply of 3.3v or 2.5v is required to power the device. The programmable settings can be applied via pin settings, SMBus (I2C) protocol or loaded directly from an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver.

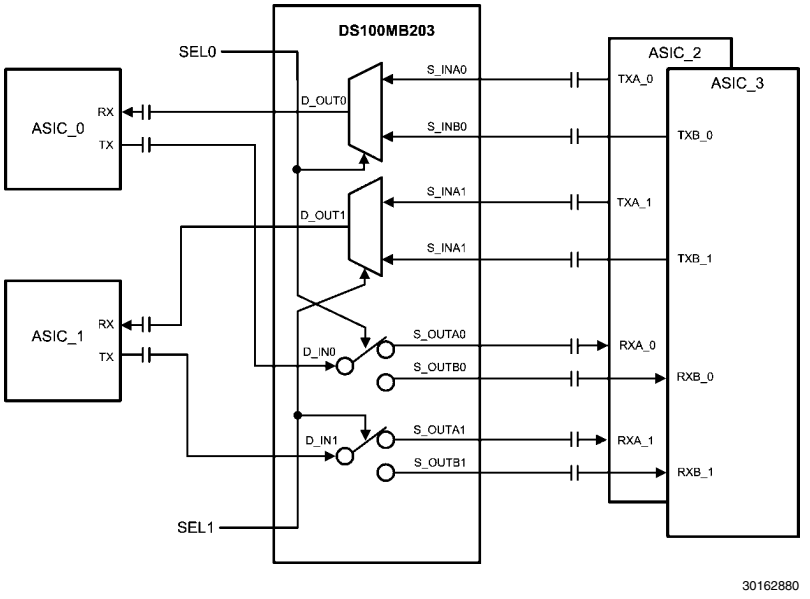
Features

- 10.3125 Gbps Dual Lane 2:1 Mux, 1:2 Switch or Fanout
- Low 390 mW total power (typ) power consumption, with option to power down unused channels
- Advanced signal conditioning features
  - Receive Equalization up to 36 dB at 5 GHz
  - Transmit de-emphasis up to -12 dB
  - Transmit output voltage control: 600 mV to 1300 mV
- Programmable via pin selection, EEPROM or SMBus interface
- Single supply operation selectable: 2.5V or 3.3V
- -40° to +85°C operating temperature range
- 3 kV HBM ESD rating

Supported Protocols

- 10GE, 10G-KR
- PCIe Gen-1/2/3
- SAS/SATA, Fibre Channel
- XAUI, RXAUI
- sRIO, Infiniband
- Other proprietary up to 10.3125 Gbps

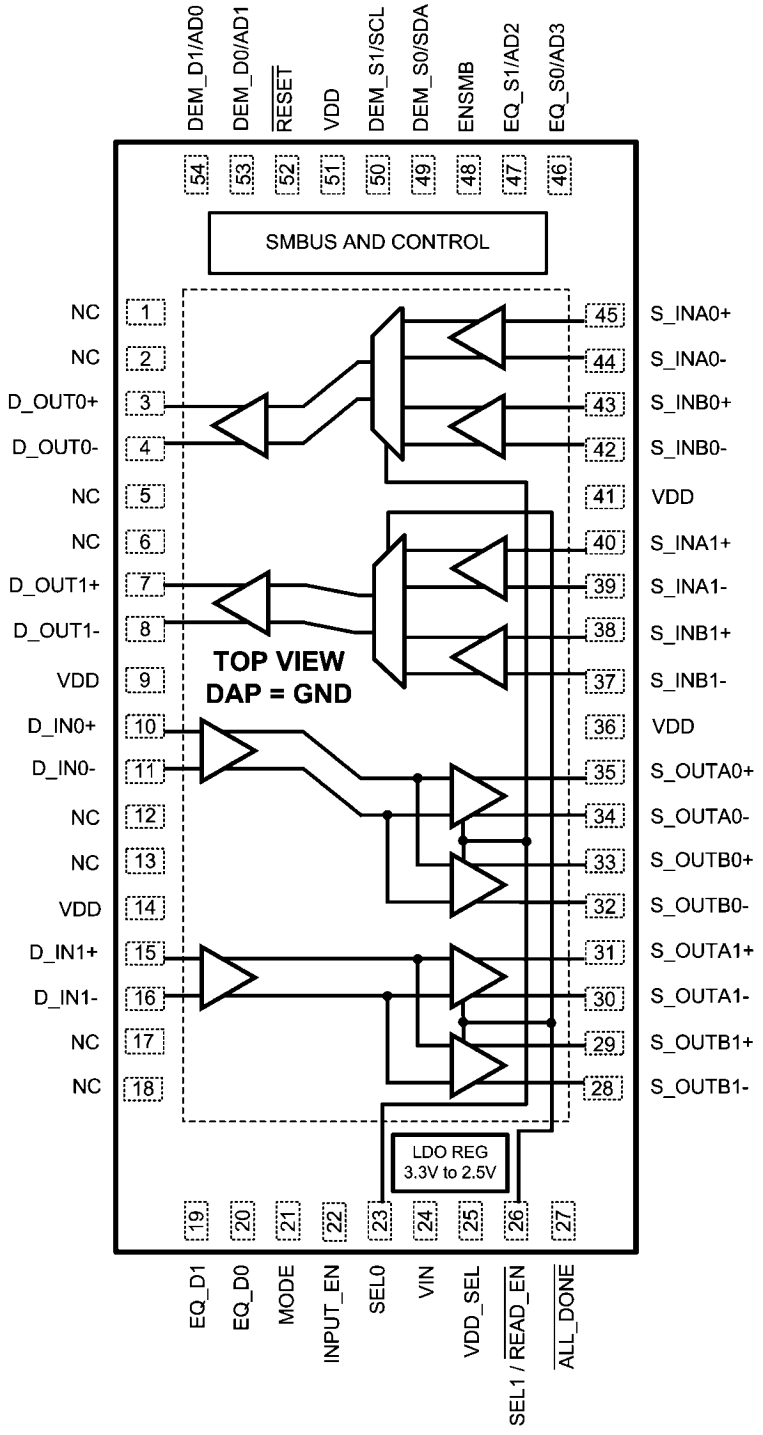
Typical Application



DS100MB203 10.3125 Gbps Dual Lane 2:1/1:2 Mux/Buffer with Equalization and De-Emphasis

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Pin Diagram



DS100MB203 Pin Diagram 54 Lead

Ordering Information

NSID	Qty	Spec	Package
DS100MB203SQ	Tape & Reel Supplied As 2,000 Units	NOPB	SQA54A
DS100MB203SQE	Tape & Reel Supplied As 250 Units	NOPB	SQA54A

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Pin Description
Differential High Speed I/O's			
D_IN0+, D_IN0-, D_IN1+, D_IN1-	10, 11, 15, 16	I	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects D_INn+ to VDD and D_INn- to VDD when enabled.
D_OUT0+, D_ OUT0-, D_OUT1+, D_OUT1-	3, 4, 7, 8	O	Inverting and non-inverting low power differential signaling 50Ω outputs with de-emphasis. Fully compatible with AC coupled CML inputs.
S_INA0+, S_INA0-, S_INA1+, S_INA1-	45, 44, 40, 39	I	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω termination resistor connects S_INAn+ to VDD and S_INAn- to VDD
S_OUTA0+, S_OUTA0-, S_OUTA1+, S_OUTA1-	35, 34, 31, 30	O	Inverting and non-inverting low power differential signaling 50Ω outputs with de-emphasis. Fully compatible with AC coupled CML inputs.
S_INB0+, S_INB0-, S_INB1+, S_INB1-	43, 42, 38, 37	I	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω termination resistor connects S_INBn+ to VDD and S_INBn- to VDD
S_OUTB0+, S_OUTB0-, S_OUTB1+, S_OUTB1-	33, 32, 29, 28	O	Inverting and non-inverting low power differential signaling 50Ω outputs with de-emphasis. Fully compatible with AC coupled CML inputs.
Control Pins - Shared (LVCMOS)			
ENSMB	48	I, FLOAT, LVCMOS	System Management Bus (SMBus) enable pin LOW = Pin Mode FLOAT = Read External EEPROM HIGH = Register Access SMBus Slave mode
ENSMB = 1 (SMBUS SLAVE MODE), Float (SMBUS MASTER MODE)			
SCL	50	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode SMBUS clock input pin is enabled (slave mode) SMBUS clock output when loading configuration from EEPROM (master mode)
SDA	49	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode The SMBus bi-directional SDA pin is enabled. Data input or open drain (pull-down only) output.
AD0-AD3	54, 53, 47, 46	I, LVCMOS	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs.
$\overline{\text{READ_EN}}$	26	I, LVCMOS	ENSMB = FLOAT (SMBUS master mode) When using an External EEPROM, a transition from high to low starts the load from the external EEPROM
ENSMB = 0 (PIN MODE)			
EQ_D0, EQ_D1 EQ_S0, EQ_S1	20, 19 46, 47	I, 4-LEVEL, LVCMOS	EQ_D[1:0] and EQ_S[1:0] control the level of equalization on the high speed input pins. The pins are active only when ENSMB is deasserted (low). The input are organized into two sides. The D side is controlled with the EQ_D[1:0] pins and the S side is controlled with the EQ_S[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The EQ_S[1:0] pins are converted to SMBUS AD2/ AD3 inputs. EQ_D[1:0] pins are not used.

Pin Name	Pin Number	I/O, Type	Pin Description
DEM_S0, DEM_S1 DEM_D0, DEM_D1	49, 50 53, 54	I, 4-LEVEL, LVCMOS	DEM_D[1:0] and DEM_S[1:0] control the level of VOD and de-emphasis on the high speed output. The pins are active only when ENSMB is deasserted (low). The output are organized into two sides. The D side is controlled with the DEM_D[1:0] pins and the S side is controlled with the DEM_S [1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The DEM_D [1:0] and DEM_S[1:0] pins are converted to SMBUS AD1/AD0 and SCL/SDA inputs.
Control Pins — Both Pin and SMBus Modes (LVCMOS)			
MODE	21	I, 4-LEVEL, LVCMOS	0: SATA/SAS, PCIe GEN 1/2 and 10GE 20kΩ to GND: PCIe GEN 3 FLOAT: AUTO (PCIe GEN 1/2 or GEN 3) 1: 10-KR
INPUT_EN	22	I, 4-LEVEL, LVCMOS	0: Normal Operation, FANOUT is disabled, use SEL0/1 to select the A or B input/output (see SEL0/1 pin), input always enabled with 50 ohms. 20kΩ to GND: Reserved FLOAT: AUTO - Use RX Detect, SEL0/1 to determine which input or output to enable, FANOUT is disable 1: Normal Operation, FANOUT is enabled (both S_OUT0/1 are ON). Input always enabled with 50 ohms.
SEL0	23	I, 4-LEVEL, LVCMOS	Select pin for Lane 0. 0: selects input **S_INB0+/-**, output **S_OUTB0+/-**. 20kΩ to GND: selects input **S_INB0+/-**, output **S_OUTA0+/-**. FLOAT: selects input **S_INA0+/-**, output **S_OUTB0+/-**. 1: selects input **S_INA0+/-**, output **S_OUTA0+/-**.
SEL1	26	I, 4-LEVEL, LVCMOS	Select pin for Lane 1. 0: selects input **S_INB1+/-**, output **S_OUTB1+/-**. 20kΩ to GND: selects input **S_INB1+/-**, output **S_OUTA1+/-**. FLOAT: selects input **S_INA1+/-**, output **S_OUTB1+/-**. 1: selects input **S_INA1+/-**, output **S_OUTA1+/-**.
VDD_SEL	25	I, FLOAT	Controls the internal regulator FLOAT = 2.5V mode Tied to GND: 3.3V mode
$\overline{\text{RESET}}$	52	I, LVCMOS	0: Normal Operation (device is enabled). 1: Low Power Mode.
Output (LVCMOS)			
$\overline{\text{ALL_DONE}}$	27	0, LVCMOS	Valid Register Load Status Output 0: External EEPROM load passed 1: External EEPROM load failed
Power			
VIN	24	Power	In 3.3V mode, feed 3.3V +/-10% to VIN In 2.5V mode, leave floating.
VDD	9, 14,36, 41, 51	Power	Power supply pins CML/analog 2.5V mode, connect to 2.5V +/-5% 3.3V mode, connect 0.1 uF cap to each VDD pin
GND	DAP	Power	Ground pad (DAP - die attach pad).

Notes:

LVCMOS inputs without the “Float” conditions must be driven to a logic low or high at all times or operation is not guaranteed. Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.

Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.

For 3.3V mode operation, VIN pin = 3.3V and the "VDD" for the 4-level input is 3.3V.

For 2.5V mode operation, VDD pin = 2.5V and the "VDD" for the 4-level input is 2.5V.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Supply Voltage (VDD - 2.5V mode)	-0.5V to +2.75V
Supply Voltage (VIN - 3.3V mode)	-0.5V to +4.0V
LVCMOS Input/Output Voltage	-0.5V to +4.0V
CML Input Voltage	-0.5V to (VDD+0.5)
CML Input Current	-30 to +30 mA
Junction Temperature	125°C
Storage Temperature	-40°C to +125°C
SQA54A Package	
Derate SQA54A Package	52.6mW/°C above +25°C

ESD Rating	
HBM, STD - JESD22-A114F	3 kV
MM, STD - JESD22-A115-A	200 V
CDM, STD - JESD22-C101-D	1 kV
Thermal Resistance	
θJC	11.5°C/W
θJA, No Airflow, 4 layer JEDEC	19.1°C/W
Soldering Information (Note 4)	

	Min	Typ	Max	Units
Supply Voltage (2.5V mode)	2.375	2.5	2.625	V
Supply Voltgae (3.3V mode)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C
SMBus (SDA, SCL)			3.6	V
Supply Noise up to 50 MHz (Note 5)			100	mVp-p

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power						
PD	Power Dissipation	VDD = 2.5 V supply EQ Enabled, VOD = 1.0 Vp-p, RESET = 0		390	499	mW
		VIN = 3.3 V supply EQ Enabled, VOD = 1.0 Vp-p, RESET = 0		515	684	mW
LVCMOS / LVTTL DC Specifications						
V_{ih}	High Level Input Voltage		2.0		VDD	V
V_{il}	Low Level Input Voltage		0		0.8	V
V_{oh}	High Level Output Voltage (ALL_DONE pin)	I_{oh}= –4mA	2.0			V
V_{ol}	Low Level Output Voltage (ALL_DONE pin)	I_{ol}= 4mA			0.4	V
I_{ih}	Input High Current (RESET pin)	VIN = 3.6 V, LVCMOS = 3.6 V	-15		+15	uA
	Input High Current with internal resistors (4–level input pin)		+20		+150	uA
I_{il}	Input Low Current (RESET pin)	VIN = 3.6 V, LVCMOS = 0 V	-15		+15	uA
	Input Low Current with internal resistors (4–level input pin)		-160		-40	uA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CML Receiver Inputs (IN_n+, IN_n-)						
$RL_{rx-diff}$	RX Differential return loss	0.05 - 1.25 GHz		-16		dB
		1.25 - 2.5 GHz		-16		dB
		2.5 - 4.0 GHz		-14		dB
RLrx-cm	RX Common mode return loss	0.05 - 2.5 GHz		-12		dB
		2.5 - 4.0 GHz		-8		dB
Zrx-dc	RX DC common mode impedance	Tested at VDD = 2.5 V	40	50	60	Ω
Zrx-diff-dc	RX DC differntial mode impedance	Tested at VDD = 2.5 V	80	100	120	Ω
Vrx-signal-det-diff-pp	Signal detect assert level for active data signal	0101 pattern at 10.3125 Gbps		180		mVp-p
Vrx-idle-det-diff-pp	Signal detect de-assert level for electrical idle	0101 pattern at 10.3125 Gbps		110		mVp-p

Symbol	Parameter	Conditions	Min	Typ	Max	Units
High Speed Outputs						
$V_{tx\text{-}diff\text{-}pp}$	Output Voltage Differential Swing	Differential measurement with OUT_n+ and OUT_n-, terminated by 50Ω to GND, AC-Coupled, VID = 1.0 Vp-p, DEM_x[1:0] = R, F, (*Note 8*)	0.8	1.0	1.2	Vp-p
$V_{tx\text{-}de\text{-}ratio_3.5}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM_x[1:0] = R, F		-3.5		dB
$V_{tx\text{-}de\text{-}ratio_6}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM_x[1:0] = F, 0		-6		dB
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	TX Dj > 1.5 MHz				0.15	UI
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	TX RMS jitter < 1.5 MHz				3.0	ps RMS
$T_{TX\text{-}RISE\text{-}FALL}$	TX rise/fall time	20% to 80% of differential output voltage	35	45		ps
$T_{RF\text{-}MISMATCH}$	TX rise/fall mismatch	20% to 80% of differential output voltage		0.01	0.1	UI
$RL_{TX\text{-}DIFF}$	TX Differential return loss	0.05 - 1.25 GHz		-16		dB
		1.25 - 2.5 GHz		-12		dB
		2.5 - 4 GHz		-11		dB
$RL_{TX\text{-}CM}$	TX Common mode return loss	0.05 - 2.5 GHz		-12		dB
		2.5 - 4 GHz		-8		dB
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance			100		Ω
$V_{TX\text{-}CM\text{-}AC\text{-}PP}$	TX AC common mode voltage	VOD = 1.0 Vp-p, DEM_x[1:0] = R, F			100	mVpp
$I_{TX\text{-}SHORT}$	TX short circuit current limit	Total current the transmitter can supply when shorted to VDD or GND		20		mA
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle				100	mV
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common mode voltgae between TX+ and TX-				25	mV
$T_{TX\text{-}IDLE\text{-}DATA}$	Max time to transition to differential DATA signal after IDLE	VID = 1.0 Vp-p, 8 Gbps		3.5		ns
$T_{TX\text{-}DATA\text{-}IDLE}$	Max time to transition to IDLE after differential DATA signal	VID = 1.0 Vp-p, 8 Gbps		6.2		ns
$T_{PLHD/PHLD}$	High to Low and Low to High Differential Propagation Delay	EQ = 00, (*Note 7*)		200		ps
T_{LSK}	Lane to lane skew	T = 25C, VDD = 2.5V		25		ps
T_{PPSK}	Part to part propagation delay skew	T = 25C, VDD = 2.5V		40		ps
$T_{MUX\text{-}SWITCH}$	Mux/Switch Time			100		ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Equalization						
DJE1	Residual deterministic jitter at 10.3125 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 1F'h,** DEM = 0 dB		0.3		UI
DJE2	Residual deterministic jitter at 8 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 1F'h,** DEM = 0 dB		0.14		UI
DJE3	Residual deterministic jitter at 5 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15,**EQ = 1F'h,** DEM = 0 dB		0.1		UI
DJE4	Residual deterministic jitter at 2.5 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 1F'h,** DEM = 0 dB		0.05		UI
DJE5	Residual deterministic jitter at 10.3125 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 2F'h,** DEM = 0 dB		0.3		UI
DJE6	Residual deterministic jitter at 8 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 2F'h,** DEM = 0 dB		0.16		UI
DJE7	Residual deterministic jitter at 5 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 2F'h,** DEM = 0 dB		0.1		UI
DJE8	Residual deterministic jitter at 2.5 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 2F'h,** DEM = 0 dB		0.05		UI

Symbol	Parameter	Conditions	Min	Typ	Max	Units
De-emphasis (MODE = 0)						
DJD1	Residual deterministic jitter at 2.5 Gbps and 5.0 Gbps	10” 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 00, VOD = 1.0 Vp-p, **DEM = –3.5 dB**		0.1		UI
DJD2	Residual deterministic jitter at 2.5 Gbps and 5.0 Gbps	20” 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 00, VOD = 1.0 Vp-p, **DEM = –9 dB**		0.1		UI
DJD3	Residual deterministic jitter at 10.3125 Gbps	20” 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 00, VOD = 1.0 Vp-p, **DEM = –9 dB**		0.1		UI

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

Note 2: Typical values represent most likely parametric norms at VDD = 2.5V, TA = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 4: See Application Note SNOA549C: http://www.ti.com/lit/an/snoa549c/snoa549c.pdf

Note 5: Allowed supply noise (mVp-p sine wave) under typical conditions.

Note 6: Guaranteed by device characterization.

Note 7: Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 00 will result in the shortest propagation delays.

Note 8: In GEN3 mode, the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEM_x[1:0] in GEN3 mode is dependent on the VID level and the frequency content. The DS100MB203 repeater in GEN3 mode is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support the PCIe GEN3 handshake negotiation link training.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(*Note 9*)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	(*Note 9*, *Note 10*)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	Pullup V_{DD} = 3.3V, (*Note 9*, *Note 10*, *Note 11*)		2000		Ω
		Pullup V_{DD} = 2.5V, (*Note 9*, *Note 10*, *Note 11*)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode)	280	400	520	kHz
TBUF	Bus Free Time Between Stop and Start Condition		1.3			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	0.6			µs
TSU:STA	Repeated Start Condition Setup Time		0.6			µs
TSU:STO	Stop Condition Setup Time		0.6			µs
THD:DAT	Data Hold Time		0			ns
TSU:DAT	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period	(*Note 12*)	0.6		50	µs
t_F	Clock/Data Fall Time	(*Note 12*)			300	ns
t_R	Clock/Data Rise Time	(*Note 12*)			300	ns
t_{POR}	Time in which a device must be operational after power-on reset	(*Note 12*, *Note 13*)			500	ms

Note 9: Recommended value.

Note 10: Recommended maximum capacitance load per bus segment is 400pF.

Note 11: Maximum termination voltage should be identical to the device supply voltage.

Note 12: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

Note 13: Guaranteed by Design. Parameter not tested in production.

Timing Diagrams

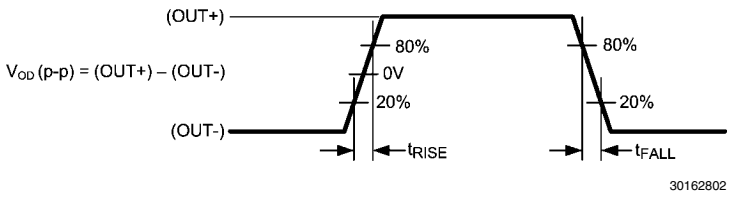


FIGURE 1. CML Output and Rise and FALL Transition Time

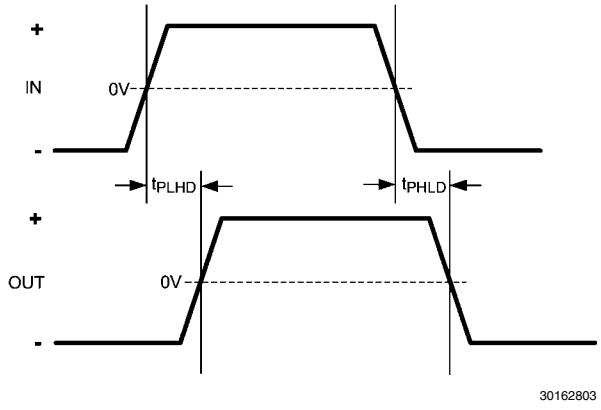


FIGURE 2. Propagation Delay Timing Diagram

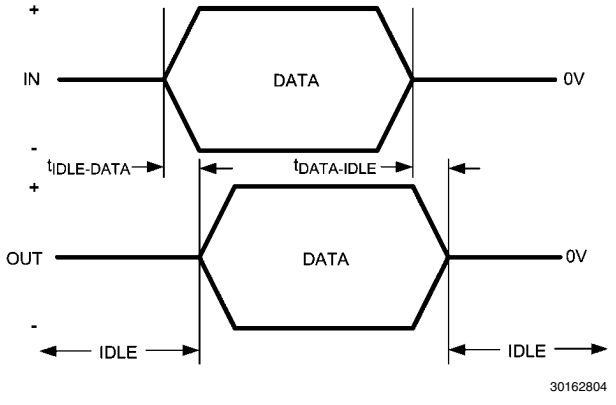


FIGURE 3. Transmit IDLE-DATA and DATA-IDLE Response Time

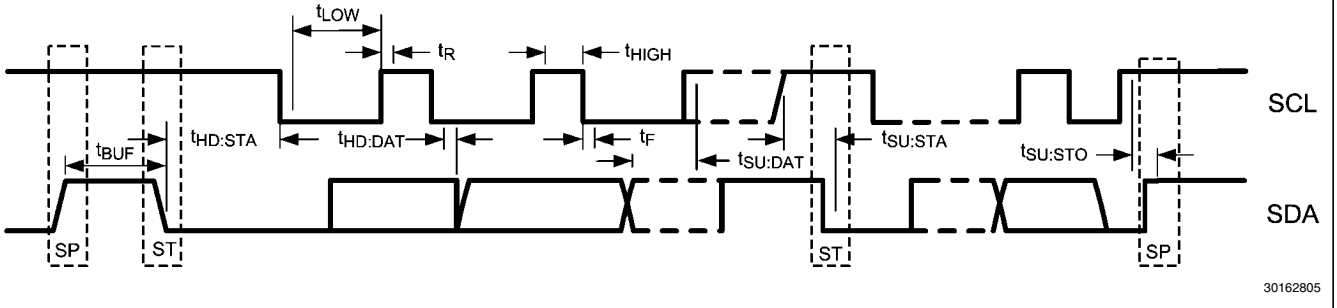


FIGURE 4. SMBus Timing Parameters

Functional Descriptions

The DS100MB203is a dual lane 2:1 multiplexer and 1:2 switch or fan-out buffer with signal conditioning. The DS100MB203 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS100MB203 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register informations from external EEPROM; please refer to SMBUS Master Mode for additional information.

Pin Control Mode:

When in pin mode (ENSMB = 0), equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per the De-Emphasis table below.

SMBUS Mode:

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by D or S as in the pin mode case. Upon assertion of ENSMB, the EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. On power-up and when ENSMB is driven low all registers are reset to their default state. If RESET is asserted (tied High) while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most PCIe applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. The tables show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-Emphasis levels are set by registers.

The input control pins have been enhanced to have 4 different levels and provide a wider range of control settings when ENSMB=0.

Table 1: 4–Level Control Pin Settings

Pin Setting	Description	Voltage at Pin
0	Tie 1kΩ to GND	0.03 x VDD
R	Tie 20kΩ to GND	1/3 x VDD
Float	Float (leave pin open)	2/3 x VDD
1	Tie 1kΩ to VDD	0.98 x VDD
Note: The above required resistor value is for a single device. When there are multiple devices connected to the pull-up / pull-down resistor, the value must scale with the number of devices. If 4 devices are connected to a single pull-up or pull-down, the 1kΩ resistor value should be 250Ω. For the 20kΩ to GND, this should also scale to 5kΩ.		

3.3V or 2.5V Supply Mode Operation

The DS100MB203 has an optional internal voltage regulator to provide the 2.5V supply to the device. In 3.3V mode, the VIN pin = 3.3V is used to supply power to the device and the VDD pins should be left open. The internal regulator will provide the 2.5V to the VDD pins of the device and a 0.1 uF cap is needed at each of 5 VDD pins for power supply de-coupling (total capacitance should be ≤0.5 uF). The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5V mode, the VIN pin should be left open and 2.5V supply must be applied to the VDD pins. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

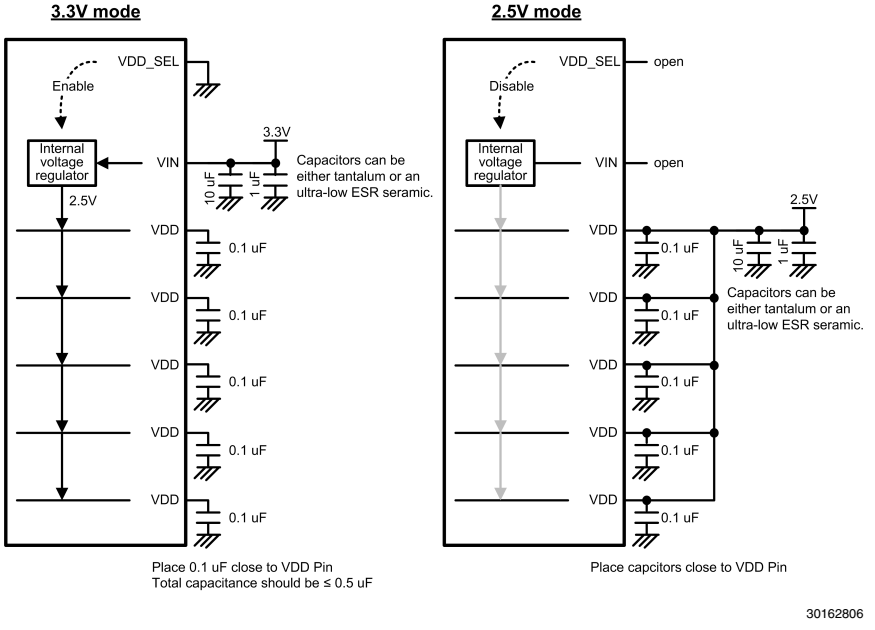


FIGURE 5. 3.3V or 2.5V Supply Connection Diagram

Table 2: Equalizer Settings

Level	EQ–D1 EQ_S1	EQ_D0 EQ_S0	EQ – 8 bits [7:0]	dB at 1.25 GHz	dB at 2.5 GHz	dB at 4 GHz	dB at 5 GHz	Suggested Use
1	0	0	0000 0000 = 0x00	2.1	3.7	4.9	5.3	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	3.4	5.8	7.9	8.7	FR4 5 inch 5–mil trace
3	0	Float	0000 0010 = 0x02	4.8	7.7	9.9	10.6	FR4 5 inch 4–mil trace
4	0	1	0000 0011 = 0x03	5.9	8.9	11.0	11.7	FR4 10 inch 5–mil trace
5	R	0	0000 0111 = 0x07	7.2	11.2	14.3	15.6	FR4 10 inch 4–mil trace
6	R	R	0001 0101 = 0x15	6.1	11.4	14.6	16.6	FR4 15 inch 4–mil trace
7	R	Float	0000 1011 = 0x0B	8.8	13.5	17.0	18.3	FR4 20 inch 4–mil trace
8	R	1	0000 1111 = 0x0F	10.2	15.0	18.5	19.7	FR4 25 to 30 inch 4–mil trace
9	Float	0	0101 0101 = 0x55	7.5	12.8	18.0	20.3	FR4 30 inch 4–mil trace
10	Float	R	0001 1111 = 0x1F	11.4	17.4	22.0	23.6	FR4 35 inch 4–mil trace
11	Float	Float	0010 1111 = 0x2F	13.0	19.7	24.4	25.8	10m, 30awg cable
12	Float	1	0011 1111 = 0x3F	14.2	21.1	25.8	27.0	10m – 12m cable
13	1	0	1010 1010 = 0xAA	13.8	21.7	27.4	29.1	
14	1	R	0111 1111 = 0x7F	15.6	23.5	29.0	30.7	
15	1	Float	1011 1111 = 0xBF	17.2	25.8	31.4	32.7	
16	1	1	1111 1111 = 0xFF	18.4	27.3	32.7	33.8	

Table 3: De-emphasis and Output Voltage Settings

Level	DEM_D1 DEM_S1	DEM_D0 DEM_S0	VOD Vp-p	DEM dB	Inner Amplitude Vp-p	Suggested Use
1	0	0	0.6	0	0.6	FR4 <5 inch 4–mil trace
2	0	R	0.8	0	0.8	FR4 <5 inch 4–mil trace
3	0	Float	0.8	- 3.5	0.55	FR4 10 inch 4–mil trace
4	0	1	0.9	0	1.0	FR4 <5 inch 4–mil trace
5	R	0	0.9	- 3.5	0.45	FR4 10 inch 4–mil trace
6	R	R	0.9	- 6	0.5	FR4 15 inch 4–mil trace
7	R	Float	1.0	0	1.0	FR4 <5 inch 4–mil trace
8	R	1	1.0	- 3.5	0.7	FR4 10 inch 4–mil trace
9	Float	0	1.0	- 6	0.5	FR4 15 inch 4–mil trace
10	Float	R	1.1	0	1.1	FR4 <5 inch 4–mil trace
11	Float	Float	1.1	- 3.5	0.7	FR4 10 inch 4–mil trace
12	Float	1	1.1	- 6	0.55	FR4 15 inch 4–mil trace
13	1	0	1.2	0	1.2	FR4 <5 inch 4–mil trace
14	1	R	1.2	- 3.5	0.8	FR4 10 inch 4–mil trace
15	1	Float	1.2	- 6	0.6	FR4 15 inch 4–mil trace
16	1	1	1.2	- 9	0.45	FR4 20 inch 4–mil trace

Table 4: Input Termination Condition with RESET, INPUT_EN and SEL0 / SEL1

RESET	INPUT_EN	SEL0 SEL1	Mode	Input_Term S_INA0 S_INA1	Input_Term S_INB0 S_INB1	Input_Term D_IN0 D_IN1
1	X	X	Low Power	High Z	High Z	High Z
0	0	X	Manual Mux Mode	50 Ω	50 Ω	50 Ω
0	R	X	Reserved	Reserved	Reserved	Reserved
0	F	0	Auto - continuous poll, DIN_B	High Z	Auto RX-Detect, output tests every 12msec until detection occcurs, input termination is high-z until detection; once detected input termination is 50 Ohm	Auto RX-Detect, output tests every 12msec until detection occcurs, input termination is high-z until detection; once detected input termination is 50 Ohm
0	F	R	Auto - continuous poll, DIN_B	High Z	Auto RX-Detect, output tests every 12msec until detection occcurs, input termination is high-z until detection; once detected input termination is 50 Ohm	Auto RX-Detect, output tests every 12msec until detection occcurs, input termination is high-z until detection; once detected input termination is 50 Ohm
0	F	F	Auto - continuous poll, DIN_A	Auto RX-Detect, output tests every 12msec until detection occcurs, input termination is high-z until detection; once detected input termination is 50 Ohm	High Z	Auto RX-Detect, output tests every 12msec until detection occcurs, input termination is high-z until detection; once detected input termination is 50 Ohm
0	F	1	Auto - continuous poll, DIN_A	Auto RX-Detect, output tests every 12msec until detection occcurs, input termination is high-z until detection; once detected input termination is 50 Ohm	High Z	Auto RX-Detect, output tests every 12msec until detection occcurs, input termination is high-z until detection; once detected input termination is 50 Ohm
0	1	X	Manual Fanout Mode	50 Ω	50 Ω	50 Ω

Table 5: Mux/Switch and FANOUT Control

SEL0	SEL1	INPUT_EN	Description of Connection Path
0	0	0	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTB0. S_OUTA0 is in IDLE (output muted). D_IN1 connects to S_OUTB1. S_OUTA1 is in IDLE (output muted).
0	0	R	Reserved
0	0	F	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTB0. S_OUTA0 is in IDLE (output muted). D_IN1 connects to S_OUTB1. S_OUTA1 is in IDLE (output muted).
0	0	1	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTB0 and S_OUTA0. D_IN1 connects to S_OUTB1 and S_OUTA1.
R	R	0	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).
R	R	R	Reserved
R	R	F	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).
R	R	1	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTB0 and S_OUTA0. D_IN1 connects to S_OUTB1 and S_OUTA1.
F	F	0	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTB0. S_OUTA0 is in IDLE (output muted). D_IN1 connects to S_OUTB1. S_OUTA1 is in IDLE (output muted).
F	F	R	Reserved
F	F	F	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTB0. S_OUTA0 is in IDLE (output muted). D_IN1 connects to S_OUTB1. S_OUTA1 is in IDLE (output muted).
F	F	1	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTB0 and S_OUTA0. D_IN1 connects to S_OUTB1 and S_OUTA1.
1	1	0	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).
1	1	R	Reserved
1	1	F	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).
1	1	1	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTA0 and S_OUTB0. D_IN1 connects to S_OUTA1 and S_OUTB1.

SMBUS Master Mode

The DS100MB203 devices support reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS100MB203 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines below. **NOTE: SEL0, SEL1 and INPUT_EN control are to be set with the external strap pins because there no register bits to configure them.**

- Set ENSMB = Float — enable the SMBUS master mode.
- The external EEPROM device address byte must be 0xA0'h and capable of 400 kHz operation at 2.5V and 3.3V supply.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is B0'h.

When tying multiple DS100MB203 devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM. Example below is for 4 device.
  U1: AD[3:0] = 0000 = 0xB0'h,
  U2: AD[3:0] = 0001 = 0xB2'h,
  U3: AD[3:0] = 0010 = 0xB4'h,
  U4: AD[3:0] = 0011 = 0xB6'h
- Use a pull-up resistor on SDA and SCL; value = 2k ohms
- Daisy-chain READEN# (pin 26) and ALL_DONE# (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  1. Tie READEN# of the 1st device in the chain (U1) to GND
  2. Tie ALL_DONE# of U1 to READEN# of U2
  3. Tie ALL_DONE# of U2 to READEN# of U3
  4. Tie ALL_DONE# of U3 to READEN# of U4
  5. Optional: Tie ALL_DONE# output of U4 to a LED to show the devices have been loaded successfully

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS100MB203 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS100MB203 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS100MB203 device.

:20000000**00001000000407002FAD4002FAD4002FAD4002FAD401805F5A8005F5A8005F5A**D8

:20002000**8005F5A800005454**0000000000000000000000000000000000000000000000000F6

:20006000000000000000000000000000000000000000000000000000000000000000000080

:20008000000000000000000000000000000000000000000000000000000000000000000060

:2000A000000000000000000000000000000000000000000000000000000000000000000040

:2000C000000000000000000000000000000000000000000000000000000000000000000020

:2000E000000000000000000000000000000000000000000000000000000000000000000000

:20004000000000000000000000000000000000000000000000000000000000000000000A0

Table 6: EEPROM Register Map with Default Value

EEPROM Address	Byte	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	0	00	CRC EN	Address Map Present	EEPROM > 256 Bytes	RES	RES	RES	RES	RES
Binary			0	0	0	0	0	0	0	0
Description	1	00	RES	RES	RES	RES	RES	RES	RES	RES
Binary			0	0	0	0	0	0	0	0
Description	2	10	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Binary			0	0	0	1	0	0	0	0
Description	3	00	PWDN_ch7	PWDN_ch6	PWDN_ch5	PWDN_ch4	PWDN_ch3	PWDN_ch2	PWDN_ch1	PWDN_ch0
Binary			0	0	0	0	0	0	0	0
Description	4	00	RES	RES	RES	RES	Ovrd_RESET	RES	RES	RES
Binary			0	0	0	0	0	0	0	0
Description	5	04	RES	RES	RES	RES	RES	rxdet_btb_en	RES	RES
Binary			0	0	0	0	0	1	0	0
Description	6	07	RES	Ovrd_RX_DET	Ovrd_MODE	RES	RES	rx_delay_sel_2	rx_delay_sel_1	rx_delay_sel_0
Binary			0	0	0	0	0	1	1	1
Description	7	00	RD_delay_sel_3	RD_delay_sel_2	RD_delay_sel_1	RD_delay_sel_0	RES	RES	ch0_RXDET_1	ch0_RXDET_0
Binary			0	0	0	0	0	0	0	0
Description	8	2F	ch0_BST_7	ch0_BST_6	ch0_BST_5	ch0_BST_4	ch0_BST_3	ch0_BST_2	ch0_BST_1	ch0_BST_0
Binary			0	0	1	0	1	1	1	1
Description	9	AD	ch0_RES	ch0_RES	ch0_RES_2	ch0_RES_1	ch0_RES_0	ch0_RES_2	ch0_RES_1	ch0_RES_0
Binary			1	0	1	0	1	1	0	1
Description	10	40	ch0_RES_2	ch0_RES_1	ch0_RES_0	ch0_Slow	ch0_RES_1	ch0_RES_0	ch0_RES_1	ch0_RES_0
Binary			0	1	0	0	0	0	0	0
Description	11	02	ch1_RES	ch1_RES	ch1_RXDET_1	ch1_RXDET_0	ch1_BST_7	ch1_BST_6	ch1_BST_5	ch1_BST_4
Binary			0	0	0	0	0	0	1	0
Description	12	FA	ch1_BST_3	ch1_BST_2	ch1_BST_1	ch1_BST_0	ch1_Sel_scp	ch1_Sel_MODE	ch1_RES_2	ch1_RES_1
Binary			1	1	1	1	1	0	1	0
Description	13	D4	ch1_RES_0	ch1_VOD_2	ch1_VOD_1	ch1_VOD_0	ch1_DEM_2	ch1_DEM_1	ch1_DEM_0	ch1_Slow
Binary			1	1	0	1	0	1	0	0
Description	14	00	ch1_RES_1	ch1_RES_0	ch1_RES_1	ch1_RES_0	ch2_RES	ch2_RES	ch2_RXDET_1	ch2_RXDET_0
Binary			0	0	0	0	0	0	0	0

Description	15	2F	ch2_BST_7	ch2_BST_6	ch2_BST_5	ch2_BST_4	ch2_BST_3	ch2_BST_2	ch2_BST_1	ch2_BST_0
Binary			0	0	1	0	1	1	1	1
Description	16	AD	ch2_RES	ch2_RES	ch2_RES_2	ch2_RES_1	ch2_RES_0	ch2_RES_2	ch2_RES_1	ch2_RES_0
Binary			1	0	1	0	1	1	0	1
Description	17	40	ch2_RES_2	ch2_RES_1	ch2_RES_0	ch2_Slow	ch2_RES_1	ch2_RES_0	ch2_RES_1	ch2_RES_0
Binary			0	1	0	0	0	0	0	0
Description	18	02	ch3_RES	ch3_RES	ch3_RXDET_1	ch3_RXDET_0	ch3_BST_7	ch3_BST_6	ch3_BST_5	ch3_BST_4
Binary			0	0	0	0	0	0	1	0
Description	19	FA	ch3_BST_3	ch3_BST_2	ch3_BST_1	ch3_BST_0	ch3_Sel_scp	ch3_Sel_MODE	ch3_RES_2	ch3_RES_1
Binary			1	1	1	1	1	0	1	0
Description	20	D4	ch3_RES_0	ch3_VOD_2	ch3_VOD_1	ch3_VOD_0	ch3_DEM_2	ch3_DEM_1	ch3_DEM_0	ch3_Slow
Binary			1	1	0	1	0	1	0	0
Description	21	01	ch3_RES_1	ch3_RES_0	ch3_RES_1	ch3_RES_0	ovrd_fast_idle	en_h_idle_th_n	en_h_idle_th_s	en_fast_idle_n
Binary			0	0	0	0	0	0	0	1
Description	22	80	en_fast_idle_s	eqsd_mgain_n	eqsd_mgain_s	ch4_RES	ch4_RES	ch4_RXDET_1	ch4_RXDET_0	ch4_BST_7
Binary			1	0	0	0	0	0	0	0
Description	23	5F	ch4_BST_6	ch4_BST_5	ch4_BST_4	ch4_BST_3	ch4_BST_2	ch4_BST_1	ch4_BST_0	ch4_Sel_scp
Binary			0	1	0	1	1	1	1	1
Description	24	5A	ch4_Sel_MODE	ch4_RES_2	ch4_RES_1	ch4_RES_0	ch4_VOD_2	ch4_VOD_1	ch4_VOD_0	ch4_DEM_2
Binary			0	1	0	1	1	0	1	0
Description	25	80	ch4_DEM_1	ch4_DEM_0	ch4_Slow	ch4_RES_1	ch4_RES_0	ch4_RES_1	ch4_RES_0	ch5_RES
Binary			1	0	0	0	0	0	0	0
Description	26	05	ch5_RES	ch5_RES	ch5_RES	ch5_RES	ch5_RES	ch5_RES	ch5_RES	ch5_RES
Binary			0	0	0	0	0	1	0	1
Description	27	F5	ch5_RES	ch5_RES	ch5_RES	ch5_Sel_scp	ch5_Sel_MODE	ch5_RES_2	ch5_RES_1	ch5_RES_0
Binary			1	1	1	1	0	1	0	1
Description	28	A8	ch5_VOD_2	ch5_VOD_1	ch5_VOD_0	ch5_DEM_2	ch5_DEM_1	ch5_DEM_0	ch5_Slow	ch5_RES_1
Binary			1	0	1	0	1	0	0	0
Description	29	00	ch5_RES_0	ch5_RES_1	ch5_RES_0	ch6_RES	ch6_RES	ch6_RXDET_1	ch6_RXDET_0	ch6_BST_7
Binary			0	0	0	0	0	0	0	0
Description	30	5F	ch6_BST_6	ch6_BST_5	ch6_BST_4	ch6_BST_3	ch6_BST_2	ch6_BST_1	ch6_BST_0	ch6_Sel_scp
Binary			0	1	0	1	1	1	1	1
Description	31	5A	ch6_Sel_MODE	ch6_RES_2	ch6_RES_1	ch6_RES_0	ch6_VOD_2	ch6_VOD_1	ch6_VOD_0	ch6_DEM_2
Binary			0	1	0	1	1	0	1	0

Description	32	80	ch6_DEM_1	ch6_DEM_0	ch6_Slow	ch6_RES_1	ch6_RES_0	ch6_RES_1	ch6_RES_0	ch7_RES
Binary			1	0	0	0	0	0	0	0
Description	33	05	ch7_RES	ch7_RES	ch7_RES	ch7_RES	ch7_RES	ch7_RES	ch7_RES	ch7_RES
Binary			0	0	0	0	0	1	0	1
Description	34	F5	ch7_RES	ch7_RES	ch7_RES	ch7_Sel_scp	ch7_Sel_MODE	ch7_RES_2	ch7_RES_1	ch7_RES_0
Binary			1	1	1	1	0	1	0	1
Description	35	A8	ch7_VOD_2	ch7_VOD_1	ch7_VOD_0	ch7_DEM_2	ch7_DEM_1	ch7_DEM_0	ch7_Slow	ch7_RES_1
Binary			1	0	1	0	1	0	0	0
Description	36	00	ch7_RES_0	ch7_RES_1	ch7_RES_0	iph_dac_ns_1	iph_dac_ns_0	ipp_dac_ns_1	ipp_dac_ns_0	ipp_dac_1
Binary			0	0	0	0	0	0	0	0
Description	37	00	ipp_dac_0	RD23_67	RD01_45	RD_PD_ovrd	RD_Sel_test	RD_RESET_ovrd	PWDB_input_DC	DEM_VOD_ovrd
Binary			0	0	0	0	0	0	0	0
Description	38	54	DEM_ovrd_N2	DEM_ovrd_N1	DEM_ovrd_N0	VOD_ovrd_N2	VOD_ovrd_N1	VOD_ovrd_N0	SPARE0	SPARE1
Binary			0	1	0	1	0	1	0	0
Description	39	54	DEM__ovrd_S2	DEM__ovrd_S1	DEM_ovrd_S0	VOD_ovrd_S2	VOD_ovrd_S1	VOD_ovrd_S0	SPARE0	SPARE1
Binary			0	1	0	1	0	1	0	0

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB = 1kΩ to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS100MB203 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, the DS100MB203 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses.

Table 7: Device Slave Address Bytes

AD[3:0] Settings	Address Bytes (HEX)
0000	B0
0001	B2
0010	B4
0011	B6
0100	B8
0101	BA
0110	BC
0111	BE
1000	C0
1001	C2
1010	C4
1011	C6
1100	C8
1101	CA
1110	CC
1111	CE

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Please see SMBus Register Map Table for more information.

Table 8: SMBUS Slave Mode Register Map

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x00	Observation, SMBus Reset	7	Reserved	R/W	0x00	Set bit to 0.
		6:3	Address Bit AD[3:0]	R		Observation of AD[3:0] bit [6]: AD3 [5]: AD2 [4]: AD1 [3]: AD0
		2	EEPROM Read Done	R		1: Device completed the read from external EEPROM.
		1	Block Reset	R/W		1: Block bit 0 from resetting the registers; self clearing.
		0	Reset	R/W		SMBus Reset 1: Reset registers to default value; self clearing.
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel [7]: CH7 (NC – S_OUTB1) [6]: CH6 (D_IN1 – S_OUTA1) [5]: CH5 (NC – S_OUTB0) [4]: CH4 (D_IN0 – S_OUTA0) [3]: CH3 (D_OUT1 – S_INB1) [2]: CH2 (NC – S_INA1) [1]: CH1 (D_OUT0 – S_INB0) [0]: CH0 (NC – S_INA0) 00'h = all channels enabled FF'h = all channels disabled; device in low power state Note: override RESET pin in Reg_02.
0x02	Override RESET Control	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Override RESET			1: Block RESET pin control; use Reg_01 to configure. 0: Allow RESET pin control.
0x05	Slave Mode CRC Bits	7:0	CRC bits	R/W	0x00	CRC bits [7:0]
0x06	Slave CRC Control	7:5	Reserved	R/W	0x10	Set bits to 0.
		4	Reserved			Set bit to 1.
		3	Slave CRC			1: Disables the slave CRC mode 0: Enables the slave CRC mode Note: In order to change VOD, DEM and EQ of the channels in slave mode, set bit to 1 to disable the CRC.
		2:0	Reserved			Set bits to 0.
0x08	Override RXDET, MODE	7:4	Reserved	R/W	0x00	Set bits to 0.
		3	Override RXDET			1: Block RXDET control; use register to configure. 0: Allow RXDET control.
		2	Override MODE			1: Block MODE pin control; use register to configure. 0: Allow MODE pin control
		1:0				Set bits to 0.

0x0E	CH0 - S_INA0 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x0F	CH0 - S_INA0 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See *Table 2: Equalizer Settings*.
0x10	Reserved	7:0	Reserved	R/W	0xAD	
0x11	Reserved	7:0	Reserved	R/W	0x02	
0x12	Reserved	7:0	Reserved	R/W	0x00	
0x15	CH1 - S_INB0 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x16	CH1 - S_INB0 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See *Table 2: Equalizer Settings*.
0x17	CH1 - D_OUT0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V

0x18	CH1 - D_OUT0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH1 - CHB1. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x19	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x1C	CH2 - S_INA1 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0				Set bits to 0.
0x1D	CH2 - S_INA1 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See .
0x1E	Reserved	7:0	Reserved	R/W	0xAD	
0x1F	Reserved	7:0	Reserved	R/W	0x02	
0x20	Reserved	7:0	Reserved	R/W	0x00	
0x23	CH3 - S_INB1 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x24	CH3 - S_INB1 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See .

0x25	CH3 - D_OUT1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V
0x26	CH3 - D_OUT1 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH1 - CHB1. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x27	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x2B	CH4 - D_IN0 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x2C	CH4 - D_IN0 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See *Table 2: Equalizer Settings*.

0x2D	CH4 - S_OUTA0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V
0x2E	CH4 - S_OUTA0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x2F	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x32	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x33	Reserved	7:0	Reserved	R/W	0x2F	
0x34	CH5 - S_OUTB0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V

0x35	CH5 - S_OUTB0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x36	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x39	CH6 - D_IN1 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x3A	CH6 - D_IN1 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See *Table 2: Equalizer Settings*.
0x3B	CH6 - S_OUTA1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V

0x3C	CH6 - S_OUTA1 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x3D	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x40	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x41	Reserved	7:0	Reserved	R/W	0x2F	EQ Control - total of 256 levels. See *Table 2: Equalizer Settings*.
0x42	CH7 - S_OUTB1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V
0x43	CH7 - S_OUTB1 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET. CH7 - CHA3. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x44	Reserved	7:4	Reserved	R/W	0x00	Set bits to 0.
0x51	Device ID	7:5	VERSION	R	0x46	010'b
		4:0	ID			00110'b

0x5E	Override SEL1, SEL0 and INPUT_EN	7:3	Reserved	R/W	0x00	Set bits to 0.
		2	Override SEL1 pin			1: Block SEL1 pin control; use Reg_5F to configure. 0: Allow SEL1 pin control
		1	Override SEL0 pin			1: Block SEL0 pin control; use Reg_5F to configure. 0: Allow SEL0 pin control
		0	Override INPUT_EN pin			1: Block INPUT_EN pin control; use Reg_5F to configure. 0: Allow INPUT_EN pin control
0x5F	Control SEL1, SEL0 and INPUT_ENl	7:6	SEL1 Control	R/W	0x00	Select for Lane 1. 00: 0 - selects input S_INB1+/-, output S_OUTB1+/-. 01: 20kΩ to GND - selects input S_INB1+/-, output S_OUTA1+/- 10: FLOAT - selects input S_INA1+/-, output S_OUTB1+/- 11: 1 - selects input S_INA1+/-, output S_OUTA1+/-.
		5:4	SEL0 Control			Select for Lane 0. 00: 0 - selects input S_INB0+/-, output S_OUTB0+/-. 01: 20kΩ to GND - selects input S_INB0+/-, output S_OUTA0+/- 10: FLOAT - selects input S_INA0+/-, output S_OUTB0+/- 11: 1 - selects input S_INA0+/-, output S_OUTA0+/-.
		3:2	INPUT_EN Control			00: 0 - Normal Operation, FANOUT is disabled, use SEL0/1 to select the A or B input/output (see SEL0/1 pin), input always enabled with 50 ohms. 01: 20kΩ to GND - Reserved. 10: FLOAT - AUTO - Use RX Detect, SEL0/1 to determine which input or output to enable, FANOUT is disable. 11: 1 - Normal Operation, FANOUT is enabled (both S_OUT0/1 are ON). Input always enabled with 50 ohms.
		1:0	Reserved			Set bits to 0.

Applications Information

GENERAL RECOMMENDATIONS

The DS100MB203 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

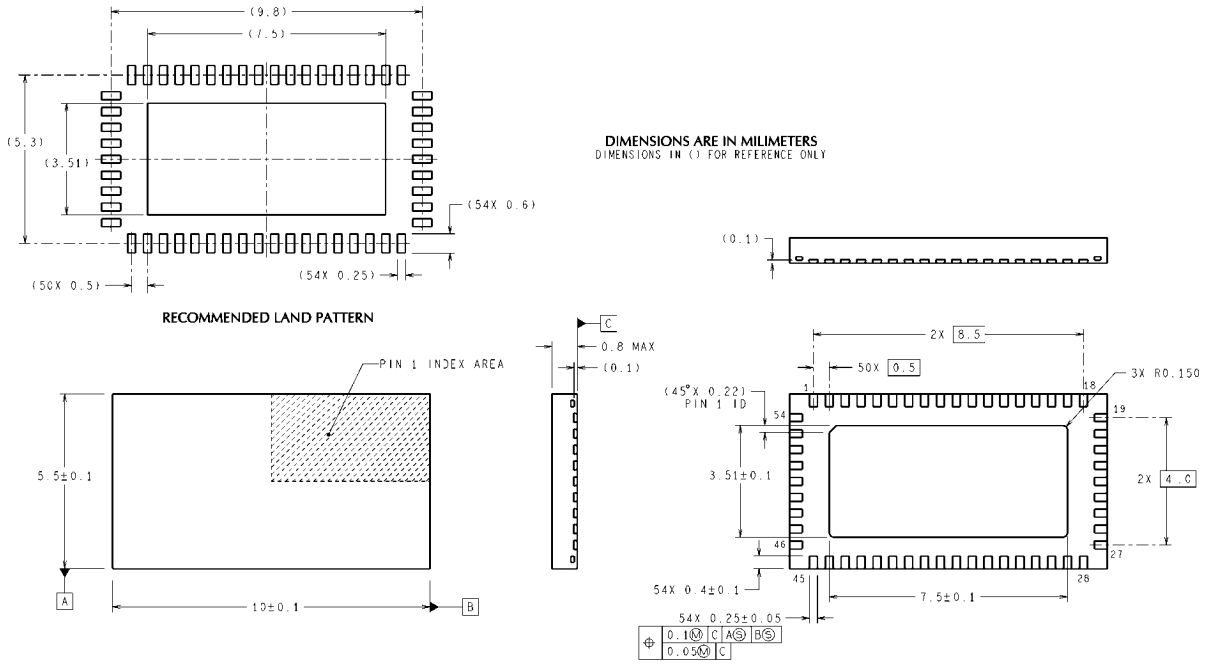
PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS100MB203 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS100MB203. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

Physical Dimensions inches (millimeters) unless otherwise noted



SQA54A (Rev B)

Order Number DS100MB203SQ (Tape and Reel 2000 units)
Order Number DS100MB203SQE (Tape and Reel 250 units)
Package Number SQA54A
(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

Notes

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