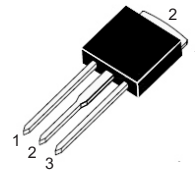
TRIACs, 4A

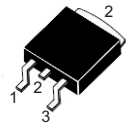
Snubberless, Logic Level and Standard

MAIN FEATURES

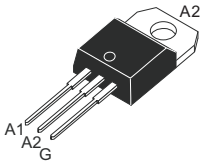
SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	4	A
V_{DRM}/V_{RRM}	600 to 1000	V
$I_{GT(Q1)}$	5 to 50	mA



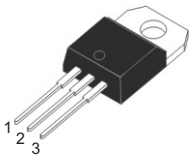
TO-251 **(I-PAK)**
(4TxxF)



TO-252 **(D-PAK)**
(4TxxG)

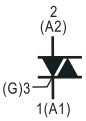


TO-220AB (**non-Insulated**)
(4TxxA)



TO-220AB **(Insulated)**
(4TxxAI)

ITO-220AB
(4TxxAF)



DESCRIPTION

The 4T triac series is suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control operation in light dimmers, motor speed controllers,...

The snubberless and logic level versions are specially recommended for use on inductive loads, thanks to their high commutation performances.

By using an internal ceramic pad, the 4T series provides voltage insulated tab (rated at 2500V_{RMS}) complying with UL standards (File ref. :E320098)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current (full sine wave)	$I_{T(RMS)}$	TO-251/TO-252/TO-220AB	T_c = 105°C	4	A
		TO-220AB insulated	T_c = 100°C		
Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	I_{TSM}	F =50 Hz	t = 20 ms	35	A
		F =60 Hz	t = 16.7 ms	38	
I^2t Value for fusing	I^2t	t_p = 10 ms		6	A^2s
Critical rate of rise of on-state current $I_G = 2xI_{GT}$, $t_r \leq 100ns$	dI/dt	F =100 Hz	T_j =125°C	50	A/µs
Peak gate current	I_{GM}	T_p =20 µs	T_j =125°C	4	A
Average gate power dissipation	$P_{G(AV)}$	T_j =125°C		1	W
Storage temperature range	T_{stg}			- 40 to + 150	°C
Operating junction temperature range	T_j			- 40 to + 125	

◎ ELECTRICAL CHARACTERISTICS (T_J= 25 ºC unless otherwise specified)

SNUBBERLESS and Logic level (3 quadrants)

SYMBOL	TEST CONDITIONS	QUADRANT		4Txxxx			Unit
				TW	SW	CW	
I_{GT}(1)	V_D = 12 V, R_L = 30Ω	I - II - III	MAX.	05	10	35	mA
V_{GT}		I - II - III	MAX.	1.3			V
V_{GD}	$V_D = V_{DRM}$, R_L = 3.3KΩ T_j = 125°C	I - II - III	MIN.	0.2			V
I_H(2)	I_T = 200 mA		MAX.	10	15	35	mA
I_L	I_G = 1.2 I_{GT}	I - III	MAX.	10	25	50	mA
		II		15	30	60	
dV/dt(2)	V_D = 67% V_{DRM}, gate open , T_j = 125°C		MIN.	20	40	400	V/µs
(dI/dt)c(2)	(dV/dt)c = 0.1 V/µs	T_j = 125°C	MIN.	1.8	2.7	-	A/ms
	(dV/dt)c = 10 V/µs	T_j = 125°C		0.9	2.0	-	
	Without snubber	T_j = 125°C		-	-	2.5	

◎ ELECTRICAL CHARACTERISTICS (T_J= 25 ºC unless otherwise specified)

Standard (4 quadrants)

SYMBOL	TEST CONDITIONS	QUADRANT		4Txxxx				UNIT
				T	D	S	A	
I_{GT}(1)	V_D = 12 V, R_L = 30Ω	I - II - III	MAX.	5	5	10	10	mA
		IV		5	10	10	25	
V_{GT}		ALL		1.3				V
V_{GD}	$V_D = V_{DRM}$, R_L = 3.3KΩ, T_j = 125°C	ALL		0.2				V
I_H(2)	I_T = 200 mA		MAX.	5	10	10	25	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	MAX.	10	10	15	25	mA
		II		15	20	25	40	
dV/d_t(2)	V_D = 67% V_{DRM}, gate open, T_j = 125°C		MIN.	5	5	10	50	V/µs
(dV/dt)c(2)	(dI/dt)c = 1.7 A/ms, T_j = 125°C		MIN.	0.5	1	2	5	

STATIC CHARACTERISTICS

SYMBOL	TEST CONDITIONS			VALUE	UNIT
V_{TM}(2)	I_{TM} = 5.5 A, t_P = 380 µs	T_j = 25°C	MAX.	1.55	V
V_{TO}(2)	Threshold voltage	T_j = 125°C	MAX.	0.85	
R_D(2)	Dynamic resistance	T_j = 125°C	MAX.	100	mΩ
I_{DRM} I_{RRM}	$V_D = V_{DRM}$ $V_R = V_{RRM}$	T_j = 25°C	MAX.	5	µA
		T_j = 125°C		1	mA

Note 1: Minimum I_{GT} is guaranted at 5% of I_{GT} max.
Note 2: For both polarities of A2 referenced to A1.

THERMAL RESISTANCE

SYMBOL				VALUE	UNIT
$R_{th(j-c)}$	Junction to case (AC)		TO-220AB,TO-251, TO-252	2.6	°C/W
			TO-220AB Insulated, ITO-220AB	4.0	
$R_{th(j-a)}$	Junction to ambient	S = 0.5 cm^2	TO-252	70	°C/W
			TO-220AB Insulated, TO-220AB, ITO-220AB	60	
			TO-251	100	

S = Copper surface under tab.

PRODUCT SELECTOR

PART NUMBER	VOLTAGE (xx)			SENSITIVITY	TYPE	PACKAGE
	600 V	800 V	1000 V			
4TxxA-CW/4TxxAI-CW	V	V	V	35 mA	Snubberless	TO-220AB
4TxxA-S/4TxxAI-S	V	V	V	10 mA	Standard	TO-220AB
4TxxA-A/4TxxAI-A	V	V	V	10 mA	Standard	TO-220AB
4TxxA-SW/4TxxAI-SW	V	V	V	10 mA	Logic level	TO-220AB
4TxxA-T/4TxxAI-T	V	V	V	5 mA	Standard	TO-220AB
4TxxA-D/4TxxAI-D	V	V	V	5 mA	Standard	TO-220AB
4TxxA-TW/4TxxAI-TW	V	V	V	5 mA	Logic level	TO-220AB
4TxxF-CW	V	V	V	35 mA	Snubberless	I-PAK
4TxxG-CW	V	V	V	35 mA	Snubberless	D-PAK
4TxxF-SW	V	V	V	10 mA	Logic level	I-PAK
4TxxG-SW	V	V	V	10 mA	Logic level	D-PAK
4TxxF-TW	V	V	V	5 mA	Logic level	I-PAK
4TxxG-TW	V	V	V	5 mA	Logic level	D-PAK
4TxxF-T/D/S/A	V	V	V	5 /5/10/10 mA	Standard	I-PAK
4TxxG-T/D/S/A	V	V	V	5 /5/10/10 mA	Standard	D-PAK
4TxxAF-CW	V	V	V	35 mA	Snubberless	ISOWAT TO-220AB
4TxxAF-SW	V	V	V	10 mA	Logic level	ISOWAT TO-220AB
4TxxAF-TW	V	V	V	5 mA	Logic level	ISOWAT TO-220AB
4TxxAF-D	V	V	V	5 mA	Standard	ISOWAT TO-220AB
4TxxAF-A	V	V	V	10 mA	Standard	ISOWAT TO-220AB

ORDERING INFORMATION

ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
4TxxA-yy	4TxxA-yy	TO-220AB	2.0g	50	Tube
4TxxAI-yy	4TxxAI-yy	TO-220AB (insulated)	2.3g	50	Tube
4TxxF-yy	4TxxF-yy	TO-251(I-PAK)	0.40g	80	Tube
4TxxG-yy	4TxxG-yy	TO-252(D-PAK)	0.38g	80	Tube
4TxxAF-yy	4TxxAF-yy	ISOWAT TO-220AB	2.5g	50	Tube

Note: xx = voltage, yy = sensitivity

ORDERING INFORMATION SCHEME

4 T 06 A - CW

Current

4 = 4A

Triac series

Voltage

06 = 600V
08 = 800V
10 = 1000V

Package type

A = TO-220AB (non-insulated)
AI = TO-220AB (insulated)
AF= TO-220F(ISOWAT TO-220AB, insulated)
F = TO-251 (I-PAK)
G = TO-252 (D-PAK)

I_{GT} Sensitivity

T = 5mA Standard
D = 5mA Standard
S = 10mA Standard
A = 10mA Standard
CW = 35mA Snubberless
TW = 5mA Logic Level
SW = 10mA Logic Level

Fig.1 Maximum power dissipation versus RMS on-state current (full cycle)

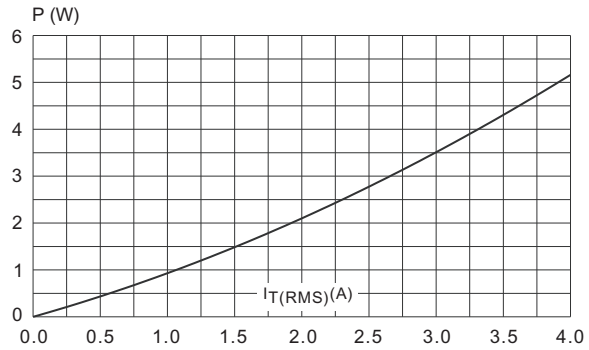


Fig.2 RMS on-state current versus case temperature (full cycle)

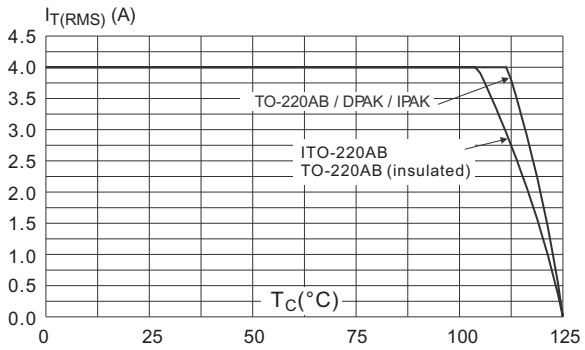


Fig.3 RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm)(full cycle)

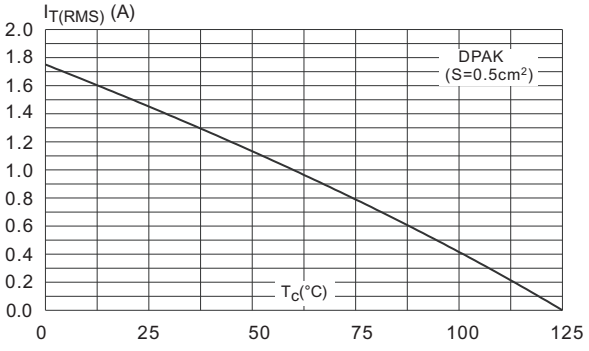


Fig.4 Relative variation of thermal impedance versus pulse duration.

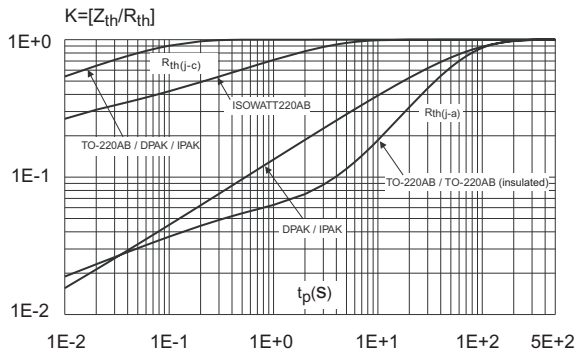


Fig.5 On-state characteristics (maximum values).

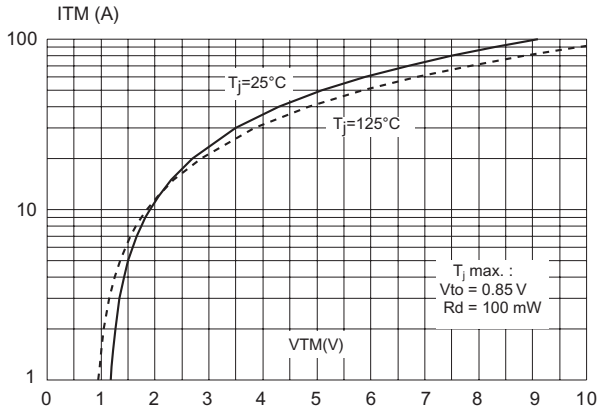


Fig.6 Surge peak on-state current versus number of cycles.

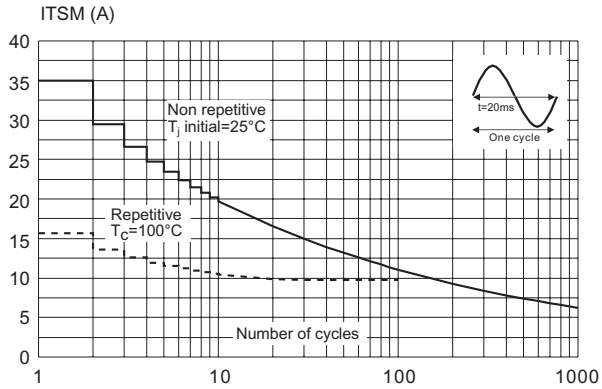


Fig.7 Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10ms. and corresponding value of I^2t.

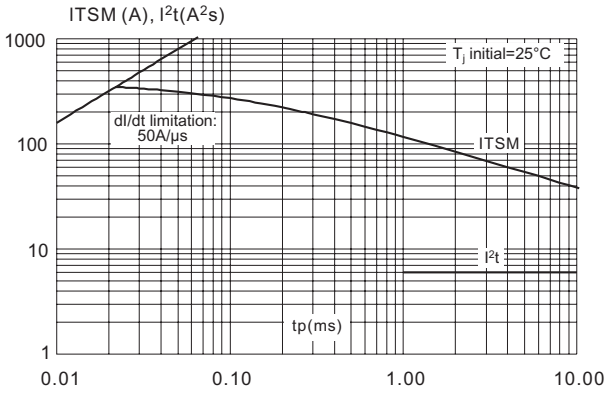


Fig.8 Relative variation of gate trigger current,holding current and latching current versus junction temperature (typical values).

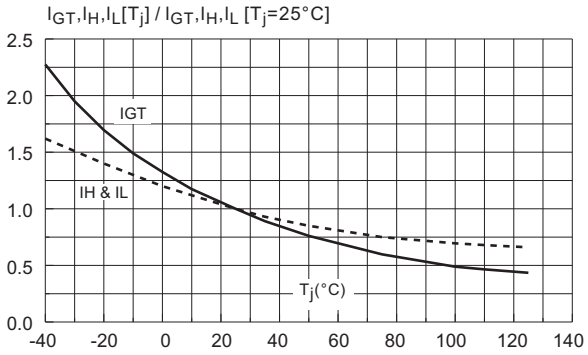


Fig.9 Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values).

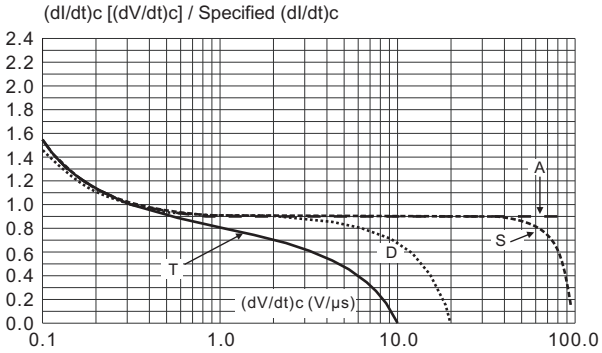


Fig.10 Relative variation of critical rate of decrease of main current versus junction temperature

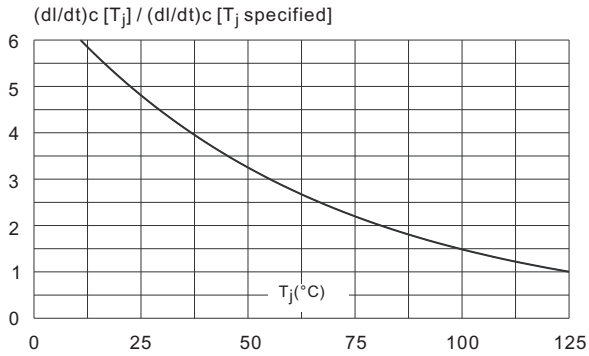
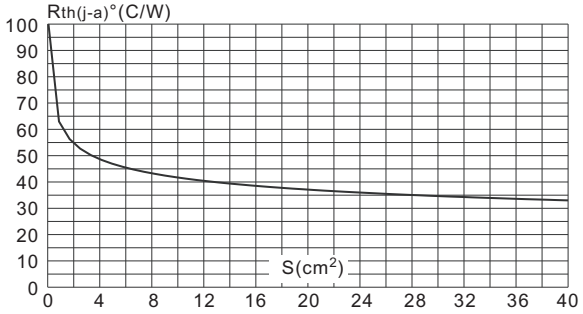
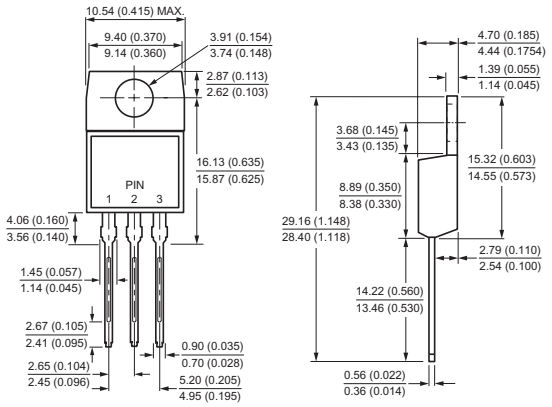


Fig.11 DPAK thermal resistance junction to ambient versus copper surface under tab (priented circuit board Fr4, copper thickness:35 µm)

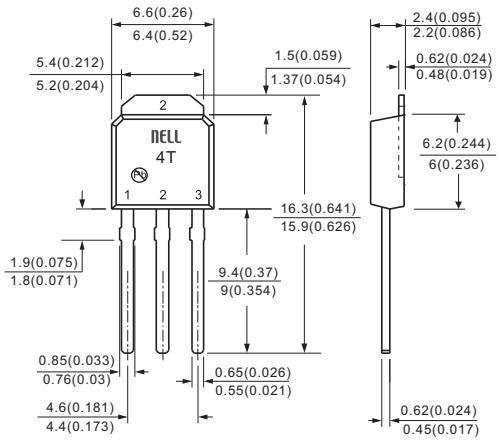


Case Style

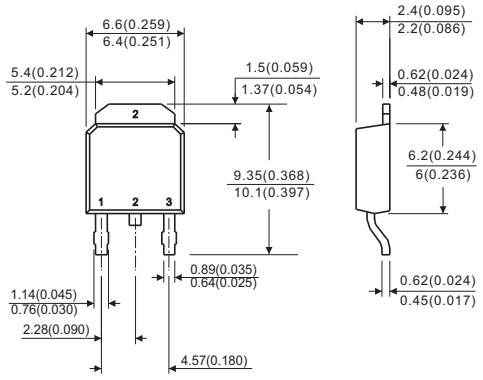
TO-220AB

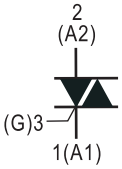


TO-251 (I-PAK)



TO-252 (D-PAK)

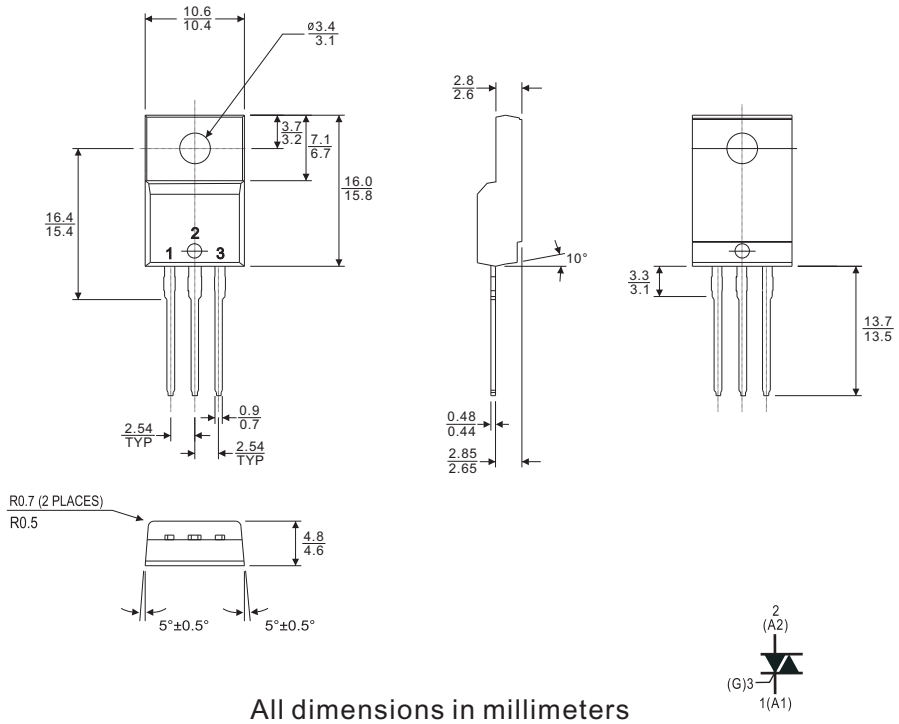




All dimensions in millimeters(inches)

Case Style

ITO-220AB



All dimensions in millimeters