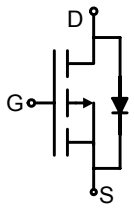
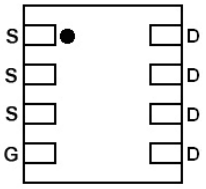
DESCRIPTION

The SSFN3313 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge .This device is suitable for use as a load switch or in PWM applications.



Schematic diagram



Marking and pin Assignment



DFN3×3-8L BOTTOM VIEW

GENERAL FEATURES

- V_{DS} =-30V,I_D =-8A
  $R_{DS(ON)}$ < 25mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$ < 14mΩ @ V_{GS}=-10V
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
SSFN3313	SSFN3313	DFN3x3-8L	-	-	-

ABSOLUTE MAXIMUM RATINGS(TA=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±25	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I_D(25℃)	-8	A
	I_D(70℃)	-6	A
	I_{DM}	-45	A
Maximum Power Dissipation	P_D	3.1	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

THERMAL CHARACTERISTICS

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	40	℃/W

ELECTRICAL CHARACTERISTICS (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	μA

Gate-Body Leakage Current	I_{GSS}	V_{GS}=±25V,V_{DS}=0V			±100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.7	-2.2	-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-7A		13	17	mΩ
		V_{GS}=-10V, I_D=-9A		11	14	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-10A		18		S
DYNAMIC CHARACTERISTICS (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz		1500		PF
Output Capacitance	C_{oss}			300		PF
Reverse Transfer Capacitance	C_{rss}			182		PF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=-15V,V_{GS}=-10V,R_{GEN}=3Ω I_D=1A		12		nS
Turn-on Rise Time	t_r			11		nS
Turn-Off Delay Time	$t_{d(off)}$			25		nS
Turn-Off Fall Time	t_f			10		nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-10A,V_{GS}=-10V		22		nC
Gate-Source Charge	Q_{gs}			7		nC
Gate-Drain Charge	Q_{gd}			4.5		nC
Body Diode Reverse Recovery Time	T_{rr}	I_F=-10A, dI/dt=100A/μs		29		nS
Body Diode Reverse Recovery Charge	Q_{rr}			15		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-1A		-0.74	-1	V

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on 1in^2 FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

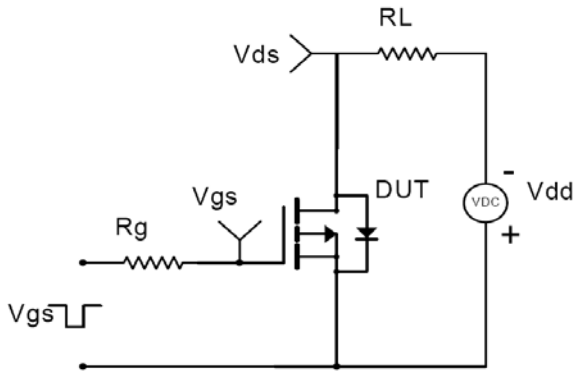


Figure 1:Switching Test Circuit

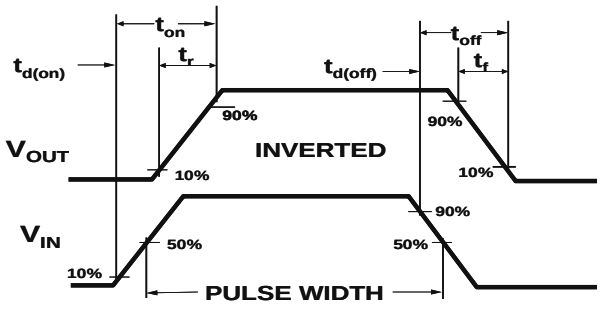


Figure 2:Switching Waveforms

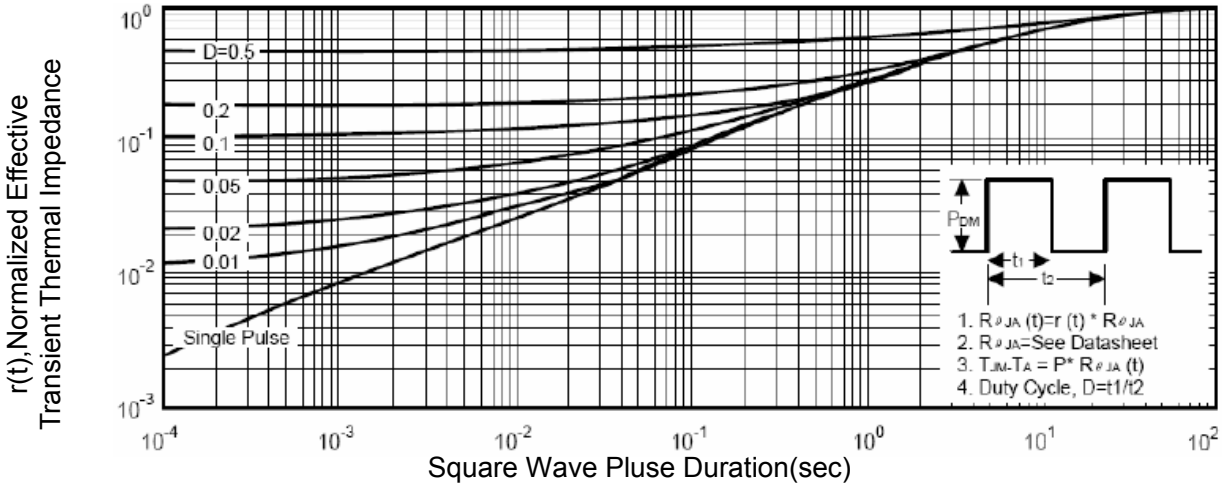
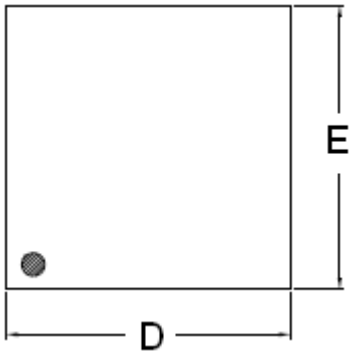
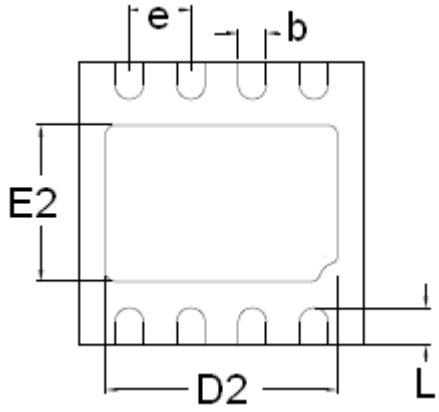


Figure 3 Normalized Maximum Transient Thermal Impedance

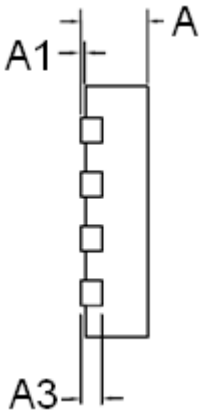
DFN3×3-8L PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W： VERY VERY THIN		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.2REF.		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
b	0.25	0.30	0.35
L	0.30	0.40	0.50
D2	2.30	2.45	2.55
E2	2.50	1.65	1.75
e	0.65BSC		

NOTES：

1. Dimensions are inclusive of plating
2. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
3. Dimension L is measured in gauge plane.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact

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