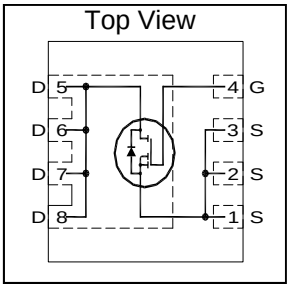
V_{DSS}	30	V
V_{GS} max	±20	V
$R_{DS(on)}$ max (@ V_{GS} = 10V)	6.6	mΩ
(@ V_{GS} = 4.5V)	9.9	
Qg (typical)	9.3	nC
I_D (@$T_{C\ (Bottom)}$ = 25°C)	25⑤	A

HEXFET® Power MOSFET





Applications

- Charge and Discharge Switch for Notebook PC Battery Application
- System/Load Switch
- Control MOSFET for synchronous buck converter

Features		Benefits
Low Thermal Resistance to PCB (<3.8°C/W)		Enable better Thermal Dissipation
Low Profile (<1.2mm)		Increased Power Density
Industry-Standard Pinout	results in	Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques	⇒	Easier Manufacturing
RoHS Compliant, Halogen-Free		Environmentally Friendlier
MSL1, Consumer Qualification		Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFHM8330PbF	PQFN 3.3 mm x 3.3 mm	Tape and Reel	4000	IRFHM8330TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	16	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	13	
I_D @ $T_{C(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V	55⑤⑥	
I_D @ $T_{C(Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V	35⑤⑥	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Source Bonding Technology Limited)	25⑥	
I_{DM}	Pulsed Drain Current	210⑦	
P_D @T_A = 25°C	Power Dissipation ④	2.7	W
P_D @$T_{C(Bottom)}$ = 25°C	Power Dissipation	33	
	Linear Derating Factor	0.021	W/°C
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Notes ① through ⑦ are on page 9

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	23	—	mV/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.3	6.6	mΩ	V_{GS} = 10V, I_D = 20A ②
		—	7.7	9.9		V_{GS} = 4.5V, I_D = 16A ②
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	V_{DS} = V_{GS}, I_D = 25µA
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-6.3	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		—	—	150		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	61	—	—	S	V_{DS} = 10V, I_D = 20A
Q_g	Total Gate Charge	—	20	—	nC	V_{GS} = 10V, V_{DS} = 15V, I_D = 20A
Q_g	Total Gate Charge	—	9.3	14	nC	V_{DS} = 15V V_{GS} = 4.5V I_D = 20A
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	2.7	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	1.6	—		
Q_{gd}	Gate-to-Drain Charge	—	2.5	—		
Q_{godr}	Gate Charge Overdrive	—	2.5	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	4.1	—		
Q_{oss}	Output Charge	—	7.1	—	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	—	1.8	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	9.2	—	ns	V_{DD} = 15V, V_{GS} = 4.5V I_D = 20A R_G=1.8Ω
t_r	Rise Time	—	15	—		
$t_{d(off)}$	Turn-Off Delay Time	—	10	—		
t_f	Fall Time	—	5.7	—		
C_{iss}	Input Capacitance	—	1450	—	pF	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	250	—		
C_{rss}	Reverse Transfer Capacitance	—	110	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ①	—	42	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	25⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	210⑦		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 20A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	—	14	21	ns	T_J = 25°C, I_F = 20A, V_{DD} = 15V
Q_{rr}	Reverse Recovery Charge	—	23	35	nC	di/dt = 390A/µs ②

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ③	—	3.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ③	—	42	
$R_{\theta JA}$	Junction-to-Ambient ④	—	47	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ④	—	32	

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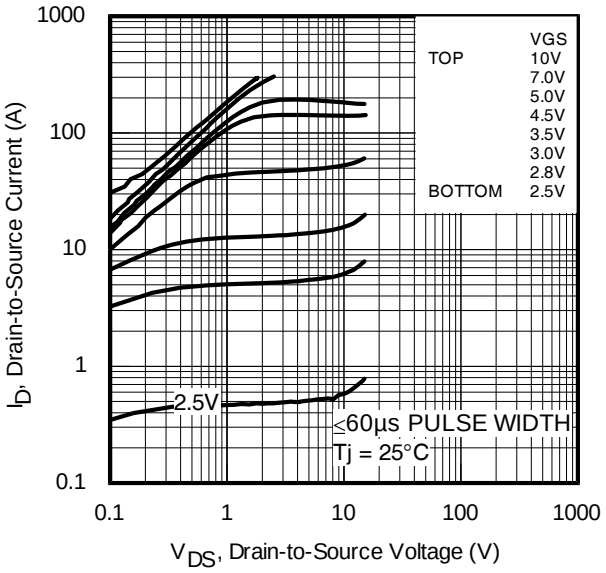


Fig 1. Typical Output Characteristics

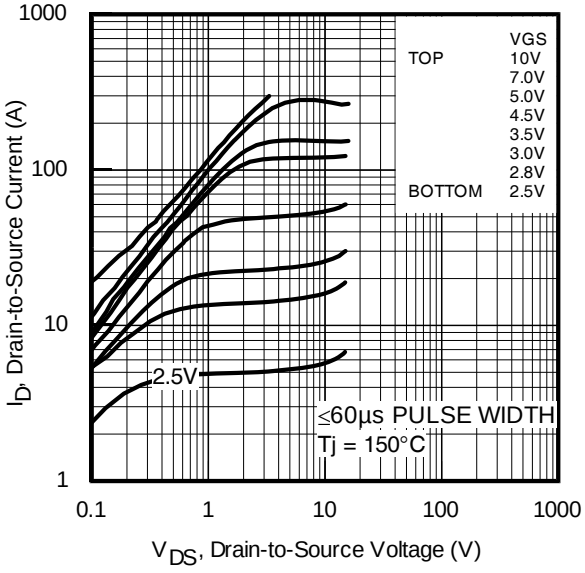


Fig 2. Typical Output Characteristics

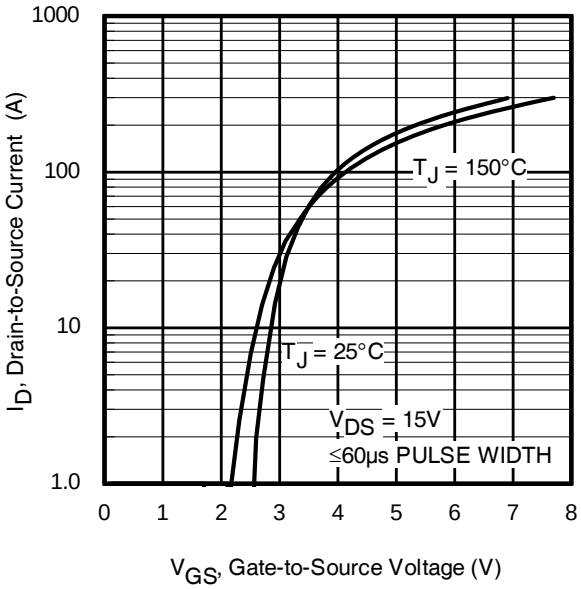


Fig 3. Typical Transfer Characteristics

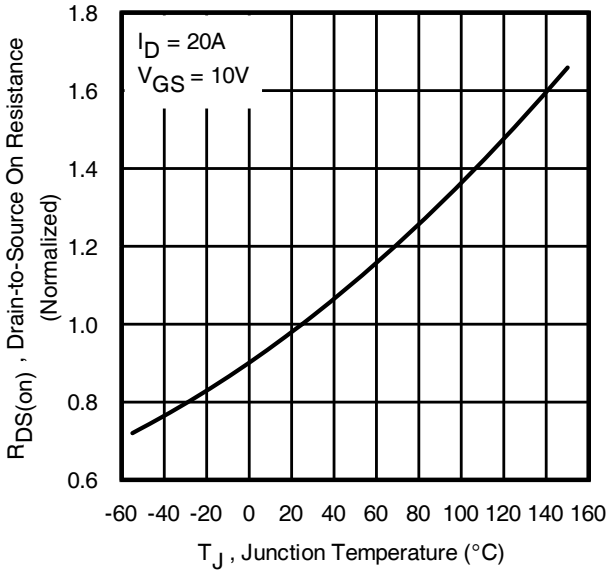


Fig 4. Normalized On-Resistance vs. Temperature

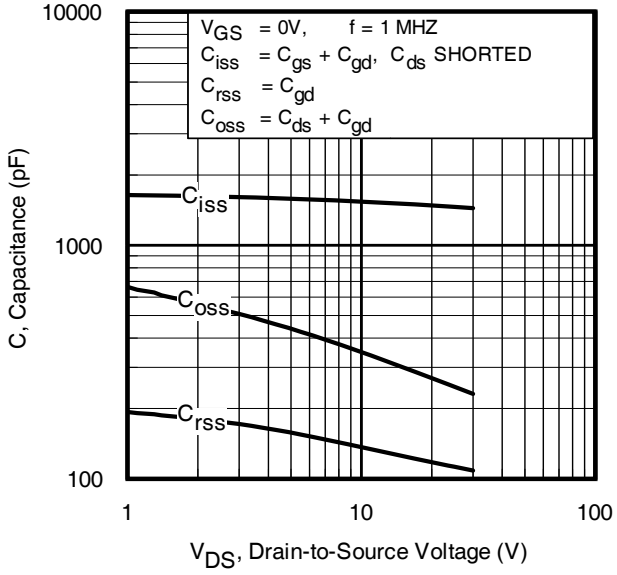


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

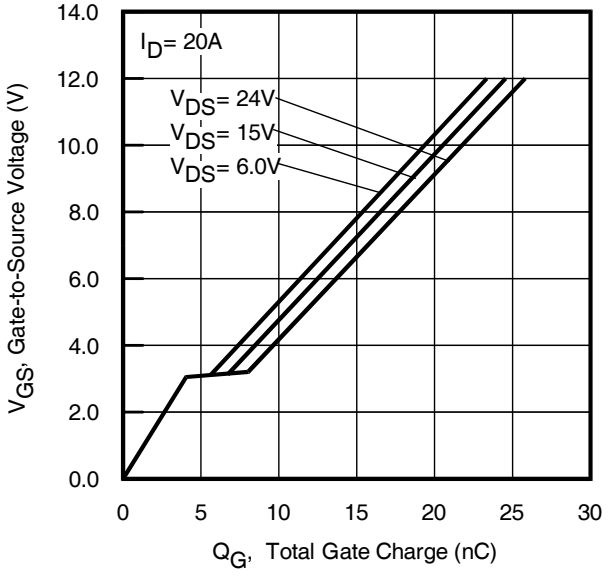


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

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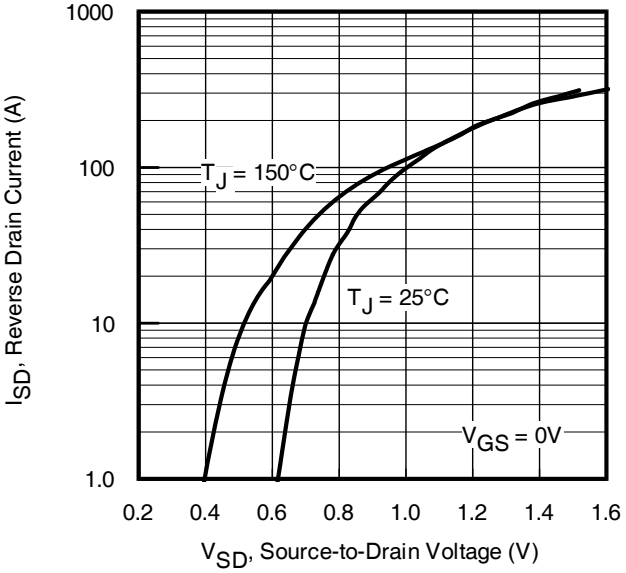


Fig 7. Typical Source-Drain Diode Forward Voltage

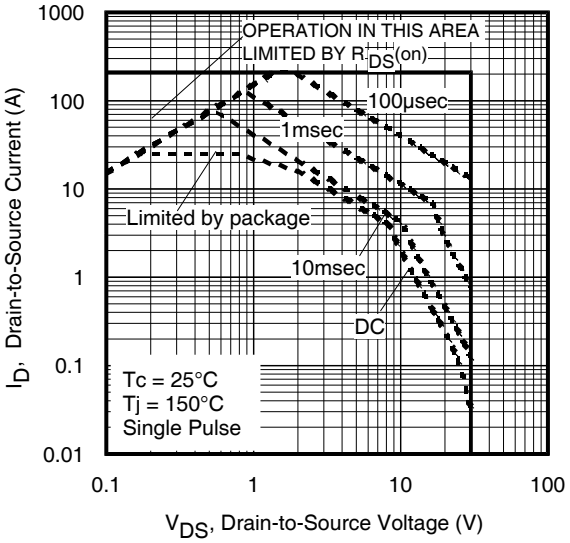


Fig 8. Maximum Safe Operating Area

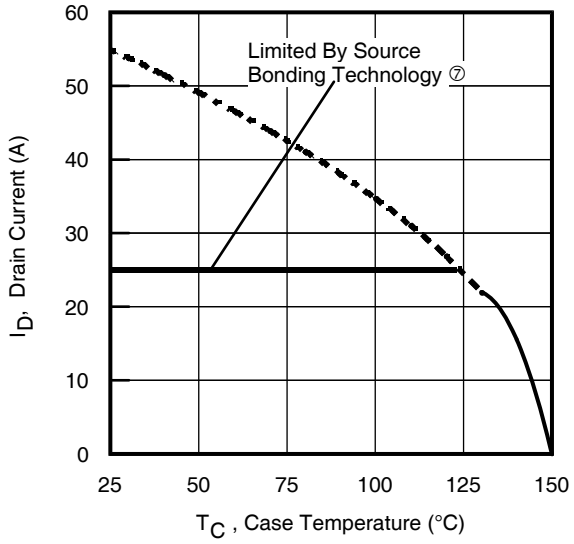


Fig 9. Maximum Drain Current vs. Case Temperature

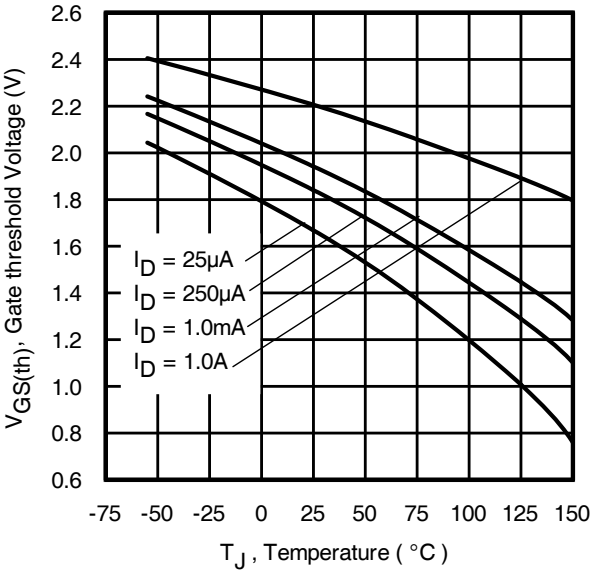


Fig 10. Drain-to–Source Breakdown Voltage

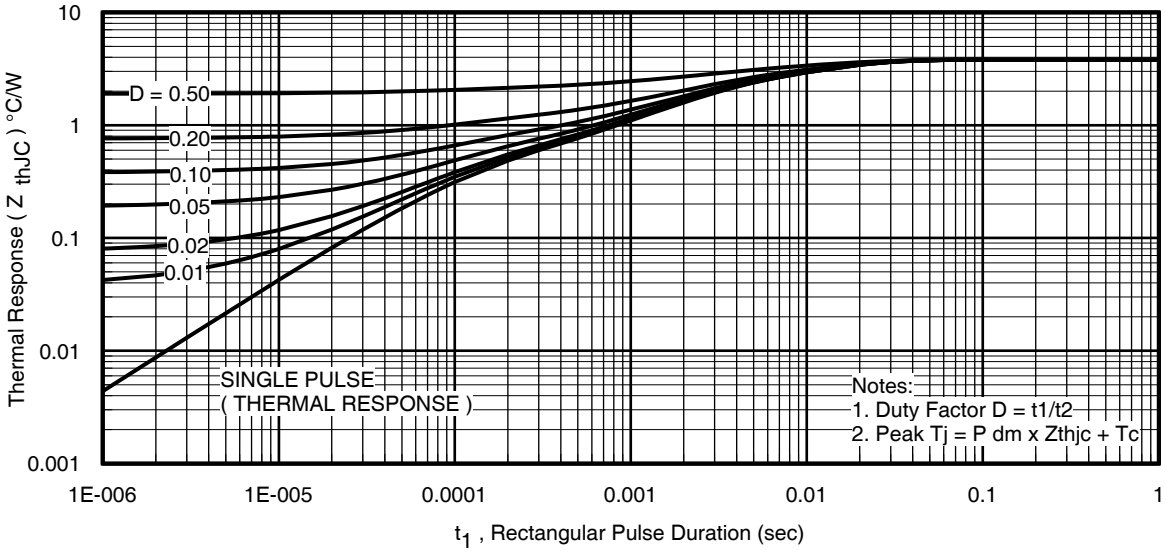


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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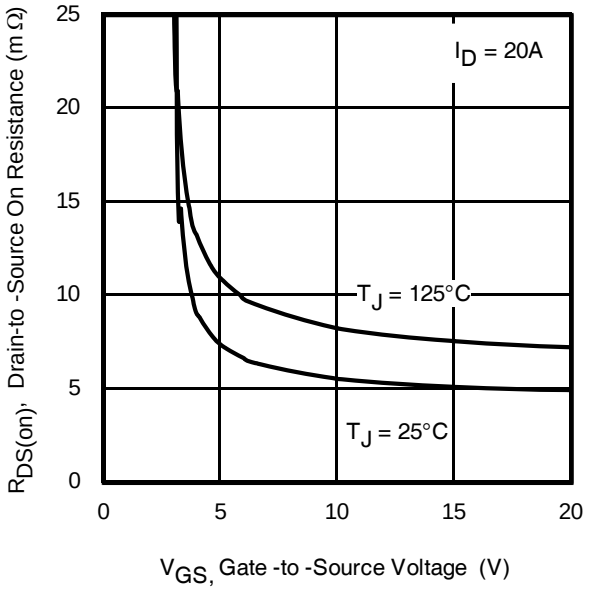


Fig 12. On-Resistance vs. Gate Voltage

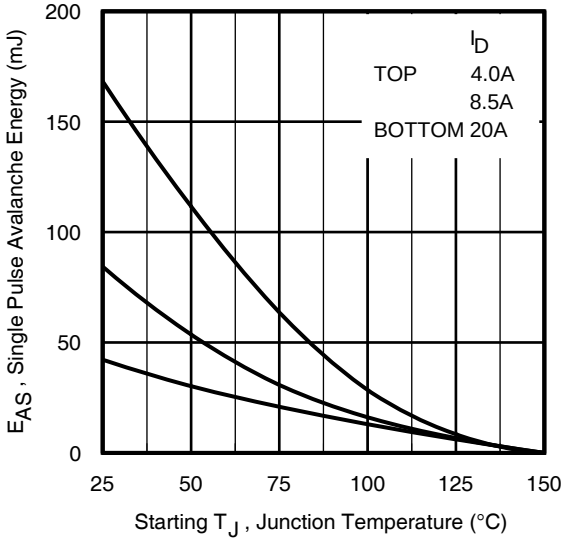


Fig 13. Maximum Avalanche Energy vs. Drain Current

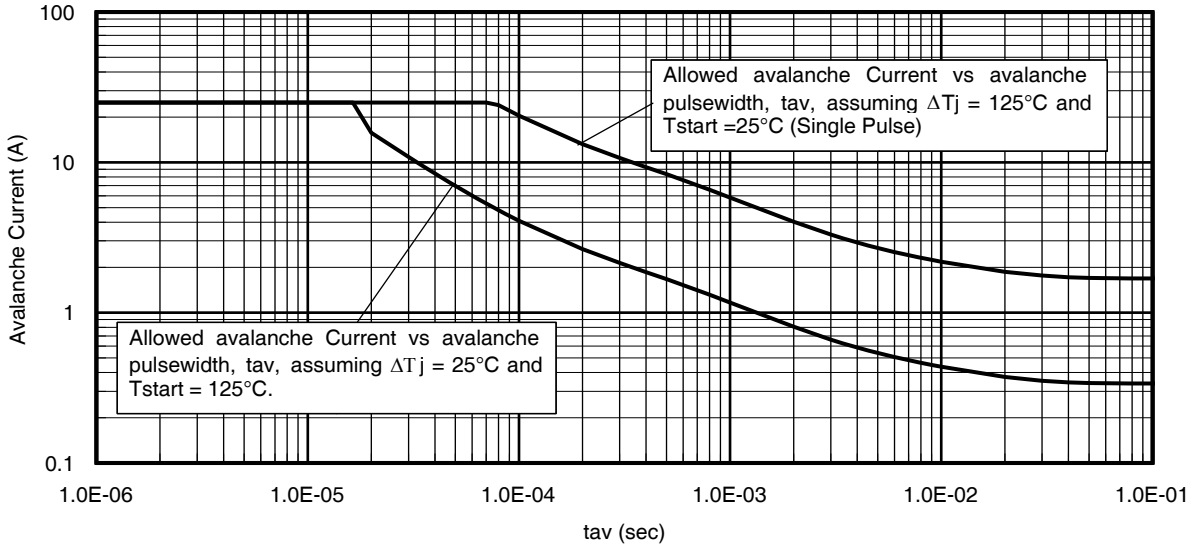


Fig 14. Single Avalanche Event: Pulse Current vs. Pulse Width

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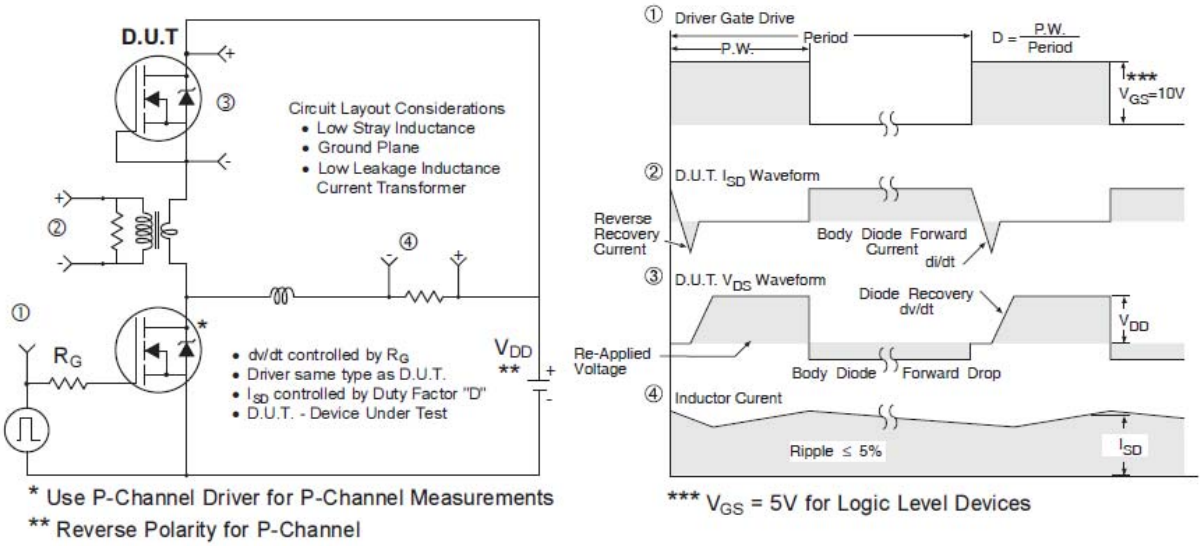


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

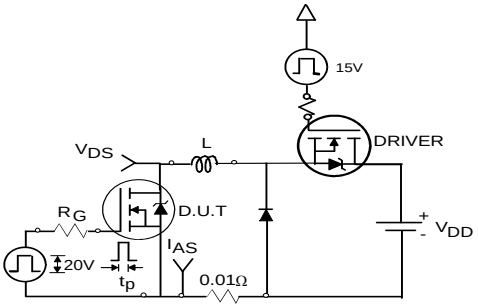


Fig 16a. Unclamped Inductive Test Circuit

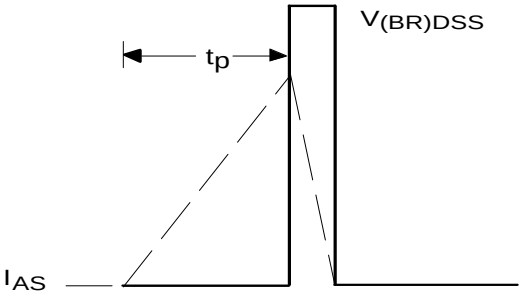


Fig 16b. Unclamped Inductive Waveforms

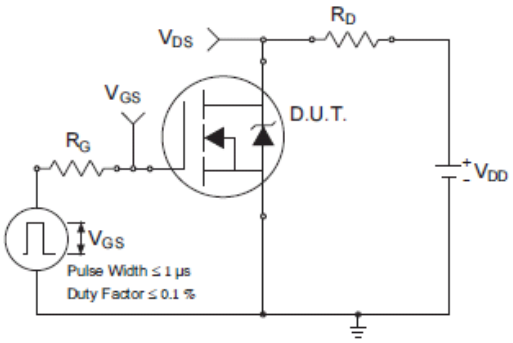


Fig 17a. Switching Time Test Circuit

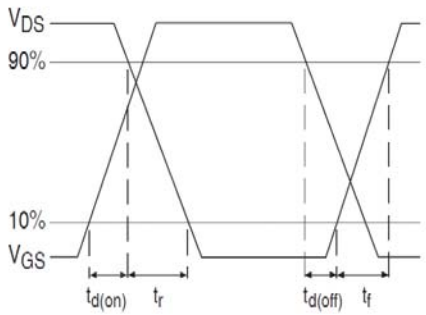


Fig 17b. Switching Time Waveforms

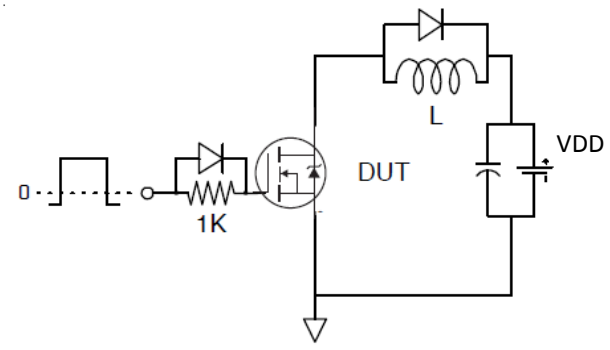


Fig 18a. Gate Charge Test Circuit

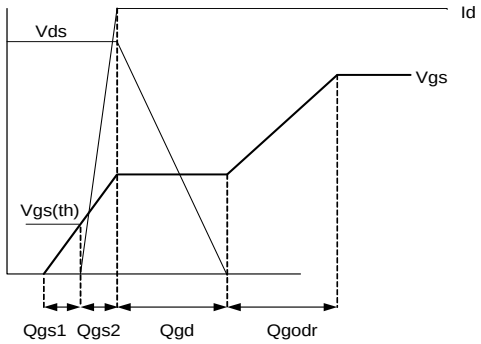


Fig 18b. Gate Charge Waveform

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Placement and Layout Guidelines

The typical application topology for this product is the synchronous buck converter. These converters operate at high frequencies (typically around 400 kHz). During turn-on and turn-off switching cycles, the high di/dt currents circulating in the parasitic elements of the circuit induce high voltage ringing which may exceed the device rating and lead to undesirable effects. One of the major contributors to the increase in parasitics is the PCB power circuit inductance.

This section introduces a simple guideline that mitigates the effect of these parasitics on the performance of the circuit and provides reliable operation of the devices.

To reduce high frequency switching noise and the effects of Electromagnetic Interference (EMI) when the control MOSFET (Q1) is turned on, the layout shown in Figure 19 is recommended. The input bypass capacitors, control MOSFET and output capacitors are placed in a tight loop to minimize parasitic inductance which in turn lowers the amplitude of the switch node ringing, and minimizes exposure of the MOSFETs to repetitive avalanche conditions.

When the synchronous MOSFET (Q2) is turned on, high average DC current flows through the path indicated in Figure 19. Therefore, the Q2 turn-on path should be laid out with a tight loop and wide traces at both ends of the inductor to minimize loop resistance.

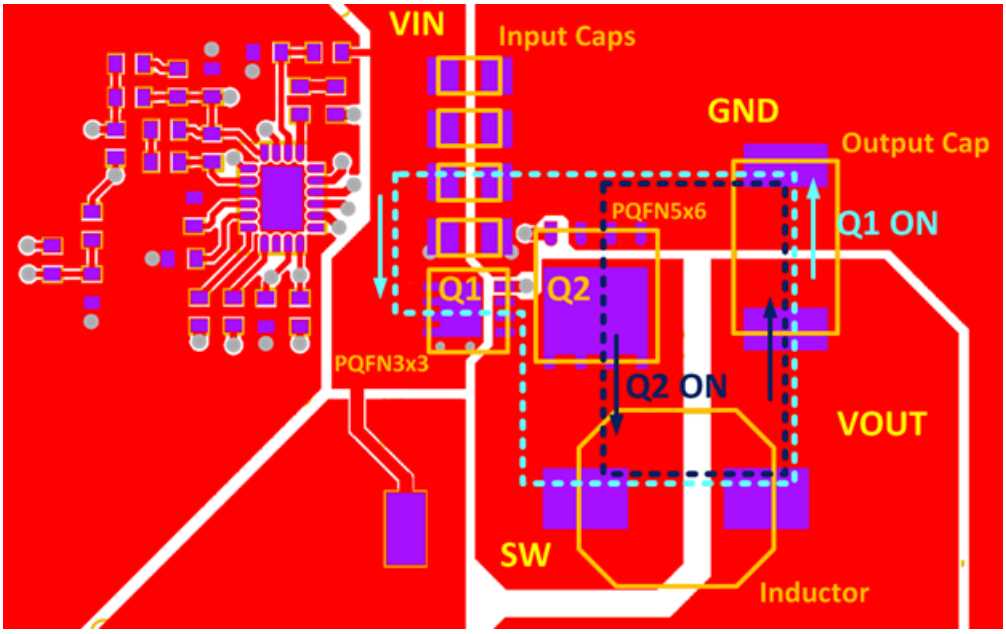
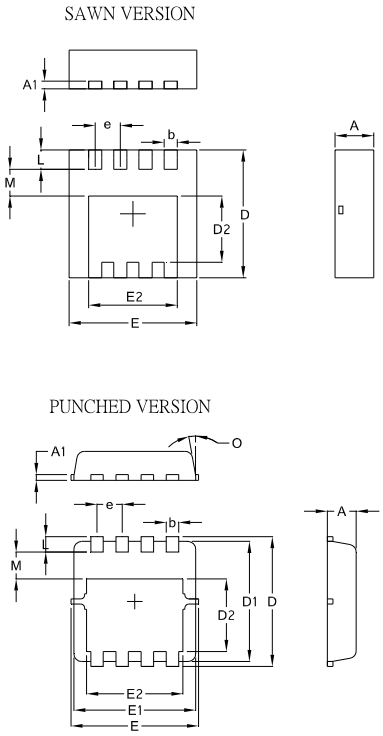


Fig 19. Placement and Layout Guidelines

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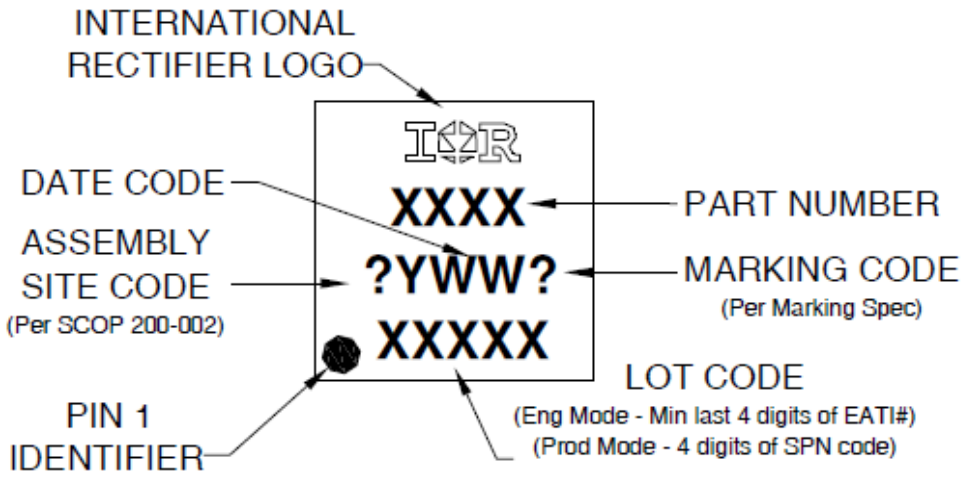
PQFN 3.3mm x 3.3mm Outline Package Details



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.05	0.0276	0.0413
A1	0.12	0.39	0.0047	0.0154
b	0.25	0.39	0.0098	0.0154
D	3.20	3.45	0.1260	0.1358
D1	3.00	3.20	0.1181	0.1417
D2	1.69	2.20	0.0665	0.0866
E	3.20	3.40	0.1260	0.1339
E1	3.00	3.20	0.1181	0.1417
E2	2.15	2.59	0.0846	0.1020
e	0.65 BSC		0.0256 BSC	
L	0.15	0.55	0.0059	0.0217
M	0.59	—	0.0232	—
O	9Deg	12Deg	9Deg	12Deg

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

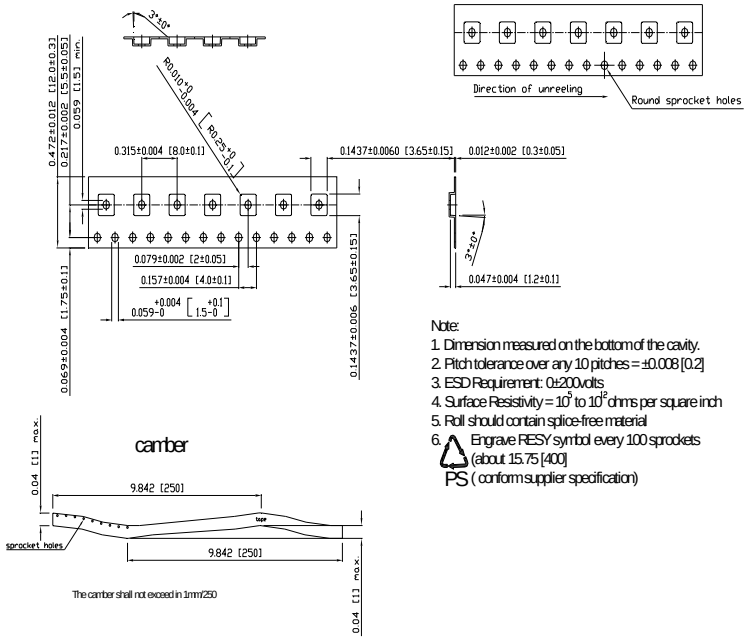
PQFN 3.3mm x 3.3mm Outline Part Marking



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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PQFN 3.3mm x 3.3mm Outline Tape and Reel



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level	Consumer (per JEDEC JESD47F†† guidelines)	
Moisture Sensitivity Level	PQFN 3.3mm x 3.3mm	MSL1 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability

†† Applicable version of JEDEC standard at the time of product release.

Notes:

① Starting T_J = 25°C, L = 0.21mH, R_G = 50Ω, I_{AS} = 20A.

② Pulse width ≤ 400μs; duty cycle ≤ 2%.

③ R_θ is measured at T_J of approximately 90°C.

④ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details: http://www.irf.com/technical-info/appnotes/an-994.pdf

⑤ Calculated continuous current based on maximum allowable junction temperature.

⑥ Current is limited to 25A by source bonding technology.

⑦ Pulse drain current is limited by source bonding technology.

International IOR Rectifier

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To contact International Rectifier, please visit http://www.irf.com/whoto-call/

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