TPS54340 42 V Input, 3.5 A, Step Down DC-DC Converter with Eco-mode™

1 Features

- 4.5 V to 42 V (45 V Abs Max) Input Range
- 3.5 A Continuous Current, 4.5 A Minimum Peak Inductor Current Limit
- Current Mode Control DC-DC Converter
- 92-mΩ High-Side MOSFET
- High Efficiency at Light Loads with Pulse Skipping Eco-mode™
- Low Dropout at Light Loads with Integrated BOOT Recharge FET
- 146 µA Operating Quiescent Current
- 1 µA Shutdown Current
- 100 kHz to 2.5 MHz Fixed Switching Frequency
- Synchronizes to External Clock
- Adjustable UVLO Voltage and Hysteresis
- Internal Soft-Start
- Accurate Cycle-by-Cycle Current Limit
- Thermal, Overvoltage, and Frequency Foldback Protection
- 0.8 V 1% Internal Voltage Reference
- 8-Terminal HSOIC with PowerPAD™ Package
- –40°C to 150°C T_J Operating Range
- Supported by WEBENCH™ Software Tool

2 Applications

12 V, 24 V Industrial, Automotive and Communications Power Systems

3 Description

The TPS54340 is a 42 V, 3.5 A, step down regulator with an integrated high side MOSFET. The device survives load dump pulses up to 45 V per ISO 7637. Current mode control provides simple external compensation and flexible component selection. A low ripple pulse skip mode reduces the no load supply current to 146 µA. Shutdown supply current is reduced to 1 µA when the enable pin is pulled low.

Undervoltage lockout is internally set at 4.3 V but can be increased using the enable pin. The output voltage start up ramp is internally controlled to provide a controlled start up and eliminate overshoot.

A wide switching frequency range allows either efficiency or external component size to be optimized. Frequency foldback and thermal shutdown protects internal and external components during an overload condition.

The TPS54340 is available in an 8-terminal thermally enhanced HSOIC PowerPAD™ package.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS54340DDA	HSOIC (8)	4,89mm x 3,9mm

4 Simplified Schematic

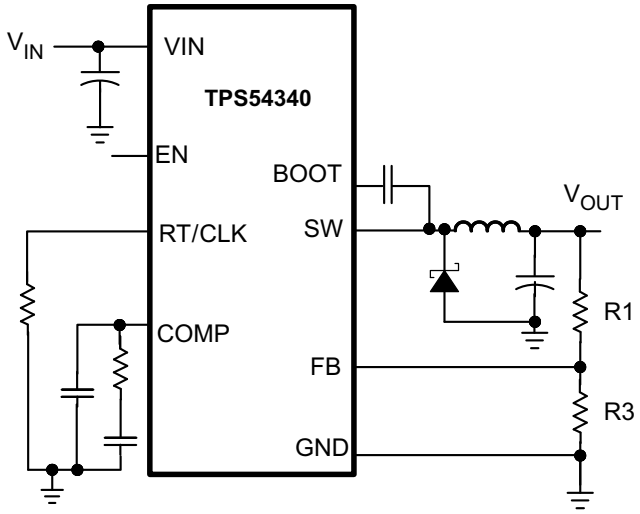
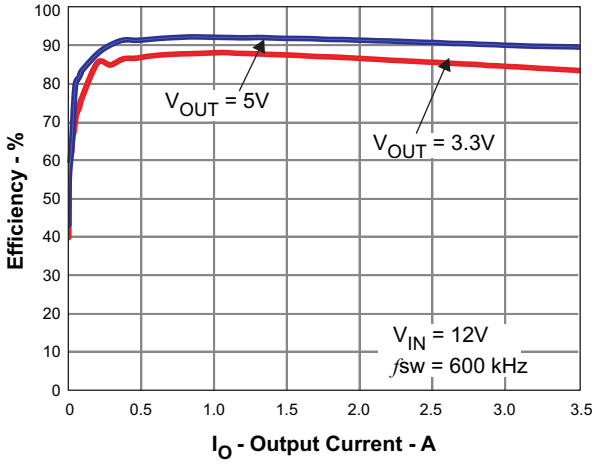


Figure 1. Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2013) to Revision B **Page**

- Changed the data sheet to the new TI layout ... 1
- Changed the Application List From: 12 V, 24 V and 48 V Industrial To: 12 V, 24 V Industrial ... 1
- Added the Device Information table ... 1
- Added the Handling Ratings table ... 4
- Added the Recommended Operating Conditions table ... 4
- Added the Thermal Information table inside the document ... 4
- Changed the Operating: nonswitching supply current TEST CONDITIONS From: FB = 0.83 V To: FB = 0.9 V ... 5
- Changed RT/CLK high threshold MAX value From: 1.7 V To: 2 V ... 5
- Changed Figure 7 title From: HIGH FREQUENCY RANGE To: LOW FREQUENCY RANGE ... 6
- Changed Figure 8 title From: LOW FREQUENCY RANGE To: HIGH FREQUENCY RANGE ... 7
- Added the Power Supply Recommendations section ... 34

Changes from Original (October 2012) to Revision A **Page**

- Changed Figure 12 From: I_{EN} (µV) To: I_{EN} (µA) ... 7
- Changed Figure 13 From: I_{EN} (µV) To: I_{EN} (µA) ... 7

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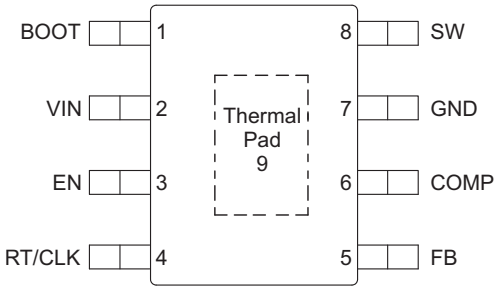
6 Terminal Configuration and Functions

HSOIC PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high side MOSFET, the output is switched off until the capacitor is refreshed.
VIN	2	I	Input supply voltage with 4.5 V to 42 V operating range.
EN	3	I	Enable terminal, with internal pull-up current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the Enable and Adjusting Undervoltage Lockout section.
RT/CLK	4	I	Resistor Timing and External Clock. An internal amplifier holds this terminal at a fixed voltage when using an external resistor to ground to set the switching frequency. If the terminal is pulled above the PLL upper threshold, a mode change occurs and the terminal becomes a synchronization input. The internal amplifier is disabled and the terminal is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
FB	5	I	Inverting input of the transconductance (gm) error amplifier.
COMP	6	O	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this terminal.
GND	7	–	Ground
SW	8	I	The source of the internal high-side power MOSFET and switching node of the converter.
Thermal Pad	9	–	GND terminal must be electrically connected to the exposed pad on the printed circuit board for proper operation.

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7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	45	V
	EN	–0.3	8.4	
	BOOT		53	
	FB	–0.3	3	
	COMP	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	BOOT-SW		8	V
	SW	–0.6	45	
	SW, 10-ns Transient	–2	45	
Operating junction temperature		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage temperature range	–65	150	°C
V_{ESD} (1)	Human Body Model (HBM) ESD Stress Voltage (2)		2	kV
	Charged Device Model (HBM) ESD Stress Voltage (3)		500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. terminals listed as 1000V may actually have higher performance.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. terminals listed as 250V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	4.5	42	V
V_O	Output voltage	0.8	41.1	V
I_O	Output current	0	5	A
T_J	Junction Temperature	–40	150	°C

7.4 Thermal Information

THERMAL METRIC(1)(2)		TPS54340 DDA (8 TERMINALS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance (standard board)	42.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	
ψ_{JB}	Junction-to-board characterization parameter	23.4	
θ_{JCtop}	Junction-to-case(top) thermal resistance	45.8	
θ_{JCbot}	Junction-to-case(bottom) thermal resistance	3.6	
θ_{JB}	Junction-to-board thermal resistance	23.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section of this data sheet for more information.

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7.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 4.5 V to 42 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN TERMINAL)						
	Operating input voltage		4.5		42	V
	Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
	Internal undervoltage lockout threshold hysteresis			325		mV
	Shutdown supply current	EN = 0 V, 25°C, 4.5 V ≤ VIN ≤ 42 V		1.3	3.5	µA
	Operating: nonswitching supply current	FB = 0.9 V, T_A = 25°C		146	175	
ENABLE AND UVLO (EN TERMINAL)						
	Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
	Input current	Enable threshold +50 mV		–4.6		µA
		Enable threshold –50 mV	–0.58	–1.2	-1.8	
	Hysteresis current		–2.2	–3.4	-4.5	µA
VOLTAGE REFERENCE						
	Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET						
	On-resistance	VIN = 12 V, BOOT-SW = 6 V		92	190	mΩ
ERROR AMPLIFIER						
	Input current			50		nA
	Error amplifier transconductance (g_M)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		350		µMhos
	Error amplifier transconductance (g_M) during soft-start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{FB} = 0.4 V		77		µMhos
	Error amplifier dc gain	V_{FB} = 0.8 V		10,000		V/V
	Min unity gain bandwidth			2500		kHz
	Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±30		µA
	COMP to SW current transconductance			12		A/V
CURRENT LIMIT						
	Current limit threshold	All V_{IN} and temperatures, Open Loop(1)	4.5	5.5	6.8	A
		All temperatures, VIN = 12 V, Open Loop(1)	4.5	5.5	6.25	
		V_{IN} = 12 V, T_A = 25°C, Open Loop(1)	5.2	5.5	5.85	
THERMAL SHUTDOWN						
	Thermal shutdown			176		°C
	Thermal shutdown hysteresis			12		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK TERMINAL)						
	Switching frequency range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching frequency range using CLK mode		160		2300	kHz
	RT/CLK high threshold			1.55	2	V
	RT/CLK low threshold		0.5	1.2		V

(1) Open Loop current limit measured directly at the SW terminal and is independent of the inductor value and slope compensation.

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7.6 Timing Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE AND UVLO (EN TERMINAL)					
Enable to COMP active	V_{IN} = 12 V , T_A = 25°C		540		µs
INTERNAL SOFT-START TIME					
Soft-Start Time	f_{SW} = 500 kHz, 10% to 90%		2.1		ms
Soft-Start Time	f_{SW} = 2.5 MHz, 10% to 90%		0.42		ms
HIGH-SIDE MOSFET					
Minimum controllable on time	VIN = 12 V, T_A = 25°C		135		ns
CURRENT LIMIT					
Current limit threshold delay			60		ns
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK TERMINAL)					
Minimum CLK input pulse width			15		ns
RT/CLK falling edge to SW rising edge delay	Measured at 500 kHz with RT resistor in series		55		ns
PLL lock in time	Measured at 500 kHz		78		µs

7.7 Typical Characteristics

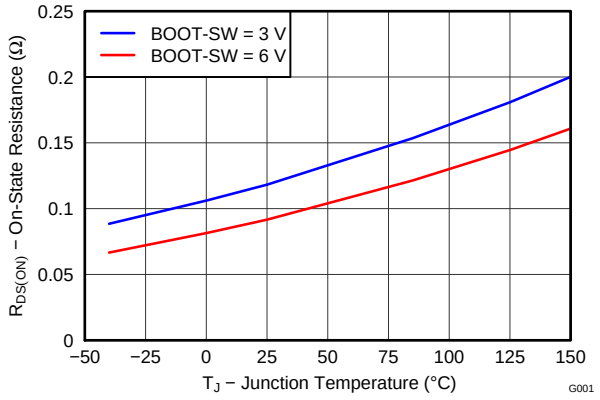

Figure 2. On Resistance vs Junction Temperature

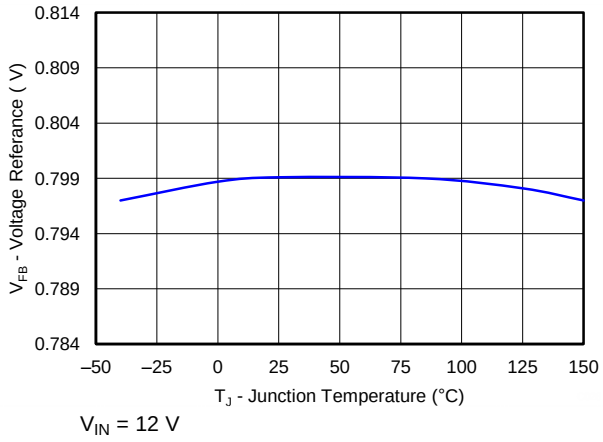

Figure 3. Voltage Reference vs Junction Temperature

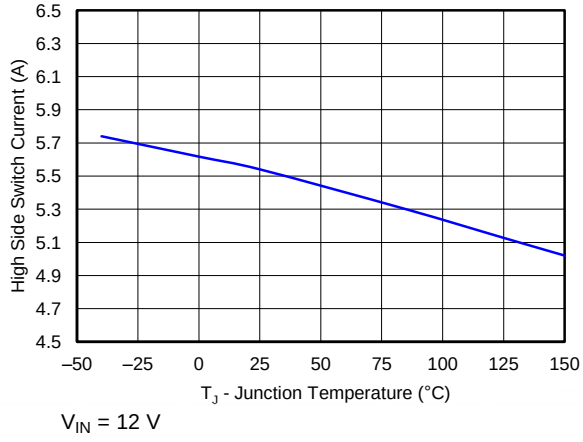

Figure 4. Switch Current Limit vs Junction Temperature

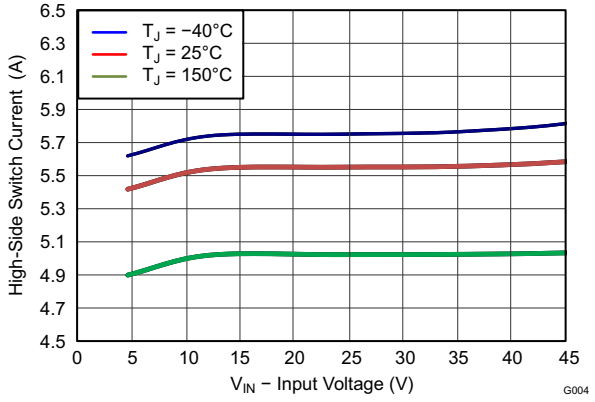

Figure 5. Switch Current Limit vs Input Voltage

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Typical Characteristics (continued)

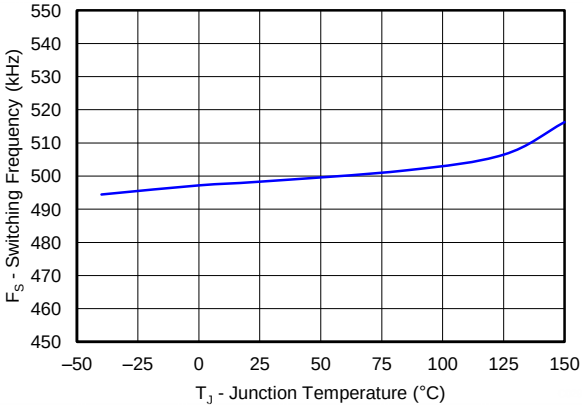

Figure 6. Switching Frequency vs Junction Temperature

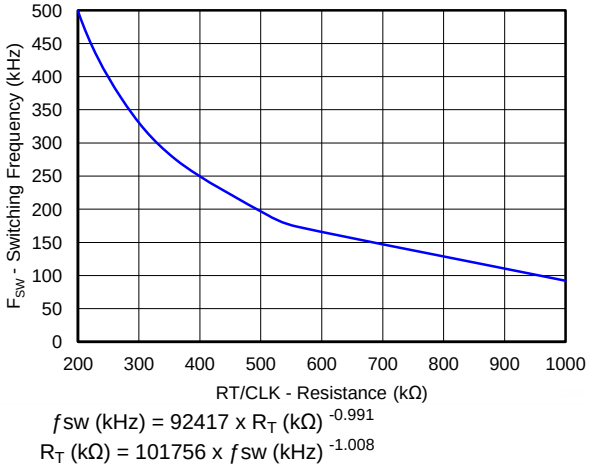

Figure 7. Switching Frequency vs RT/CLK Resistance Low Frequency Range

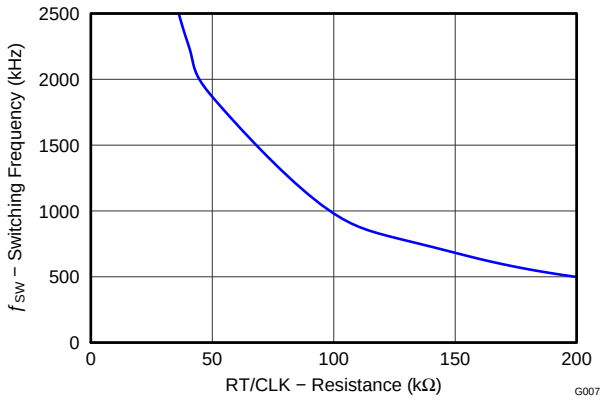

Figure 8. Switching Frequency vs RT/CLK Resistance High Frequency Range

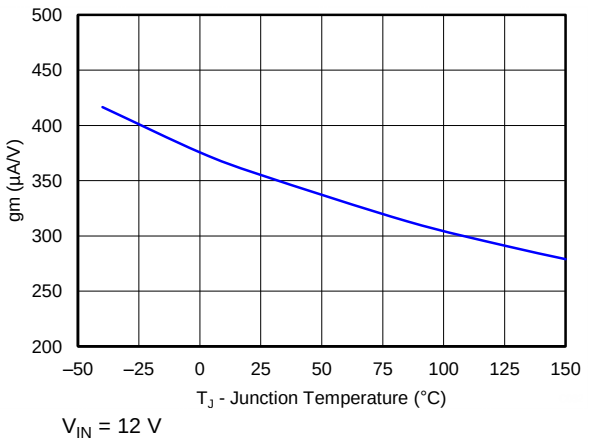

Figure 9. EA Transconductance vs Junction Temperature

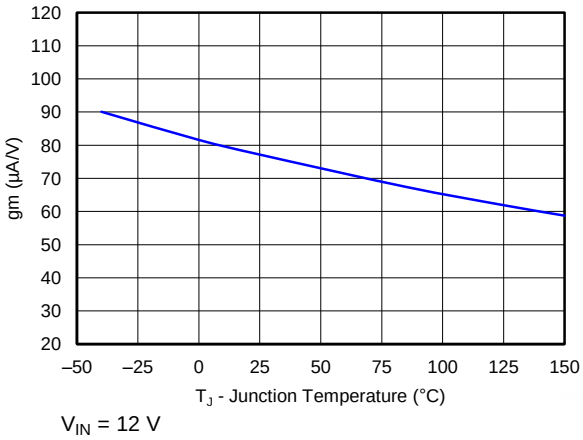

Figure 10. EA Transconductance During Soft-Start vs Junction Temperature

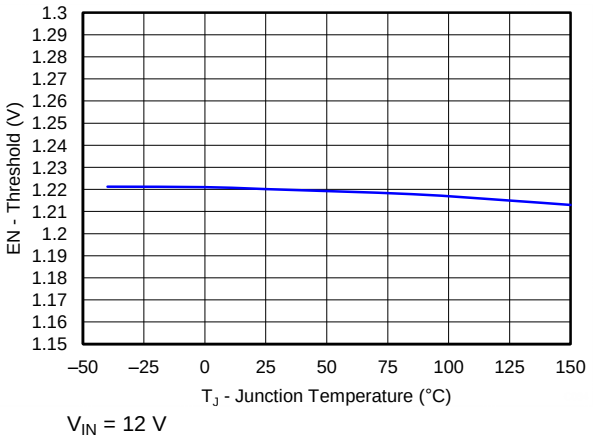

Figure 11. EN Terminal Voltage vs Junction Temperature

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Typical Characteristics (continued)

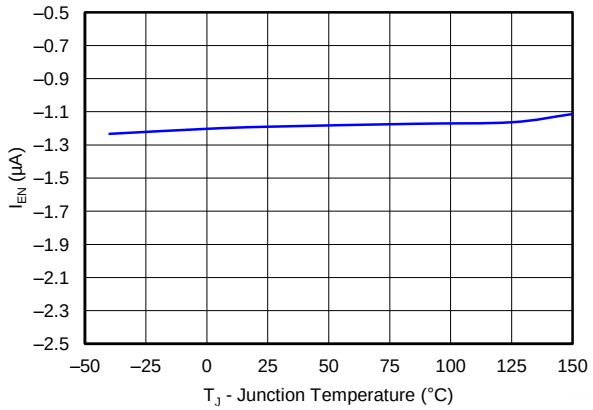

Figure 12. EN Terminal Current vs Junction Temperature

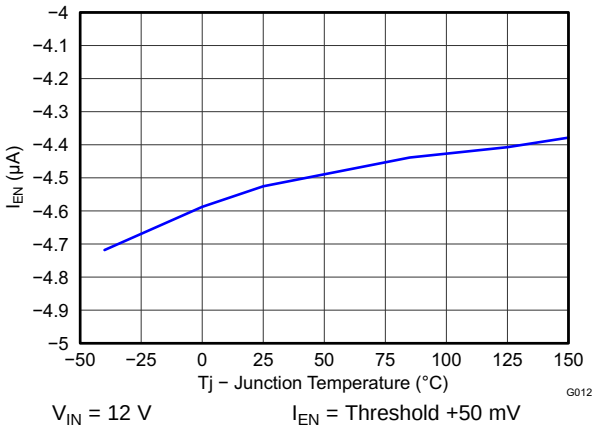

Figure 13. EN Terminal Current vs Junction Temperature

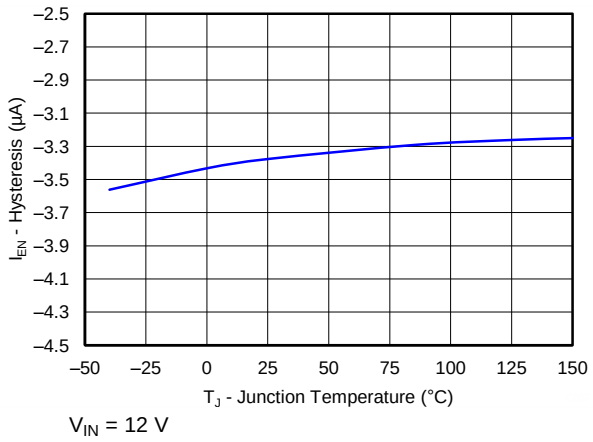

Figure 14. EN Terminal Current Hysteresis vs Junction Temperature

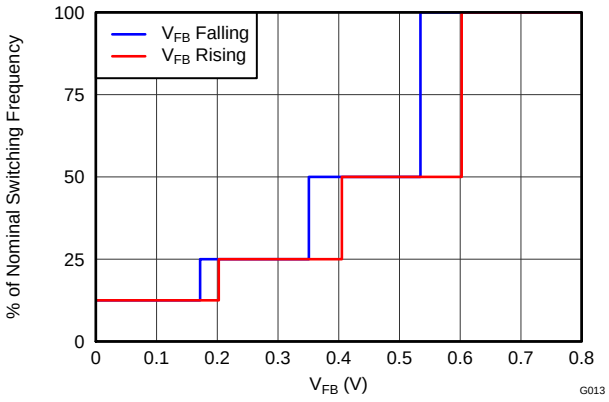

Figure 15. Switching Frequency vs FB

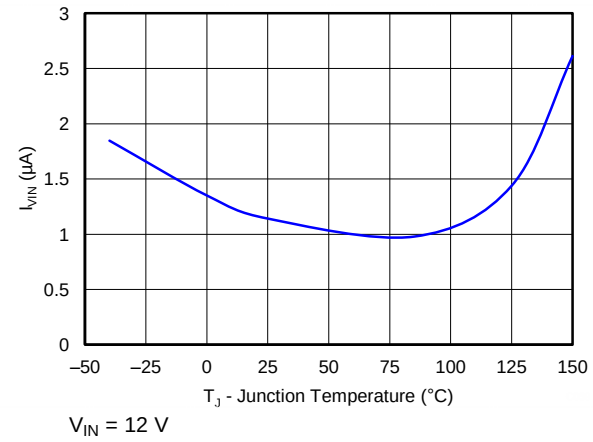

Figure 16. Shutdown Supply Current vs Junction Temperature

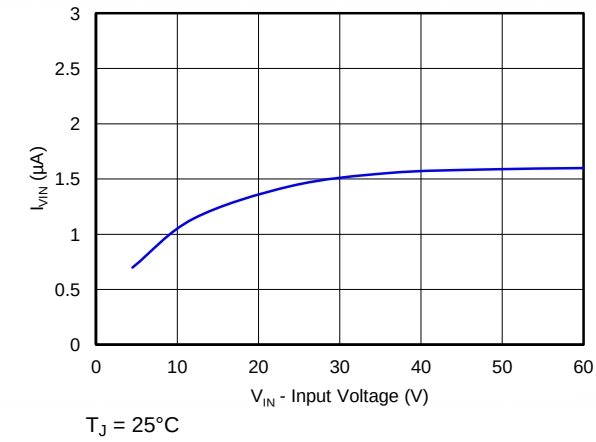

Figure 17. Shutdown Supply Current vs Input Voltage (V_{IN})

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Typical Characteristics (continued)

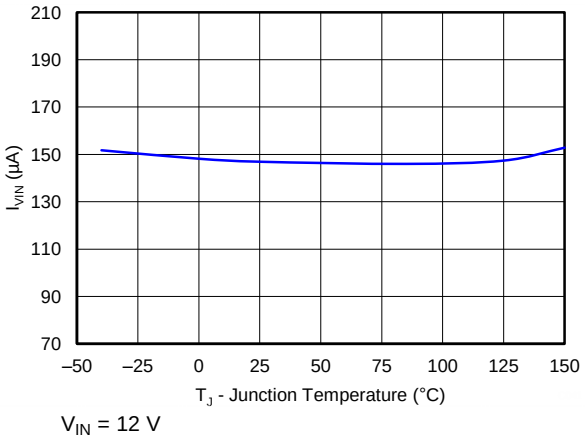

Figure 18. V_{IN} Supply Current vs Junction Temperature

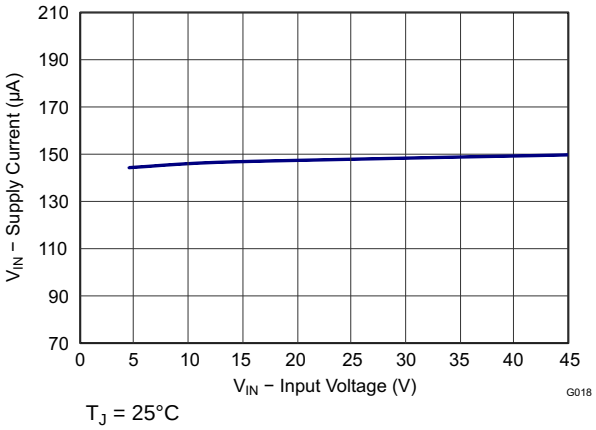

Figure 19. V_{IN} Supply Current vs Input Voltage

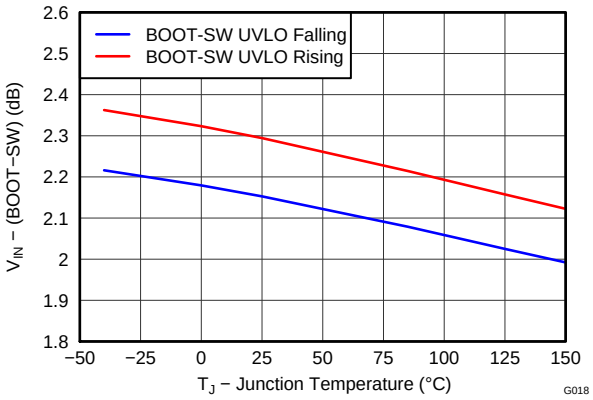

Figure 20. BOOT-SW UVLO vs Junction Temperature

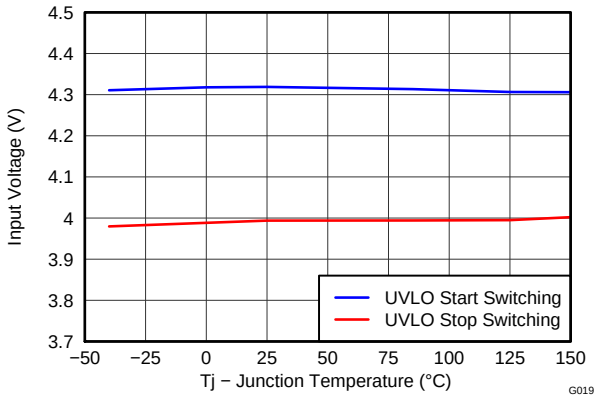

Figure 21. Input Voltage UVLO vs Junction Temperature

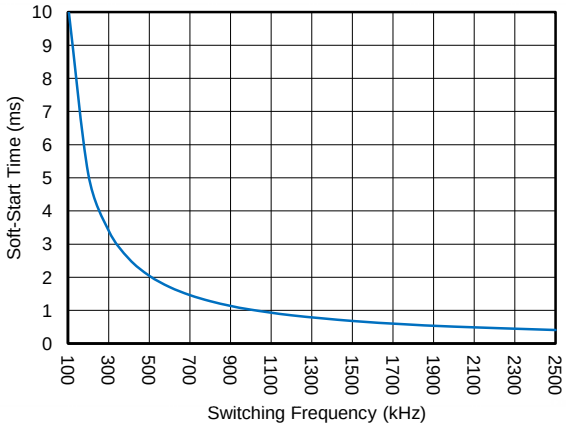

Figure 22. Soft-Start Time vs Switching Frequency

8 Detailed Description

8.1 Overview

The TPS54340 is a 42 V, 3.5 A, step-down (buck) regulator with an integrated high side n-channel MOSFET. The device implements constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 kHz to 2500 kHz allows either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK terminal. The device has an internal phase-locked loop (PLL) connected to the RT/CLK terminal that will synchronize the power switch turn on to a falling edge of an external clock signal.

The TPS54340 has a default input start-up voltage of approximately 4.3 V. The EN terminal can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. An internal pull up current source enables operation when the EN terminal is floating. The operating current is 146 µA under no load condition (not switching). When the device is disabled, the supply current is 1 µA.

The integrated 92mΩ high side MOSFET supports high efficiency power supply designs capable of delivering 3.5 amperes of continuous current to a load. The gate drive bias voltage for the integrated high side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to SW terminals. The TPS54340 reduces the external component count by integrating the bootstrap recharge diode. The BOOT terminal capacitor voltage is monitored by a UVLO circuit which turns off the high side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54340 to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is the internal 0.8 V feedback reference.

Output overvoltage transients are minimized by an Overvoltage Transient Protection (OVP) comparator. When the OVP comparator is activated, the high side MOSFET is turned off and remains off until the output voltage is less than 106% of the desired output voltage.

The TPS54340 includes an internal soft-start circuit that slows the output rise time during start-up to reduce in-rush current and output voltage overshoot. Output overload conditions reset the soft-start timer. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help maintain control of the inductor current.

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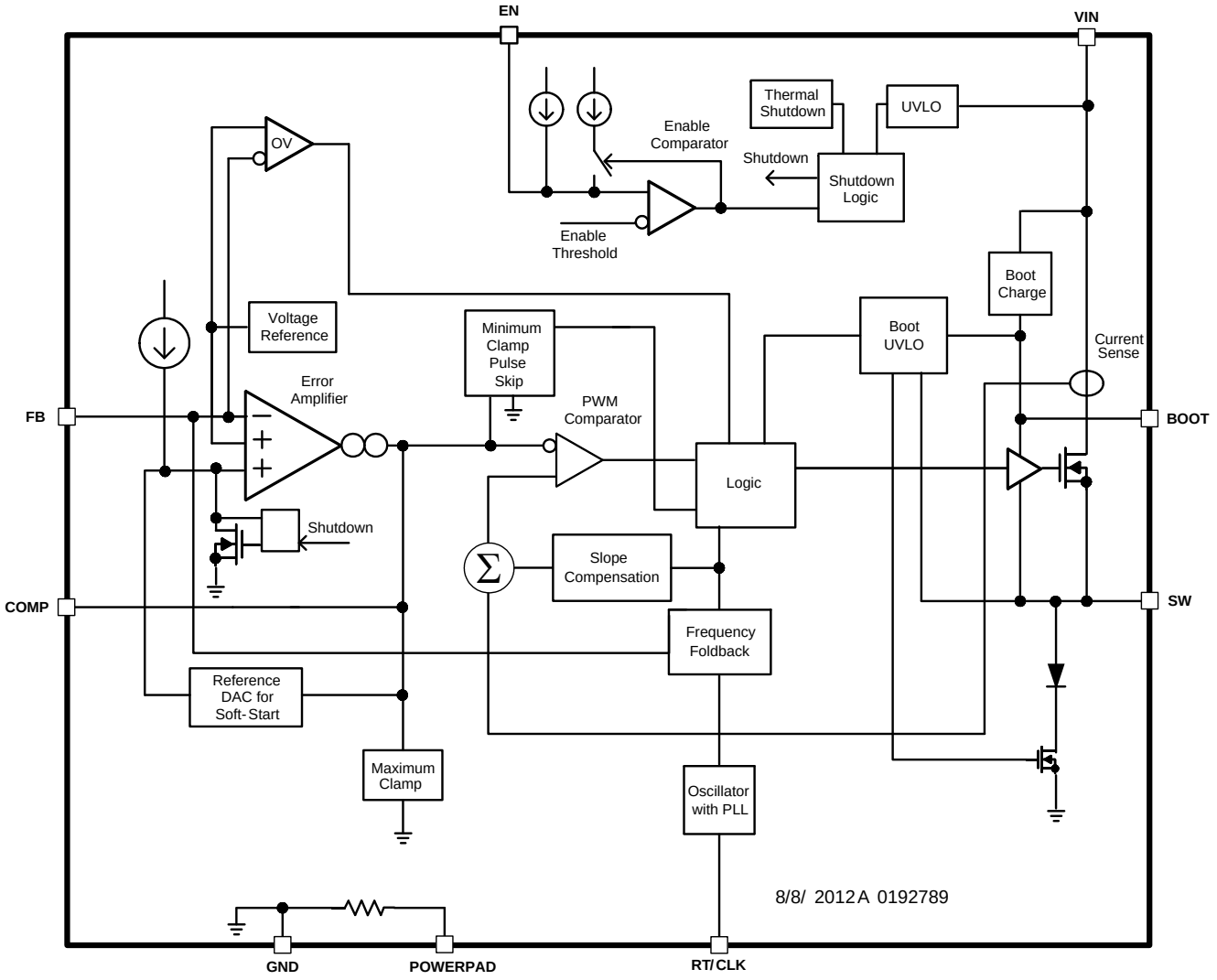
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The TPS54340 uses fixed frequency, peak current mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB terminal to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output at the COMP terminal controls the high side power switch current. When the high side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off. The COMP terminal voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP terminal voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP terminal.

8.3.2 Slope Compensation Output Current

The TPS54340 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

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Feature Description (continued)

8.3.3 Pulse Skip Eco-mode

The TPS54340 operates in a pulse skipping Eco-mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters Eco-mode. The pulse skipping current threshold is the peak switch current level corresponding to a nominal COMP voltage of 600 mV.

When in Eco-mode, the COMP terminal voltage is clamped at 600 mV and the high side MOSFET is inhibited. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the COMP terminal voltage. The high side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the Eco-mode pulse skipping threshold at which time the device again enters Eco-mode. The internal PLL remains operational when in Eco-mode. When operating at light load currents in Eco-mode, the switching transitions occur synchronously with the external clock signal.

During Eco-mode operation, the TPS54340 senses and controls peak switch current, not the average load current. Therefore the load current at which the device enters Eco-mode is dependent on the output inductor value. The circuit in Figure 36 enters Eco-mode at about 31.4 mA output current. As the load current approaches zero, the device enters a pulse skip mode during which it draws only 146 µA input quiescent current.

8.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54340 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW terminals provides the gate drive voltage for the high side MOSFET. The BOOT capacitor is refreshed when the high side MOSFET is off and the external low side diode conducts. The recommended value of the BOOT capacitor is 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high side MOSFET of the TPS54340 will operate at 100% duty cycle as long as the BOOT to SW terminal voltage is greater than 2.1V. When the voltage from BOOT to SW drops below 2.1V, the high side MOSFET is turned off and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low side MOSFET at high output voltages, it is disabled at 24 V output and re-enabled when the output reaches 21.5 V.

Since the gate drive current sourced from the BOOT capacitor is small, the high side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low side diode voltage and the printed circuit board resistance.

The start and stop voltage for a typical 5 V output application is shown in Figure 23 where the Vin voltage is plotted versus load current. The start voltage is defined as the input voltage needed to regulate the output within 1% of nominal. The stop voltage is defined as the input voltage at which the output drops by 5% or where switching stops.

During high duty cycle (low dropout) conditions, inductor current ripple increases when the BOOT capacitor is being recharged resulting in an increase in output voltage ripple. Increased ripple occurs when the off time required to recharge the BOOT capacitor is longer than the high side off time associated with cycle by cycle PWM control.

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Feature Description (continued)

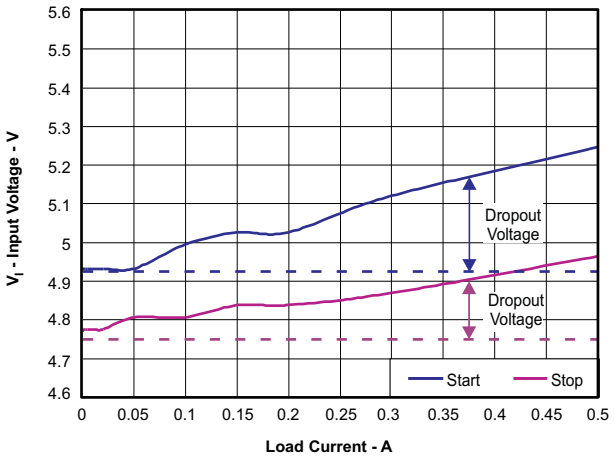

Figure 23. 5V Start/Stop Voltage

8.3.5 Error Amplifier

The TPS54340 voltage regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB terminal voltage to the lower of the internal soft-start voltage or the internal 0.8 V voltage reference. The transconductance (gm) of the error amplifier is 350 µA/V during normal operation. During soft-start operation, the transconductance is reduced to 78 µA/V and the error amplifier is referenced to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor and capacitor) are connected between the error amplifier output COMP terminal and GND terminal.

8.3.6 Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8 V ±1% voltage reference over the operating temperature and voltage range by scaling the output of a bandgap reference circuit. The output voltage is set by a resistor divider from the output node to the FB terminal. It is recommended to use 1% tolerance or better divider resistors. Select the low side resistor R_{LS} for the desired divider current and use Equation 1 to calculate R_{HS}. To improve efficiency at light loads consider using larger value resistors. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current may become noticeable.

$$R_{HS} = R_{LS} \times \left(\frac{Vout - 0.8V}{0.8\ V} \right) \quad (1)$$

8.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54340 is enabled when the VIN terminal voltage rises above 4.3 V and the EN terminal voltage exceeds the enable threshold of 1.2 V. The TPS54340 is disabled when the VIN terminal voltage falls below 4 V or when the EN terminal voltage is below 1.2 V. The EN terminal has an internal pull-up current source, I1, of 1.2 µA that enables operation of the TPS54340 when the EN terminal floats.

If an application requires a higher undervoltage lockout (UVLO) threshold, use the circuit shown in Figure 24 to adjust the input voltage UVLO with two external resistors. When the EN terminal voltage exceeds 1.2 V, an additional 3.4 µA of hysteresis current, Ihys, is sourced out of the EN terminal. When the EN terminal is pulled below 1.2 V, the 3.4 µA Ihys current is removed. This addional current facilitates adjustable input voltage UVLO hysteresis. Use Equation 2 to calculate R_{UVLO1} for the desired UVLO hysteresis voltage. Use Equation 3 to calculate R_{UVLO2} for the desired VIN start voltage.

In applications designed to start at relatively low input voltages (e.g., 4.5 V) and withstand high input voltages (e.g., 40 V), the EN terminal may experience a voltage greater than the absolute maximum voltage of 8.4 V during the high input voltage condition. It is recommended to use a zener diode to clamp the terminal voltage below the absolute maximum rating.

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Feature Description (continued)

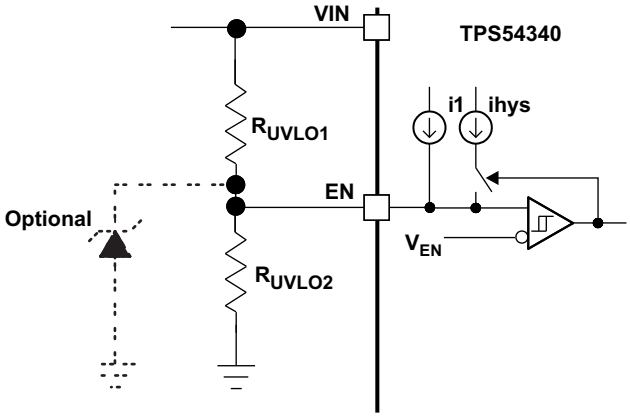

Figure 24. Adjustable Undervoltage Lockout (UVLO)

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \quad (3)$$

8.3.8 Internal Soft-Start

The TPS54340 has an internal digital soft-start that ramps the reference voltage from zero volts to its final value in 1024 switching cycles. The internal soft-start time (10% to 90%) is calculated using Equation 4.

$$t_{SS}(ms) = \frac{1024}{f_{SW}(kHz)} \quad (4)$$

If the EN terminal is pulled below the stop threshold of 1.2 V, switching stops and the internal soft-start resets. The soft-start also resets in thermal shutdown.

8.3.9 Constant Switching Frequency and Timing Resistor (RT/CLK) Terminal)

The switching frequency of the TPS54340 is adjustable over a wide range from 100 kHz to 2500 kHz by placing a resistor between the RT/CLK terminal and GND terminal. The RT/CLK terminal voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 5 or Equation 6 or the curves in Figure 6 and Figure 7. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 135 ns which limits the maximum operating frequency in applications with high input to output step down ratios. The maximum switching frequency is also limited by the frequency foldback circuit. A more detailed discussion of the maximum switching frequency is provided in the next section.

$$RT\ (k\Omega) = \frac{92417}{f sw\ (kHz)^{0.991}} \quad (5)$$

$$f sw\ (kHz) = \frac{101756}{RT\ (k\Omega)^{1.008}} \quad (6)$$

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Feature Description (continued)

8.3.10 Accurate Current Limit Operation and Maximum Switching Frequency

The TPS54340 implements peak current mode control in which the COMP terminal voltage controls the peak current of the high side MOSFET. A signal proportional to the high side switch current and the COMP terminal voltage are compared each cycle. When the peak switch current intersects the COMP control voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier increases switch current by driving the COMP terminal high. The error amplifier output is clamped internally at a level which sets the peak switch current limit. The TPS54340 provides an accurate current limit threshold with a typical current limit delay of 60 ns. With smaller inductor values, the delay will result in a higher peak inductor current. The relationship between the inductor value and the peak inductor current is shown in Figure 25.

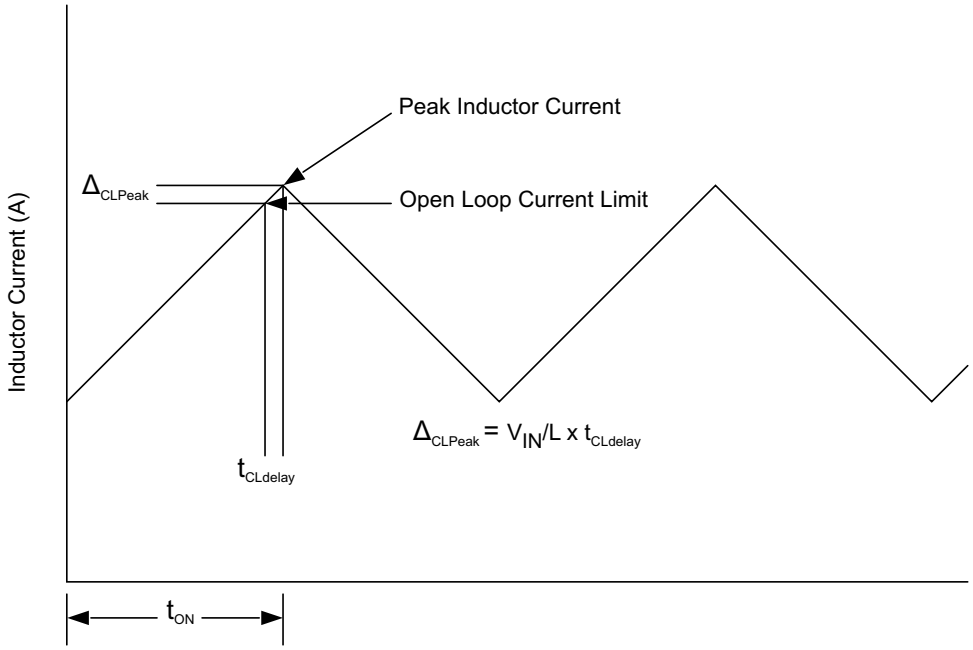

Figure 25. Current Limit Delay

To protect the converter in overload conditions at higher switching frequencies and input voltages, the TPS54340 implements a frequency foldback. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB terminal voltage falls from 0.8 V to 0 V. The TPS54340 uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency foldback effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. Equation 8 calculates the maximum switching frequency at which the inductor current will remain under control when V_{OUT} is forced to $V_{OUT(SC)}$. The selected operating frequency should not exceed the calculated value.

Equation 7 calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value will cause the regulator to skip switching pulses to achieve the low duty cycle required at maximum input voltage.

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_O \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_O \times R_{DS(on)} + V_d} \right) \quad (7)$$

Feature Description (continued)

$$f_{SW(shift)} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_{CL} \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_{CL} \times R_{DS(on)} + V_d} \right) \quad (8)$$

I_O Output current

I_{CL} Current limit

Rdc inductor resistance

V_{IN} maximum input voltage

V_{OUT} output voltage

V_{OUTSC} output voltage during short

Vd diode voltage drop

$R_{DS(on)}$ switch on resistance

t_{ON} controllable on time

f_{DIV} frequency divide equals (1, 2, 4, or 8)

8.3.11 Synchronization to RT/CLKTerminal

The RT/CLK terminal can receive a frequency synchronization signal from an external system clock. To implement this synchronization feature connect a square wave to the RT/CLK terminal through either circuit network shown in Figure 26. The square wave applied to the RT/CLK terminal must switch lower than 0.5 V and higher than 1.7 V and have a pulsewidth greater than 15 ns. The synchronization frequency range is 160 kHz to 2300 kHz. The rising edge of the SW will be synchronized to the falling edge of RT/CLK terminal signal. The external synchronization circuit should be designed such that the default frequency set resistor is connected from the RT/CLK terminal to ground when the synchronization signal is off. When using a low impedance signal source, the frequency set resistor is connected in parallel with an ac coupling capacitor to a termination resistor (e.g., 50 Ω) as shown in Figure 26. The two resistors in series provide the default frequency setting resistance when the signal source is turned off. The sum of the resistance should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10 pF ceramic capacitor to RT/CLK terminal.

The first time the RT/CLK is pulled above the PLL threshold the TPS54340 switches from the RT resistor free-running frequency mode to the PLL synchronized mode. The internal 0.5 V voltage source is removed and the RT/CLK terminal becomes high impedance as the PLL starts to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor mode to the PLL mode and locks onto the external clock frequency within 78 microseconds. During the transition from the PLL mode to the resistor programmed mode, the switching frequency will fall to 150 kHz and then increase or decrease to the resistor programmed frequency when the 0.5 V bias voltage is reapplied to the RT/CLK resistor.

The switching frequency is divided by 8, 4, 2, and 1 as the FB terminal voltage ramps from 0 to 0.8 volts. The device implements a digital frequency foldback to enable synchronizing to an external clock during normal start-up and fault conditions. Figure 27, Figure 28 and Figure 29 show the device synchronized to an external system clock in continuous conduction mode (CCM), discontinuous conduction (DCM), and pulse skip mode (Eco-Mode).

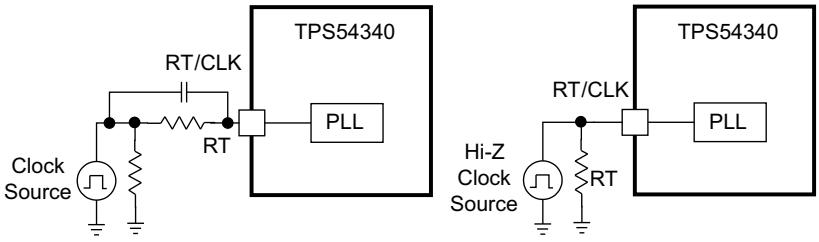

Figure 26. Synchronizing to a System Clock

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Feature Description (continued)

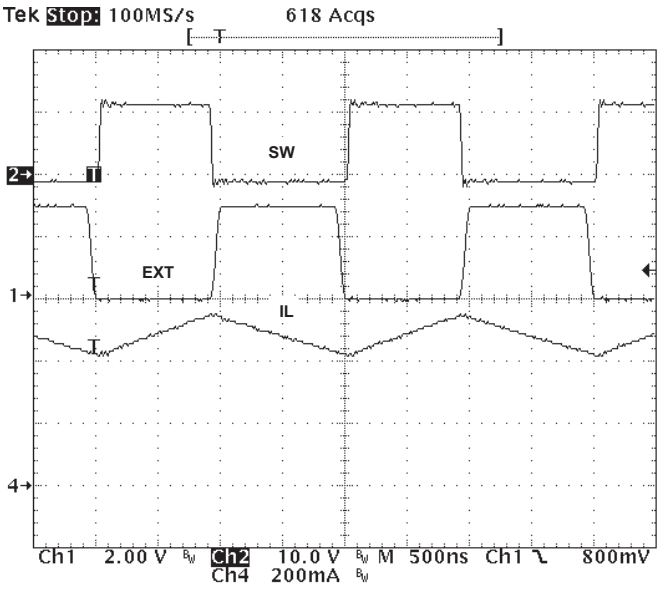

Figure 27. Plot of Synchronizing in CCM

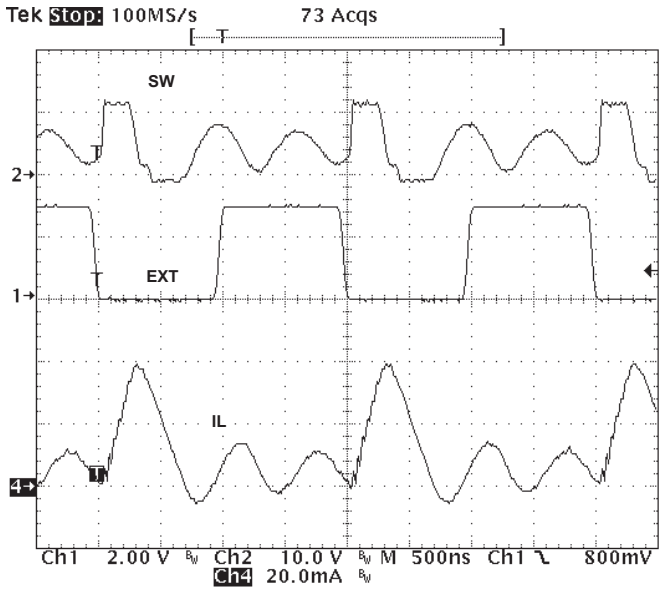

Figure 28. Plot of Synchronizing in DCM

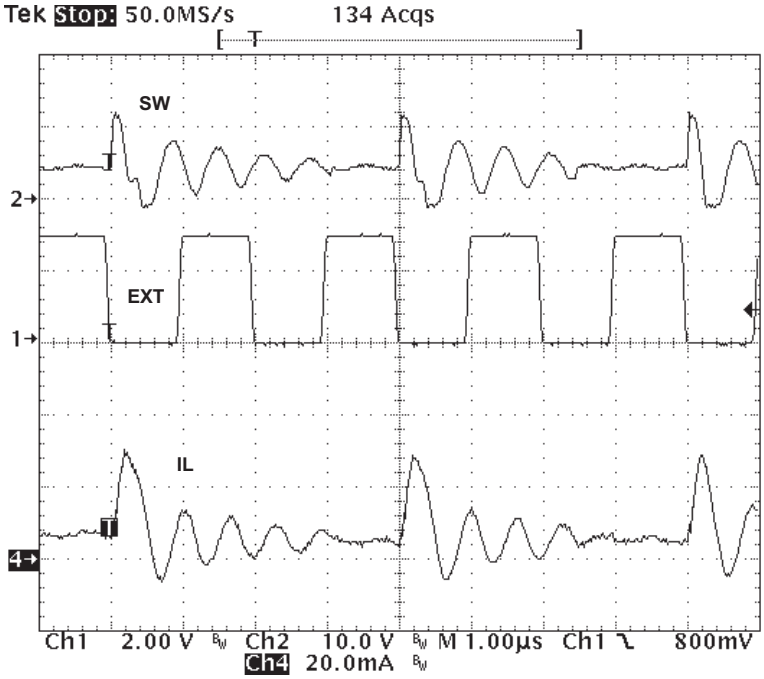

Figure 29. Plot of Synchronizing in Eco-Mode

8.3.12 Overvoltage Protection

The TPS54340 incorporates an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB terminal voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will increase to a maximum voltage corresponding to the peak current limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power supply output voltage can increase faster than the response of the error amplifier output resulting in an output overshoot.

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Feature Description (continued)

The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB terminal voltage to the rising OVP threshold which is nominally 109% of the internal voltage reference. If the FB terminal voltage is greater than the rising OVP threshold, the high side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high side MOSFET resumes normal operation.

8.3.13 Thermal Shutdown

The TPS54340 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 176°C. The high side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature falls below 164°C, the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

8.3.14 Small Signal Model for Loop Response

Figure 30 shows an equivalent model for the TPS54340 control loop which can be simulated to check the frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 3350 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_o and capacitor C_o model the open loop gain and frequency response of the amplifier. The 1mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a provides the small signal response of the frequency compensation. Plotting a/b provides the small signal response of the overall loop. The dynamic loop response can be evaluated by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous conduction mode (CCM) operation.

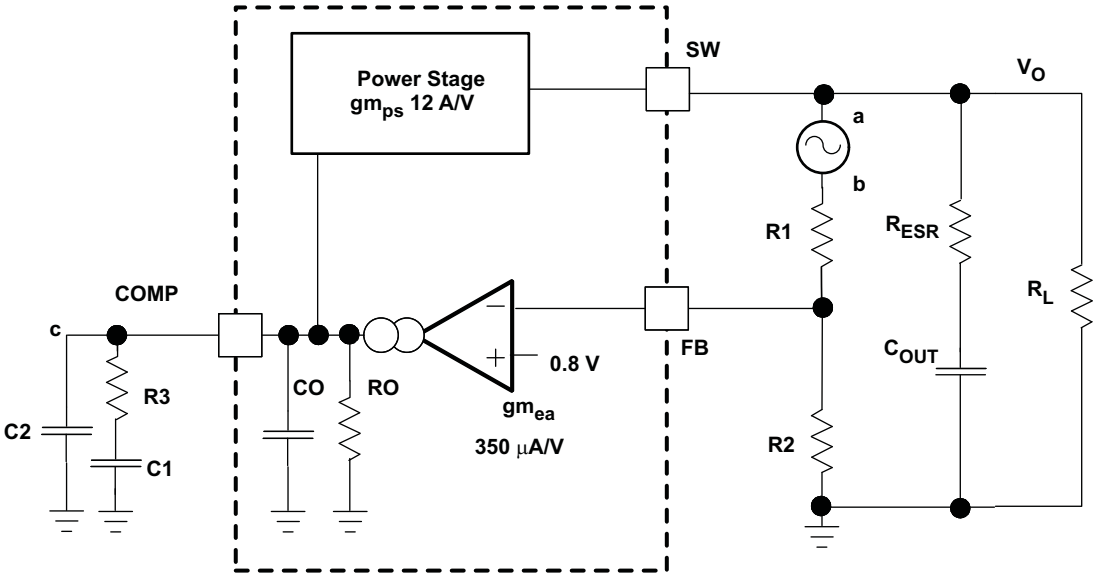

Figure 30. Small Signal Model for Loop Response

8.3.15 Simple Small Signal Model for Peak Current Mode Control

Figure 31 describes a simple small signal model that can be used to design the frequency compensation. The TPS54340 power stage can be approximated by a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 9 and consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP terminal voltage (node c in Figure 30) is the power stage transconductance, gm_{PS}. The gm_{PS} for the TPS54340 is 12 A/V. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in Equation 10.

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Feature Description (continued)

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 11). The combined effect is highlighted by the dashed line in the right half of Figure 31. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin is increased by the ESR zero of the output capacitor (see Equation 12).

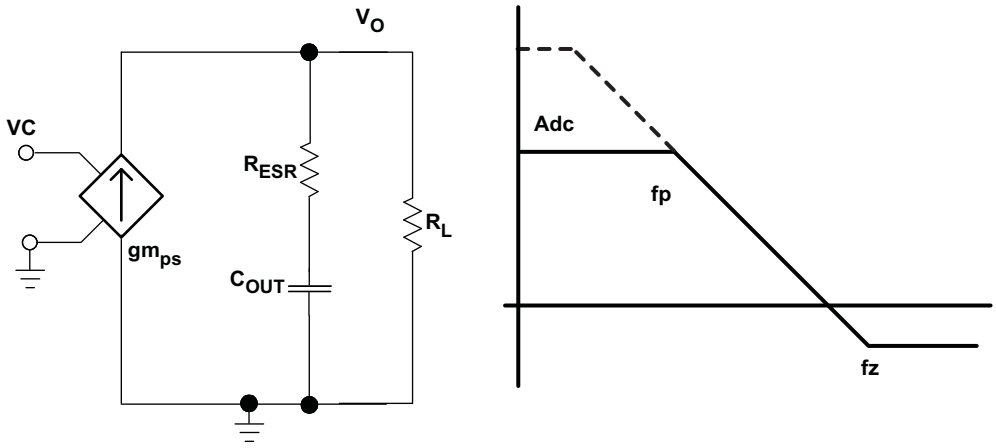

Figure 31. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (9)$$

$$Adc = gm_{ps} \times R_L \quad (10)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (11)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (12)$$

8.3.16 Small Signal Model for Frequency Compensation

The TPS54340 uses a transconductance amplifier for the error amplifier and supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 32. Type 2 circuits are typically implemented in high bandwidth power-supply designs using low ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors. Equation 13 and Equation 14 relate the frequency response of the amplifier to the small signal model in Figure 32. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 32. See the application section for a design example using a Type 2A network with a low ESR output capacitor.

Equation 13 through Equation 22 are provided as a reference. An alternative is to use WEBENCH software tools to create a design based on the power supply requirements.

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Feature Description (continued)

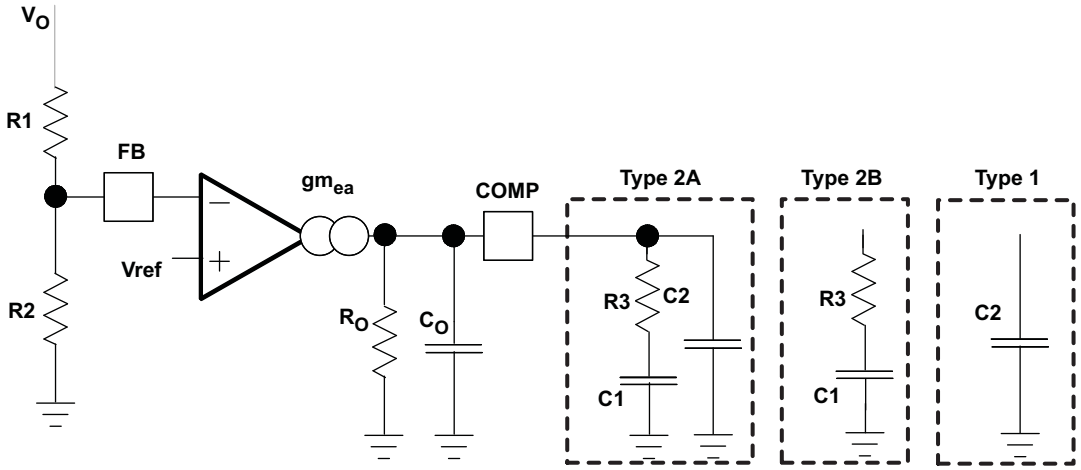

Figure 32. Types of Frequency Compensation

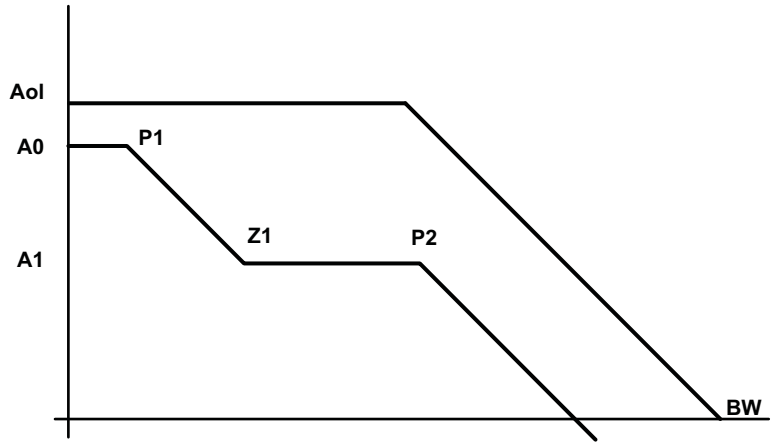

Figure 33. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$Ro = \frac{AoI(V/V)}{gm_{ea}} \quad (13)$$

$$C_O = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \quad (14)$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \quad (15)$$

$$A0 = gm_{ea} \times Ro \times \frac{R2}{R1 + R2} \quad (16)$$

$$A1 = gm_{ea} \times Ro \,||\, R3 \times \frac{R2}{R1 + R2} \quad (17)$$

$$P1 = \frac{1}{2\pi \times Ro \times C1} \quad (18)$$

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Feature Description (continued)

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (19)$$

$$P2 = \frac{1}{2\pi \times R3 \,||\, R_O \times (C2 + C_O)} \text{ type 2a} \quad (20)$$

$$P2 = \frac{1}{2\pi \times R3 \,||\, R_O \times C_O} \text{ type 2b} \quad (21)$$

$$P2 = \frac{1}{2\pi \times R_O \times (C2 + C_O)} \text{ type 1} \quad (22)$$

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8.4 Device Functional Modes

8.4.1 Operation with V_{IN} < 4.5 V (Minimum V_{IN})

The device is recommended to operate with input voltages above 4.5 V. The typical VIN UVLO threshold is 4.3 V and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device will not switch. If EN is externally pulled up to V_{IN} or left floating, when V_{IN} passes the UVLO threshold the device will become active. Switching is enabled the soft start sequence is initiated. The TPS54340 will start at the soft start time determined by the internal soft start time.

8.4.2 Operation with EN Control

The enable threshold voltage is 1.2 V typical. With EN held below that voltage the device is disabled and switching is inhibited even if V_{IN} is above its UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage is increased above the threshold while V_{IN} is above its UVLO threshold, the device becomes active. Switching is enabled, and the soft start sequence is initiated. The TPS54340 will start at the soft start time determined by the internal soft start time.

8.4.3 Alternate Power Supply Topologies

8.4.3.1 Inverting Power

The TPS54340 can be used to convert a positive input voltage to a split rail positive and negative output voltage by using a coupled inductor. Idea applications are amplifiers requiring a split rail positive and negative voltage power supply. For a more detailed example see SLVA369.

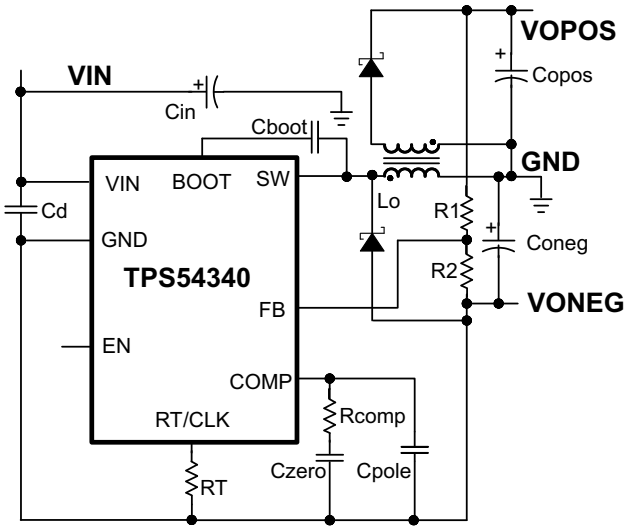

Figure 34. TPS54340 Split Rail Power Supply

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Device Functional Modes (continued)

8.4.3.2 Split Rail Power Supply

The TPS54340 can be used to convert a positive input voltage to a negative output voltage. Idea applications are amplifiers requiring a negative power supply. For a more detailed example see SLVA317.

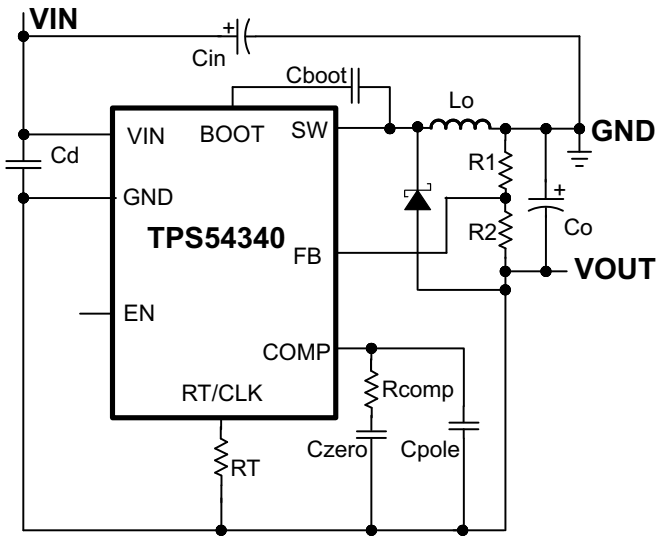

Figure 35. TPS54340 Inverting Power Supply from SLVA317 Application Note

9 Application and Implementation

9.1 Application Information

The TPS54340 is a 42 V, 3.5 A, step down regulator with an integrated high side MOSFET. Idea applications are: 12 V, 24 V Industrial, Automotive and Communications Power Systems.

9.2 Typical Application

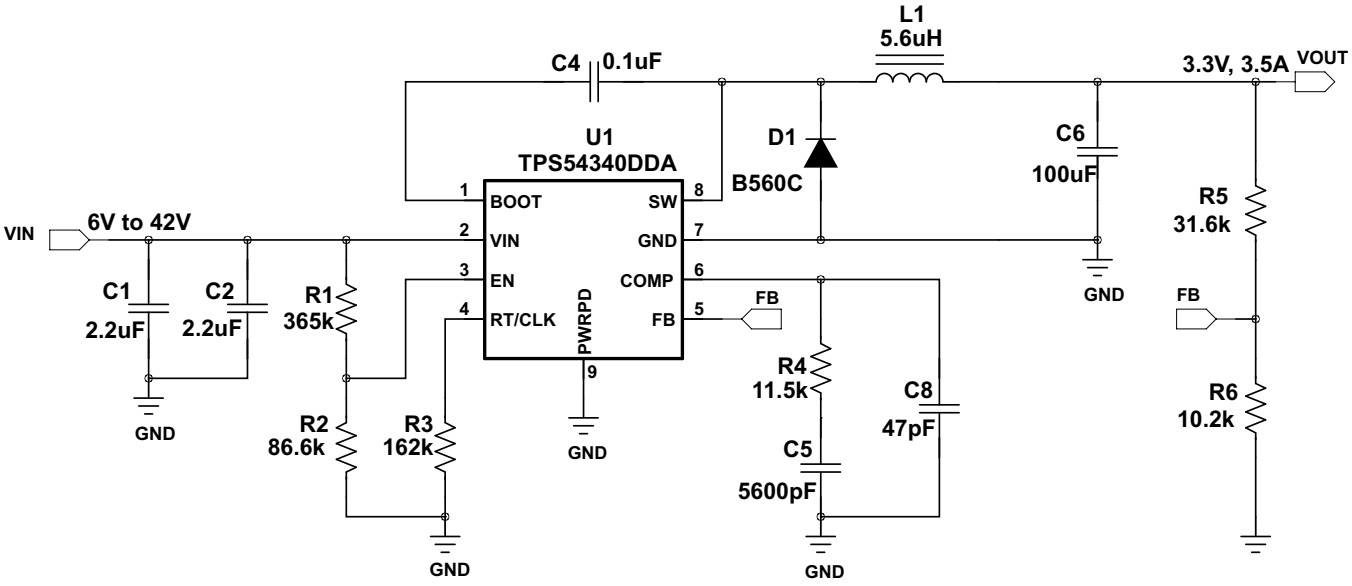

Figure 36. 3.3 V Output TPS54340 Design Example

9.2.1 Design Requirements

This guide illustrates the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These requirements are typically determined at the system level. For this example, we will start with the following known parameters:

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Output Voltage	3.3 V
Transient Response 0.875 A to 2.625 A load step	ΔV_{OUT} = 4 %
Maximum Output Current	3.5 A
Input Voltage	12 V nom. 6 V to 42 V
Output Voltage Ripple	0.5% of V_{OUT}
Start Input Voltage (rising VIN)	5.75 V
Stop Input Voltage (falling VIN)	4.5 V

9.2.2 Detailed Design Procedures

9.2.2.1 Selecting the Switching Frequency

The first step is to choose a switching frequency for the regulator. Typically, the designer uses the highest switching frequency possible since this produces the smallest solution size. High switching frequency allows for lower value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage and the frequency foldback protection.

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Equation 7 and Equation 8 should be used to calculate the upper limit of the switching frequency for the regulator. Choose the lower value result from the two equations. Switching frequencies higher than these values results in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 135 ns for the TPS54340. For this example, the output voltage is 3.3 V and the maximum input voltage is 42 V, which allows for a maximum switch frequency up to 712 kHz to avoid pulse skipping from Equation 7. To ensure overcurrent runaway is not a concern during short circuits use Equation 8 to determine the maximum switching frequency for frequency foldback protection. With a maximum input voltage of 42 V, assuming a diode voltage of 0.7 V, inductor resistance of 21 mΩ, switch resistance of 92 mΩ, a current limit value of 4.7 A and short circuit output voltage of 0.1 V, the maximum switching frequency is 1260 kHz.

For this design, a lower switching frequency of 600 kHz is chosen to operate comfortably below the calculated maximums. To determine the timing resistance for a given switching frequency, use Equation 5 or the curve in Figure 7. The switching frequency is set by resistor R_3 shown in Figure 36. For 600 kHz operation, the closest standard value resistor is 162 kΩ.

$$f_{SW(max\,skip)} = \frac{1}{135ns} \times \left(\frac{3.5\ A \times 21\ m\Omega + 3.3\ V + 0.7\ V}{42\ V - 3.5\ A \times 92\ m\Omega + 0.7\ V} \right) = 712\ kHz \quad (23)$$

$$f_{SW(shift)} = \frac{8}{135\ ns} \times \left(\frac{4.7\ A \times 21\ m\Omega + 0.1\ V + 0.7\ V}{42\ V - 4.7\ A \times 92\ m\Omega + 0.7\ V} \right) = 1260\ kHz \quad (24)$$

$$RT\ (k\Omega) = \frac{92417}{600\ (kHz)^{0.991}} = 163\ k\Omega \quad (25)$$

9.2.2.2 Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 26.

K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer, however, the following guidelines may be used.

For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be desirable. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Since the inductor ripple current is part of the current mode PWM control system, the inductor ripple current should always be greater than 150 mA for stable PWM operation. In a wide input voltage regulator, it is best to choose relatively large inductor ripple current. This provides sufficienct ripple current with the input voltage at the minimum.

For this design example, K_{IND} = 0.3 and the minimum inductor value is calculated to be 4.8 µH. The nearest standard value is 5.6 µH. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from Equation 28 and Equation 29. For this design, the RMS inductor current is 3.5 A and the peak inductor current is 3.95 A. The chosen inductor is a WE 7443552560, which has a saturation current rating of 7.5 A and an RMS current rating of 6.7 A.

As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative design approach is to choose an inductor with a saturation current rating equal to or greater than the switch current limit of the TPS54340 which is nominally 5.5 A.

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$$L_{O(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} = \frac{42\ V\ -\ 3.3\ V}{3.5\ A\ x\ 0.3} \times \frac{3.3\ V}{42\ V \times 600\ kHz} = 4.8\ \mu H \quad (26)$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} = \frac{3.3\ V\ x\ (42\ V\ -\ 3.3\ V)}{42\ V\ x\ 5.6\ \mu H\ x\ 600\ kHz} = 0.905\ A \quad (27)$$

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_O \times f_{SW}} \right)^2} = \sqrt{(3.5\ A)^2 + \frac{1}{12} \times \left(\frac{3.3\ V \times (42\ V\ -\ 3.3\ V)}{42\ V \times 5.6\ \mu H \times 600\ kHz} \right)^2} = 3.5\ A \quad (28)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 3.5\ A + \frac{0.905\ A}{2} = 3.95\ A \quad (29)$$

9.2.2.3 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the increased load current until the regulator responds to the load step. The regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to supply the difference in current for 2 clock cycles to maintain the output voltage within the specified range. Equation 30 shows the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current, $f$sw is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 0.875 A to 2.625 A. Therefore, ΔI_{OUT} is 2.625 A - 0.875 A = 1.75 A and ΔV_{OUT} = 0.04 × 3.3 = 0.13 V. Using these numbers gives a minimum capacitance of 44.9 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be included in load step calculations.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The catch diode of the regulator can not sink current so energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. A typical load step response is shown in . The excess energy absorbed in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 31 calculates the minimum capacitance required to keep the output voltage overshoot to a desired value, where L_O is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the peak output voltage, and V_I is the initial voltage. For this example, the worst case load step will be from 2.625 A to 0.875 A. The output voltage increases during this load transition and the stated maximum in our specification is 4 % of the output voltage. This makes V_f = 1.04 × 3.3 = 3.432. Vi is the initial capacitor voltage which is the nominal output voltage of 3.3 V. Using these numbers in Equation 31 yields a minimum capacitance of 38.6 µF.

Equation 32 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where $f$sw is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. Equation 32 yields 11.4 µF.

Equation 33 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 33 indicates the ESR should be less than 18 mΩ.

The most stringent criteria for the output capacitor is 44.9 µF required to maintain the output voltage within regulation tolerance during a load transient.

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Capacitance de-ratings for aging, temperature and dc bias increases this minimum value. For this example, 100 µF ceramic capacitors with 5 mΩ of ESR is used. The derated capacitance is 70 µF, well above the minimum required capacitance of 44.9 µF.

Capacitors are generally rated for a maximum ripple current that can be filtered without degrading capacitor reliability. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. Equation 34 can be used to calculate the RMS ripple current that the output capacitor must support. For this example, Equation 34 yields 261 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 1.75\ A}{600\ kHz \times 0.13\ V} = 44.9\ \mu F \quad (30)$$

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_I)^2\right)} = 5.6\ \mu H \times \frac{\left(2.625\ A^2 - 0.875\ A^2\right)}{\left(3.432\ V^2 - 3.3\ V^2\right)} = 38.6\ \mu F \quad (31)$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{ORIPPLE}}{I_{RIPPLE}}\right)} = \frac{1}{8 \times 600\ kHz} \times \frac{1}{\left(\frac{16.5\ mV}{0.905\ A}\right)} = 11.4\ \mu F \quad (32)$$

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} = \frac{16.5\ mV}{0.905\ A} = 18\ m\Omega \quad (33)$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} = \frac{3.3\ V \times (42\ V - 3.3\ V)}{\sqrt{12} \times 42\ V \times 5.6\ \mu H \times 600\ kHz} = 261\ mA \quad (34)$$

9.2.2.4 Catch Diode

The TPS54340 requires an external catch diode between the SW terminal and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 42 V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the TPS54340.

For the example design, the B560C-13-F Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the B560C-13-F is 0.70 volts at 5 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 35 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The B560C-13-F diode has a junction capacitance of 300 pF. Using Equation 35, the total loss in the diode is 2.42 Watts.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times Vfd}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times \left(V_{IN} + Vfd\right)^2}{2} =$$

$$\frac{(42\ V - 3.3\ V) \times 3.5\ A \times 0.7\ V}{42\ V} + \frac{300\ pF \times 600\ kHz \times (42\ V + 0.7\ V)^2}{2} = 2.42\ W \quad (35)$$

9.2.2.5 Input Capacitor

The TPS54340 requires a high quality ceramic type X5R or X7R input decoupling capacitor with at least 3 µF of effective capacitance. Some applications will benefit from additional bulk capacitance. The effective capacitance includes any loss of capacitance due to dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54340. The input ripple current can be calculated using Equation 36.

The value of a ceramic capacitor varies significantly with temperature and the dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is more stable over temperature. X5R and X7R ceramic dielectrics are usually selected for switching regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with consideration for the dc bias. The effective value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 42 V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V or 100 V. For this example, two 2.2 µF, 100 V capacitors in parallel are used. Table 2 shows several choices of high voltage capacitors.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 37. Using the design example values, I_{OUT} = 3.5 A, C_{IN} = 4.4 µF, $f$sw = 600 kHz, yields an input voltage ripple of 331 mV and a rms input ripple current of 1.74 A.

$$I_{CI(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} = 3.5\ A \sqrt{\frac{3.3\ V}{6\ V} \times \frac{(6\ V\ -\ 3.3\ V)}{6\ V}} = 1.74\ A \tag{36}$$

$$\Delta V_{IN} = \frac{I_{OUT} \times 0.25}{C_{IN} \times f_{SW}} = \frac{3.5\ A \times 0.25}{4.4\ \mu F \times 600\ kHz} = 331\ mV \tag{37}$$

Table 2. Capacitor Types

VALUE (µF)	EIA Size	VOLTAGE	DIALECTRIC	COMMENTS
1 to 2.2	1210	100 V	X7R	GRM32 series
1 to 4.7		50 V		
1	1206	100 V		GRM31 series
1 to 2.2		50 V		
1 to 1.8	2220	50 V		VJ X7R series
1 to 1.2		100 V		
1 to 3.9	2225	50 V		
1 to 1.8		100 V		
1 to 2.2	1812	100 V		C series C4532
1.5 to 6.8		50 V		
1 to 2.2	1210	100 V		C series C3225
1 to 3.3		50 V		
1 to 4.7	1210	50 V		X7R dielectric series
1		100 V		
1 to 4.7	1812	50 V		
1 to 2.2		100 V		

9.2.2.6 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and SW terminals for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10 V or higher voltage rating.

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9.2.2.7 Undervoltage Lockout Set Point

The Undervoltage Lockout (UVLO) can be adjusted using an external voltage divider on the EN terminal of the TPS54340. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.75 V (UVLO start). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.5 V (UVLO stop).

Programmable UVLO threshold voltages are set using the resistor divider of R_{UVLO1} and R_{UVLO2} between Vin and ground connected to the EN terminal. Equation 2 and Equation 3 calculate the resistance values necessary. For the example application, a 365 kΩ between Vin and EN (R_{UVLO1}) and a 86.6 kΩ between EN and ground (R_{UVLO2}) are required to produce the 8 V and 6.25 V start and stop voltages.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} = \frac{5.75\ V - 4.5\ V}{3.4\ \mu A} = 368\ k\Omega \tag{38}$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} = \frac{1.2\ V}{\frac{5.75\ V - 1.2\ V}{365\ k\Omega} + 1.2\ \mu A} = 87.8\ k\Omega \tag{39}$$

9.2.2.8 Output Voltage and Feedback Resistors Selection

The voltage divider of R5 and R6 sets the output voltage. For the example design, 10.2 kΩ was selected for R6. Using Equation 1, R5 is calculated as 31.9 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Due to the input current of the FB terminal, the current flowing through the feedback network should be greater than 1 µA to maintain the output voltage accuracy. This requirement is satisfied if the value of R6 is less than 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents but may also introduce noise immunity problems.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - 0.8\ V}{0.8\ V} = 10.2\ k\Omega \times \left(\frac{3.3\ V - 0.8\ V}{0.8\ V}\right) = 31.9\ k\Omega \tag{40}$$

9.2.2.9 Compensation

There are several methods to design compensation for DC-DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual crossover frequency will be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole.

To get started, the modulator pole, $f_{p(mod)}$, and the ESR zero, f_{z1} must be calculated using Equation 41 and Equation 42. For C_{OUT}, use a derated value of 70 µF. Use equations Equation 43 and Equation 44 to estimate a starting point for the crossover frequency, $f$co. For the example design, $f_{p(mod)}$ is 2411 Hz and $f_{z(mod)}$ is 455 kHz. Equation 42 is the geometric mean of the modulator pole and the ESR zero and Equation 44 is the mean of modulator pole and the switching frequency. Equation 43 yields 33.1 kHz and Equation 44 gives 26.9 kHz. Use the lower value of Equation 43 or Equation 44 for an initial crossover frequency. For this example, the target $f$co is 26.9 kHz.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} = \frac{3.5\ A}{2 \times \pi \times 3.3\ V \times 70\ \mu F} = 2411\ Hz \tag{41}$$

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2 \times \pi \times 5\ m\Omega \times 70\ \mu F} = 455\ kHz \tag{42}$$

$$f_{co} = \sqrt{f_{p(mod)} \times f_{z(mod)}} = \sqrt{2411\ Hz \times 455\ kHz} = 33.1\ kHz \tag{43}$$

$$f_{co} = \sqrt{f_{p(mod)} \times \frac{f_{SW}}{2}} = \sqrt{2411\ Hz \times \frac{600\ kHz}{2}} = 26.9\ kHz \tag{44}$$

To determine the compensation resistor, R4, use Equation 45. Assume the power stage transconductance, gmps, is 12 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 5 V, 0.8 V and 350 µA/V, respectively. R4 is calculated to be 11.6 kΩ and a standard value of 11.5 kΩ is selected. Use Equation 46 to set the compensation zero to the modulator pole frequency. Equation 46 yields 5740 pF for compensating capacitor C5. 5600 pF is used for this design.

$$R4 = \left(\frac{2 \times \pi \times f_{co} \times C_{OUT}}{gmps}\right) x \left(\frac{V_{OUT}}{V_{REF} \text{ x } gmea}\right) = \left(\frac{2 \times \pi \times 26.9 \text{ kHz} \times 70\ \mu F}{12 \text{ A/V}}\right) x \left(\frac{3.3 \text{ V}}{0.8 \text{ V x } 350\ \mu\text{A/V}}\right) = 11.6\ k\Omega \quad (45)$$

$$C5 = \frac{1}{2 \times \pi \times R4 \text{ x } f_{p(mod)}} = \frac{1}{2 \times \pi \times 11.5\ k\Omega \text{ x } 2411 \text{ Hz}} = 5740 \text{ pF} \quad (46)$$

A compensation pole can be implemented if desired by adding capacitor C8 in parallel with the series combination of R4 and C5. Use the larger value calculated from Equation 47 and Equation 48 for C8 to set the compensation pole. The selected value of C8 is 47 pF for this design example.

$$C8 = \frac{C_{OUT} \text{ x } R_{ESR}}{R4} = \frac{70\ \mu F \text{ x } 5\ m\Omega}{11.5\ k\Omega} = 30.4 \text{ pF} \quad (47)$$

$$C8 = \frac{1}{R4 \text{ x } f\text{sw x } \pi} = \frac{1}{11.5\ k\Omega \text{ x } 600 \text{ kHz x } \pi} = 46.1 \text{ pF} \quad (48)$$

9.2.2.10 Discontinuous Conduction Mode and Eco-mode Boundary

With an input voltage of 12 V, the power supply enters discontinuous conduction mode when the output current is less than 342 mA. The power supply enters Eco-mode when the output current is lower than 31.4 mA. The input current draw is 237 µA with no load.

9.2.2.11 Power Dissipation

The following formulas show how to estimate the TPS54340 power dissipation under continuous conduction mode (CCM) operation. These equations should not be used if the device is operating in discontinuous conduction mode (DCM).

The power dissipation of the IC includes conduction loss (P_{COND}), switching loss (P_{SW}), gate drive loss (P_{GD}) and supply current (P_Q). Example calculations are shown with the 12 V typical input voltage of the design example.

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \times \left(\frac{V_{OUT}}{V_{IN}}\right) = 3.5\ A^2 \times 92\ m\Omega \times \frac{3.3 \text{ V}}{12 \text{ V}} = 0.31 \text{ W} \quad (49)$$

$$P_{SW} = V_{IN} \times f_{SW} \times I_{OUT} \times t_{rise} = 12 \text{ V} \times 600 \text{ kHz} \times 3.5 \text{ A} \times 4.9 \text{ ns} = 0.123 \text{ W} \quad (50)$$

$$P_{GD} = V_{IN} \times Q_G \times f_{SW} = 12 \text{ V} \times 3nC \times 600 \text{ kHz} = 0.022 \text{ W} \quad (51)$$

$$P_Q = V_{IN} \times I_Q = 12 \text{ V} \times 146\ \mu A = 0.0018 \text{ W} \quad (52)$$

Where:

I_{OUT} is the output current (A).

$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).

V_{OUT} is the output voltage (V).

V_{IN} is the input voltage (V).

***f*sw** is the switching frequency (Hz).

trise is the SW terminal voltage rise time and can be estimated by trise = V_{IN} x 0.16ns/V + 3.0ns.

Q_G is the total gate charge of the internal MOSFET.

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I_Q is the operating nonswitching supply current.

Therefore,

$$P_{TOT} = P_{COND} + P_{SW} + P_{GD} + P_Q = 0.31\ W + 0.123\ W + 0.022\ W + 0.0018\ W = 0.457\ W \quad (53)$$

For given T_A,

$$T_J = T_A + R_{TH} \times P_{TOT} \quad (54)$$

For given T_{JMAX} = 150°C

$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT} \quad (55)$$

Where:

Ptot is the total device power dissipation (W),

T_A is the ambient temperature (°C).

T_J is the junction temperature (°C).

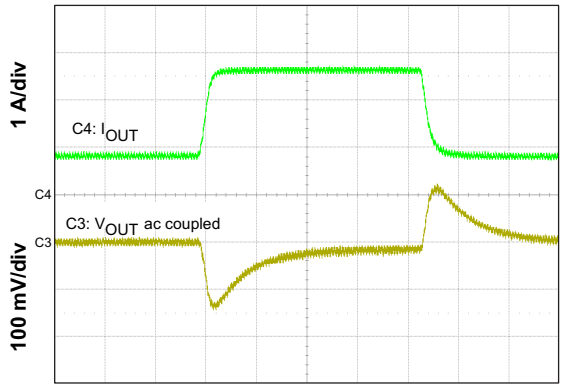
R_{TH} is the thermal resistance of the package (°C/W).

T_{JMAX} is maximum junction temperature (°C)

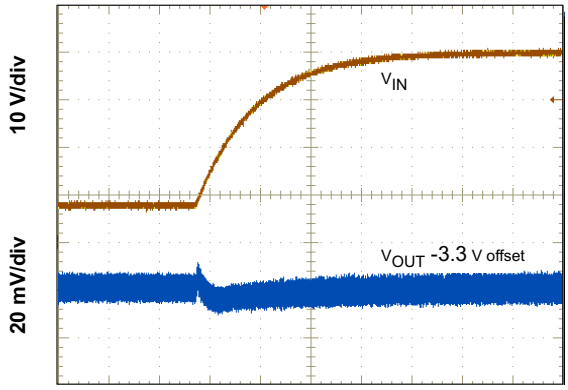
T_{AMAX} is maximum ambient temperature (°C).

There will be additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode and PCB trace resistance impacting the overall efficiency of the regulator.

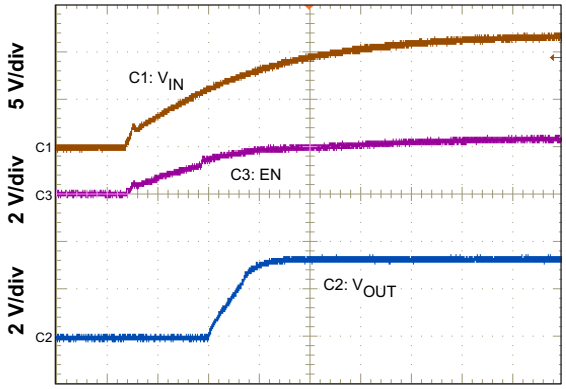
9.2.3 Application Curves



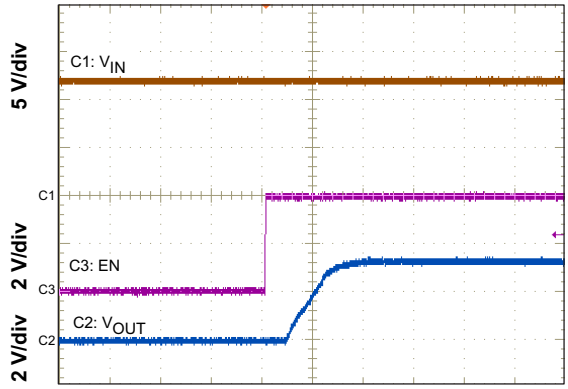
Time = 100 µs/div
Figure 37. Load Transient



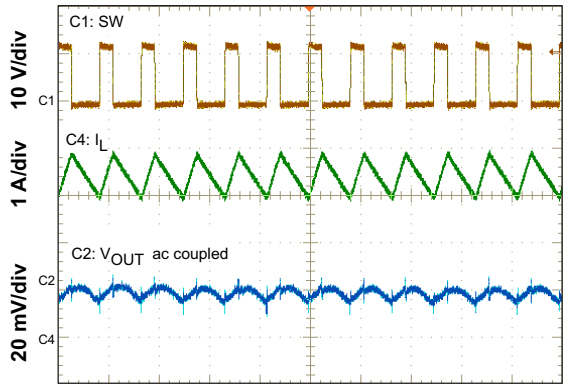
Time = 4 ms/div
Figure 38. Line Transient (8 V to 40 V)



Time = 2 ms/div
Figure 39. Start-up With VIN



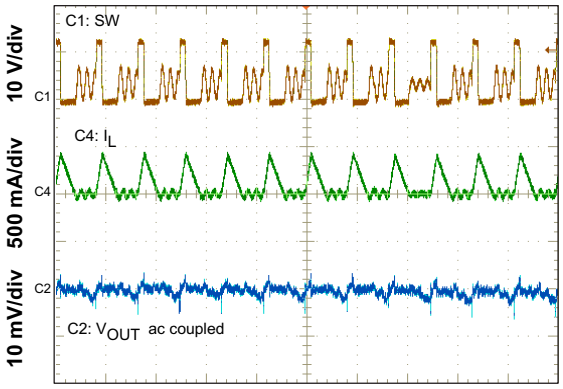
Time = 2 ms/div
Figure 40. Start-up With EN



Time = 2 µs/div

I_{OUT} = 3.5 A

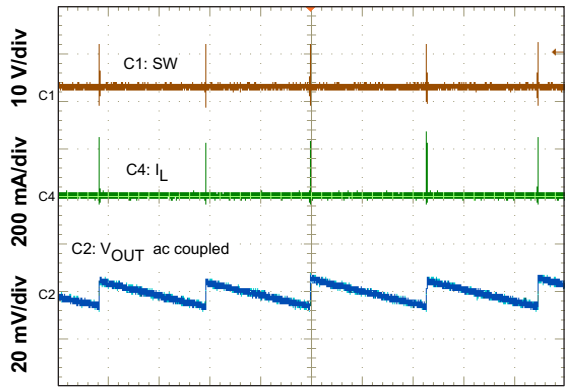
Figure 41. Output Ripple CCM



Time = 2 µs/div

I_{OUT} = 100 mA

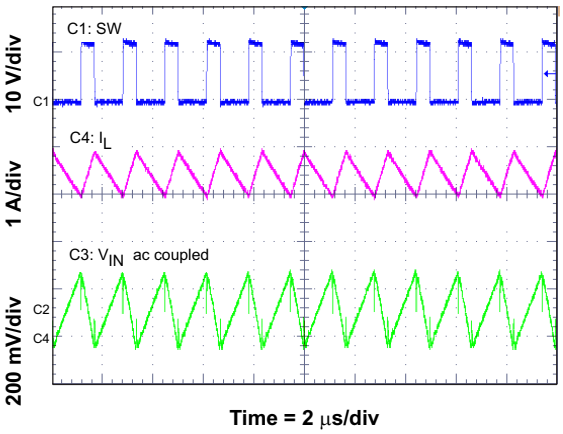
Figure 42. Output Ripple DCM



Time = 2 ms/div

No Load

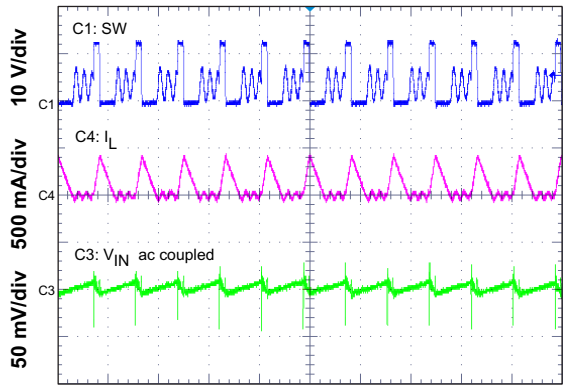
Figure 43. Output Ripple PSM



Time = 2 µs/div

I_{OUT} = 3.5 A

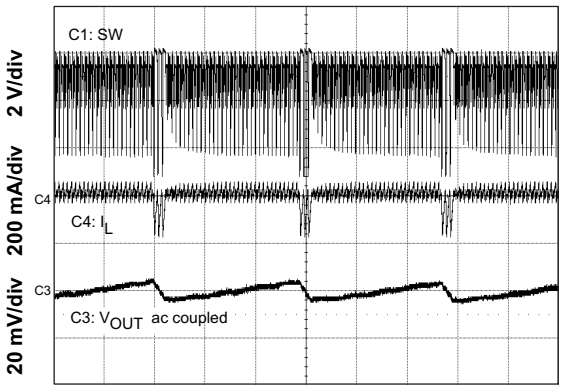
Figure 44. Input Ripple CCM



Time = 2 µs/div

I_{OUT} = 100 mA

Figure 45. Input Ripple DCM



Time = 20 µs/div

V_{IN} = 5.5 V No Load

V_{OUT} = 5 V EN Floating

Figure 46. Low Dropout Operation

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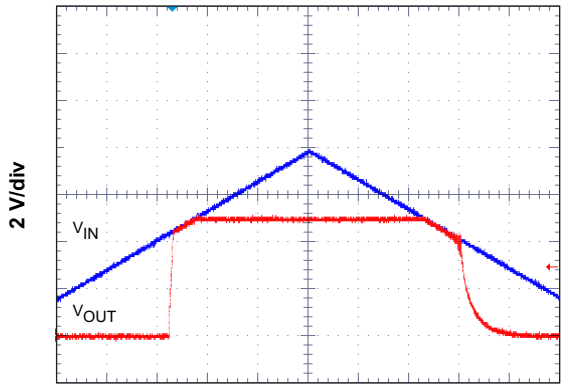
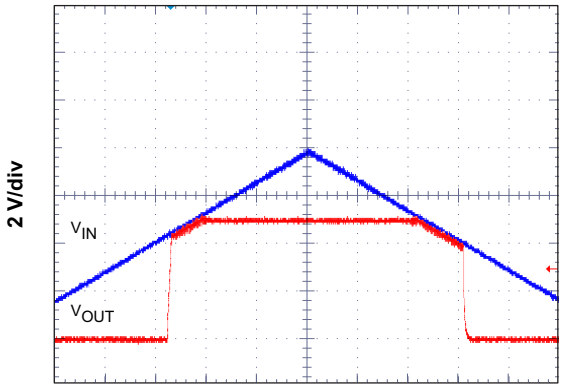


Time = 40 μs/div

I_{OUT} = 100 mA EN Floating

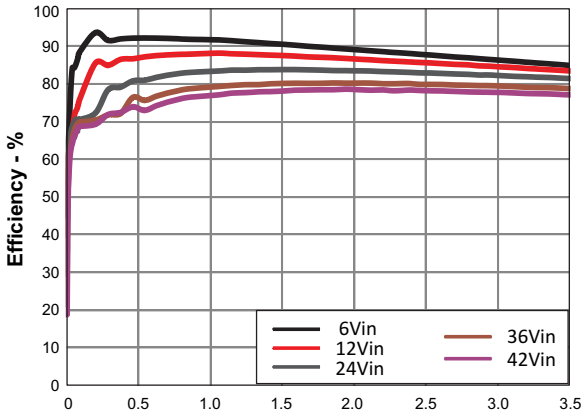
Figure 47. Low Dropout Operation



Time = 40 μs/div

I_{OUT} = 1 A EN Floating

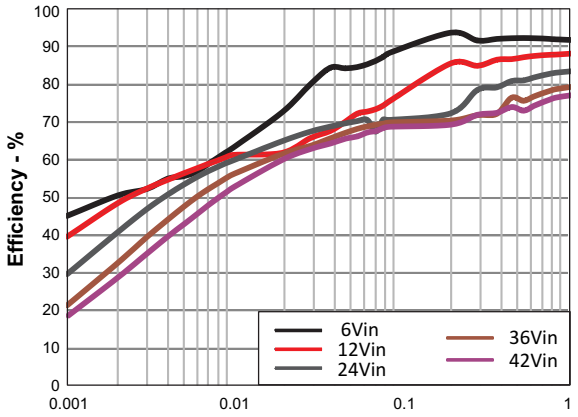
Figure 48. Low Dropout Operation



I_O - Output Current - A

V_{OUT} = 3.3 V $f$sw = 600 kHz

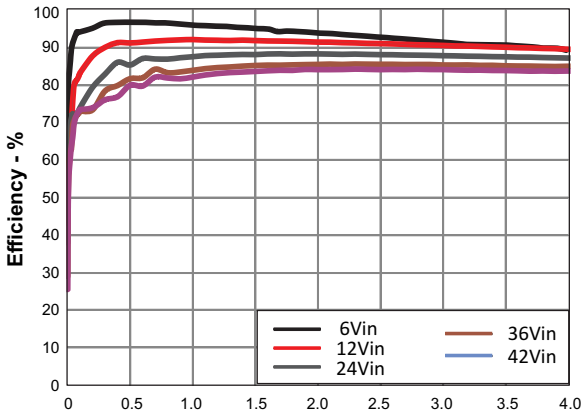
Figure 49. Efficiency vs Load Current



I_O - Output Current - A

V_{OUT} = 3.3 V $f$sw = 600 kHz

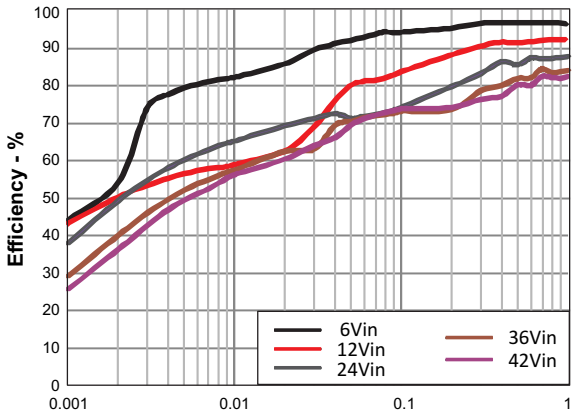
Figure 50. Light Load Efficiency



I_O - Output Current - A

V_{OUT} = 5 V $f$sw = 600 kHz

Figure 51. Efficiency vs Load Current



I_O - Output Current - A

V_{OUT} = 5 V $f$sw = 600 kHz

Figure 52. Light Load Efficiency

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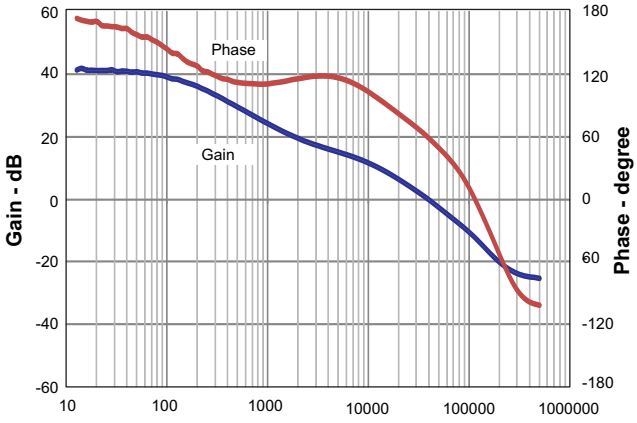
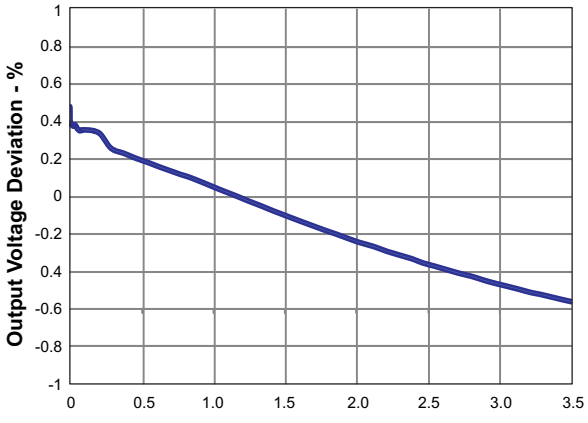


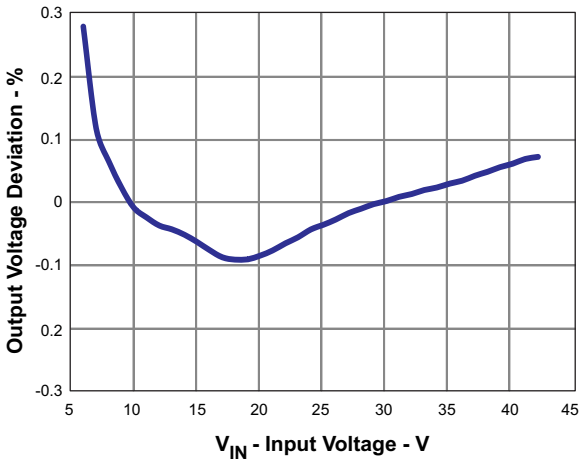
V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 3.5 A

Figure 53. Overall Loop Frequency Response



V_{IN} = 12 V V_{OUT} = 3.3 V f_{sw} = 600 kHz

Figure 54. Regulation vs Load Current



V_{OUT} = 3.3 V I_{OUT} = 3.5 A f_{sw} = 600 kHz

Figure 55. Regulation vs Input Voltage

10 Power Supply Recommendations

The device are designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS54340 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

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11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance

- To reduce parasitic effects, the VIN terminal should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN terminal, and the anode of the catch diode.
- The GND terminal should be tied directly to the power pad under the IC and the PowerPAD™.
- The PowerPAD™ should be connected to internal PCB ground planes using multiple vias directly under the IC.
- The SW terminal should be routed to the cathode of the catch diode and to the output inductor.
- Since the SW connection is the switching node, the catch diode and output inductor should be located close to the SW terminals, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- For operation at full rated load, the top side ground area must provide adequate heat dissipating area.
- The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
- The additional external components can be placed approximately as shown.
- It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

11.2 Layout Example

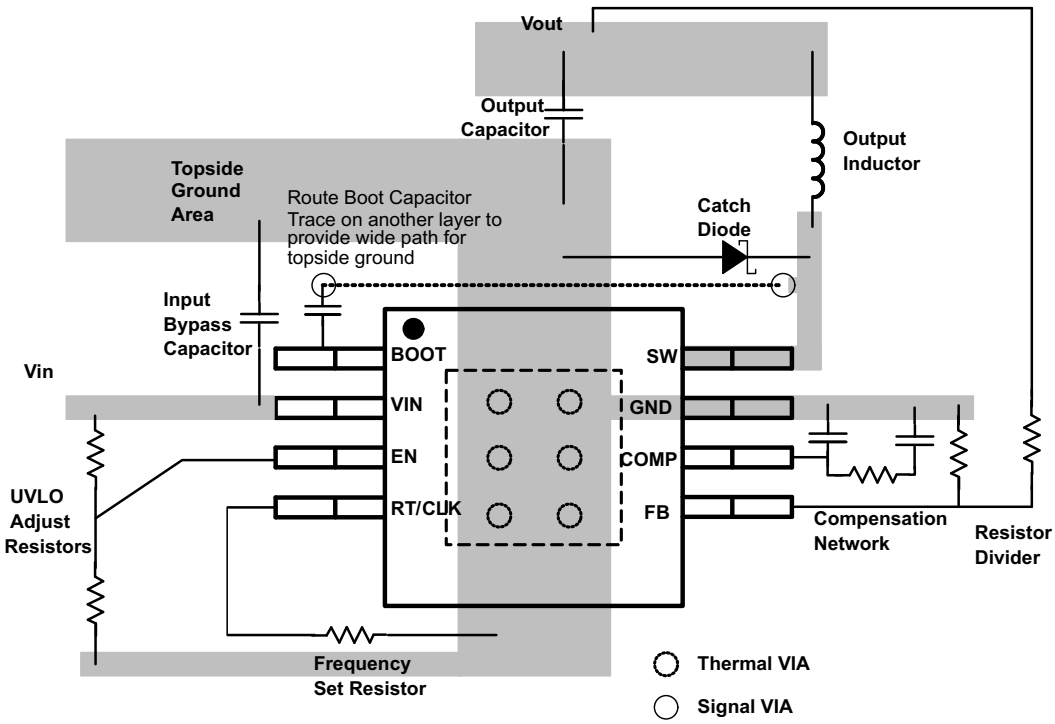

Figure 56. PCB Layout Example

11.2.1 Estimated Circuit Area

Boxing in the components in the design of Figure 36 the estimated printed circuit board area is 1.025 in^2 (661 mm^2). This area does not include test points or connectors.

12 Device and Documentation Support

12.1 Trademarks

Eco-mode, PowerPAD, WEBENCH are trademarks of Texas Instruments.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54340DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	54340	Samples
TPS54340DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	54340	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS54340 :

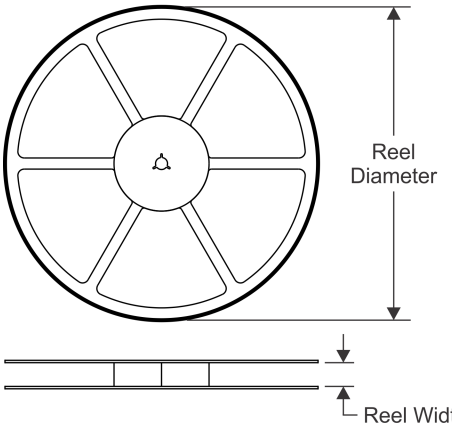
- Automotive: TPS54340-Q1

NOTE: Qualified Version Definitions:

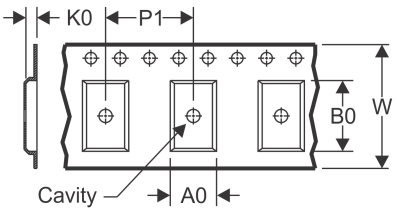
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

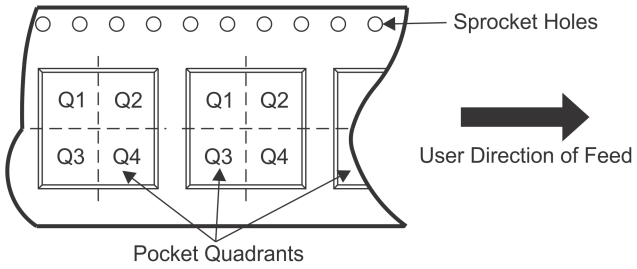


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

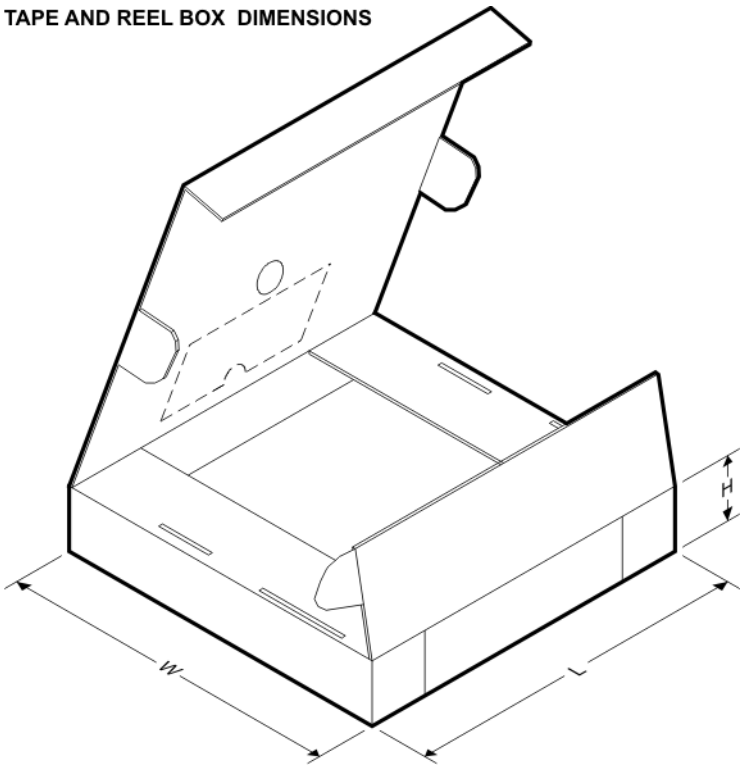
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54340DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

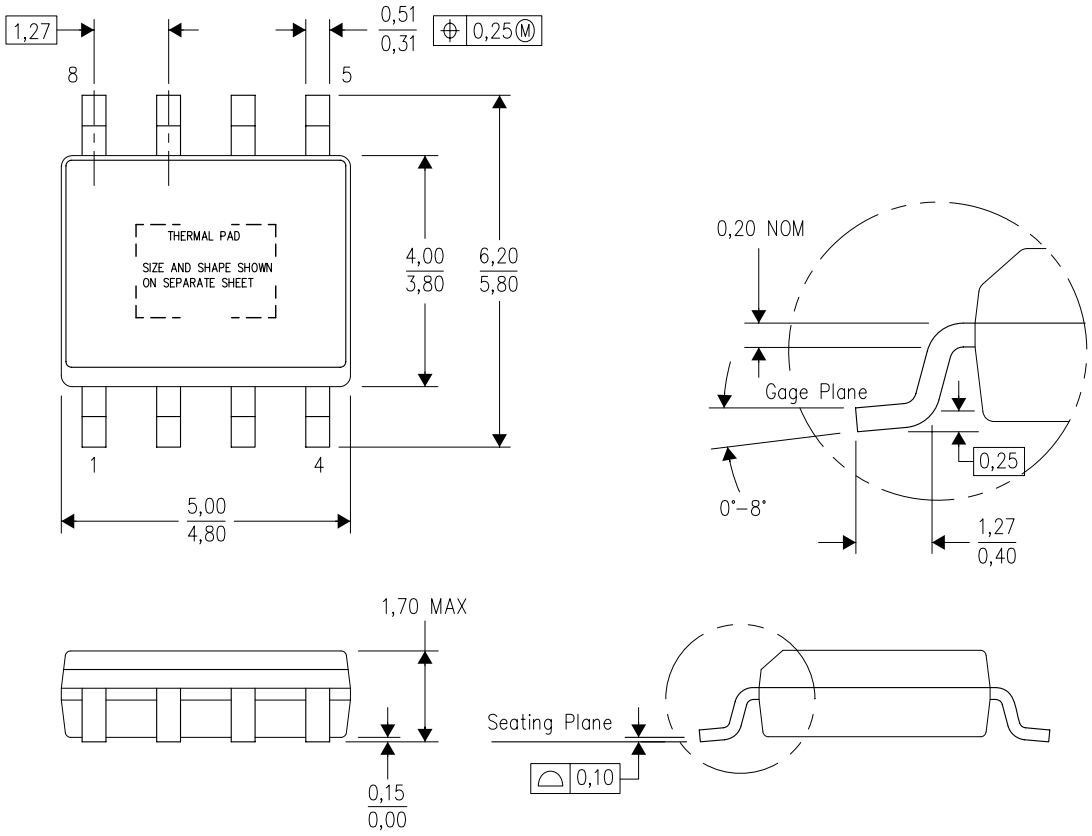
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54340DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

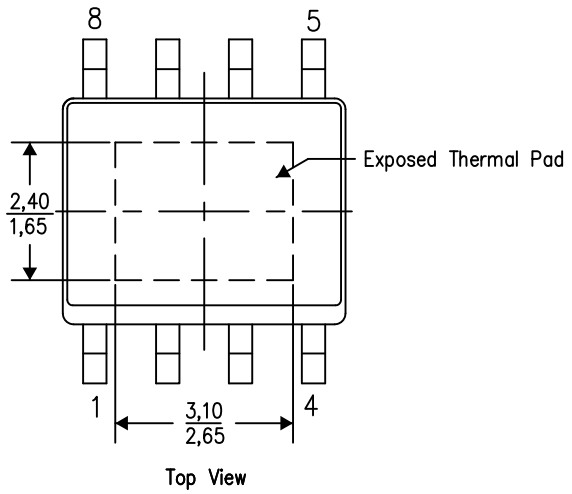
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



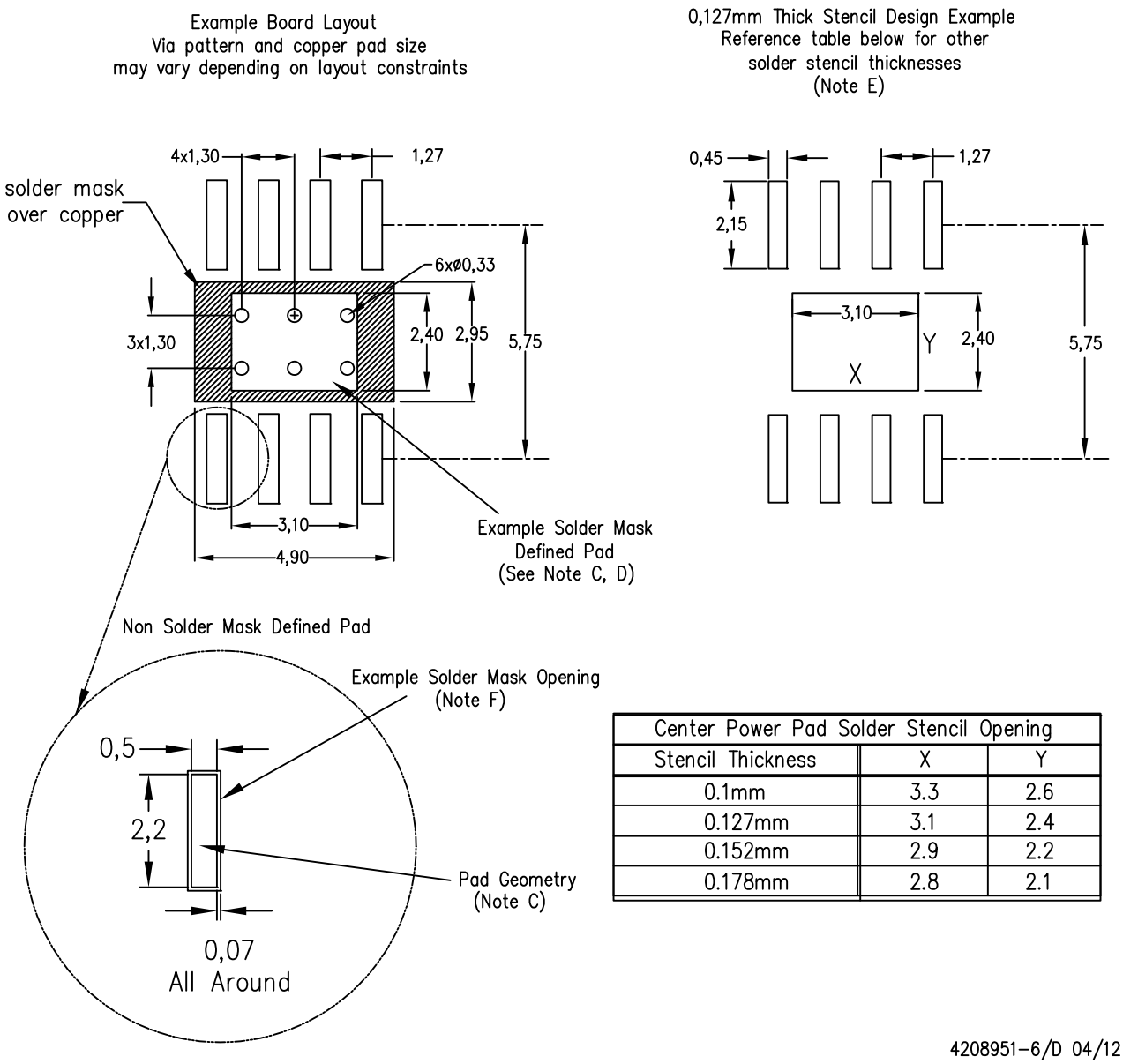
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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