NR263S

DATA SHEET

General Descriptions

The NR263S is Synchronous Rectification buck regulator ICs integrates PowerMOSFETs. With the current mode control, ultra low ESR capacitors such as ceramic capacitors can be used. The ICs can realize super-high efficiency by performing pulse skip operation at light load condition. The ICs have protection functions such as Over-Current Protection (OCP), Under-Voltage Lockout (UVLO) and Thermal Shutdown (TSD). Soft starting time can be set up by selecting an external capacitor value. The ON/OFF pin (EN Pin) turns the regulator ON/OFF. The NR263S is available in an 8-pin SOP package.

Features & Benefits

- Synchronous Rectification with internal PowerMOSFETs
- Current mode PWM control (Normal load)
- Pulse Skip Operation(at Light Load Condition)
- Up to 94% efficiency at normal load condition
- Up to 86% efficiency at light load condition (@Vin=12V,Vout=5V,Iout=10mA)
- Stable with low ESR ceramic output capacitors
- Built-in protection function
  Drooping type Over Current Protection (OCP) with Auto-restart
  Thermal Shutdown (TSD) with Auto-restart
  Under Voltage Lockout(UVLO)
  Vo Short Circuit Protection (HICCUP)
- By Vo = 5V fixed and external component count reduction (NR263S)
- Soft-start Function by External Timing Capacitor
- Turn ON/OF the regulator function

Package

SOP8 Package

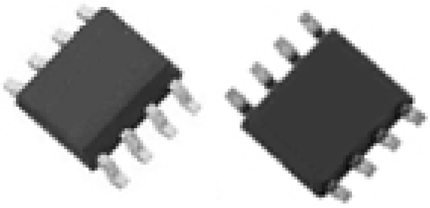


*Image: Not to scale

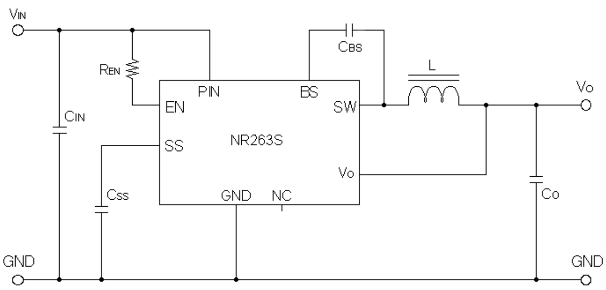
Electrical Characteristics

- Input Voltage Range V_{IN} = 8.0V～31V
- Output Voltage V_O=5V Fixed
- Output Current I_O=1A
- Operationg Frequency Fsw=500kHz Fixed

Applications

- Refrigerator
- Air conditioner
- LCD-TV
- Blu-ray
- Power supply for digital consumer

Basic Circuit Connection



NR263S (Vo=5V Fixed)

CONTENTS

1. Electrical Characteristics

1.1 Absolute Maximum Ratings

- The polarity value for current specifies a sink as “+” and a source as “–”, referencing the IC.
- Ta=25°C,unless otherwise noted.

Parameter		Symbol	Ratings	Units	Conditions
DC input voltage		V_{IN}	–0.3 to 35	V	
BS terminal voltage		V_{BS}	–0.3 to 40.5	V	
BS to SW voltage		V_{BS-SW}	-0.3 to 5.5	V	DC
			8	V	* Pulse Width Limitation ≦10[ns]
SW terminal voltage		V_{SW}	–1 to 35	V	DC
			–2 to 35		* Pulse Width Limitation ≦100[ns]
			–6 to 35		* Pulse Width Limitation ≦10[ns]
VO terminal voltage		V_O	–0.3 to 6	V	
EN terminal voltage		V_{EN}	–0.3 to 35	V	
SS terminal voltage		V_{SS}	–0.3 to 7.0	V	
SS terminal sink current		I_{ssb}	5.0	mA	
Power dissipation	(1)	P_D	1.56	W	Glass-epoxy board mounting in a 40×40mm. * The implementation in our Demo- Board, Tj=150°C
Junction temperature	(2)	T_J	–40 to 150	°C	
Storage temperature		T_{stg}	–40 to 150	°C	
Thermal resistance (Junction to PGND Lead)		θ_{JP}	60	°C /W	
Thermal resistance (Junction toAmbient air)		θ_{JA}	80	°C /W	Glass-epoxy board mounting in a 40×40mm. * The implementation in our Demo- Board

(1) Limited by thermal shutdown

(2) The temperature detection of thermal shutdown is about 165°C

1.2 Recommended Operating Conditions

Operating IC in recommended operating conditions is required for normal operating of circuit functions shown in Table 3 Electrical characteristics of NR263S.

Parameter		Symbol	Ratings		Units	Conditions
			MIN	MAX		
DC input voltage range		V_{IN}	8	31	V	
DCoutput current range	(3) (4)	I_O	0	1	A	
Operating ambient temperature	(4)	Ta	–40	85	°C	
Operating junction temperature	(4)	Tj	–40	125	°C	

(3) Refer to “Fig3-1 Typical Application Circuit”

(4) To be used within the allowable package power dissipation characteristics (Fig 4)

1.3 Electrical Characteristics

- The polarity value for current specifies a sink as "+" and a source as "–", referencing the IC.
- Ta=25°C,unless otherwise noted.

Table.3 Electrical Characteristics

Parameter			Symbol	Ratings			Units	Conditions
				MIN	TYP	MAX		
Output voltage			V_O	4.85	5.00	5.15	V	V_{IN} = 12V, I_o = 0.5A
Output voltage temperature coefficient			⊿V_O/⊿T		±0.3		mV/°C	$_{IN}$ = 12V, I_o = 0.5A -40°C ～+85°C
Operating frequency			fsw	-30%	500	+30%	kHz	V_{IN}=12V, Vo=5.0V, I_O=1A
Line regulation		(5)	V_{Line}		50		mV	V_{IN}= 8V～17V, Vo=5.0V, I_O=0.5A
Load regulation		(5)	V_{Load}		50		mV	V_{IN}=12V, Vo=5.0V, I_O=0.1A～1.0A
Over current protection threshold			I_S	1.1	1.5	2.6	A	V_{IN}=12V, Vo=5.0V,
Supply Current			I_{IN}		250		uA	V_{IN}= 12V, V_{EN}=12V I_O=0mA
Shutdown Supply Current			$I_{IN(off)}$		1.2	10	uA	V_{IN}=12V, V_{EN}=0V
Input UVLO Threshold			Vuvlo	5	6	7	V	V_{IN} Rising
Uvlo hysteresis			Vuvlo_hys		0.55			UVLO ON～UVLO OFF
SS terminal source current			I_{SS}	2.5	5.0	8.5	µA	V_{SS}=0V, V_{IN}=12V
EN terminal	Sink current		I_{EN}		14	30	µA	V_{EN}= 12V
	Turn-ON thereshold		V_{EN}	0.8	1.1	2.1	V	V_{IN}=12V
	Hysteresis voltage		V_{EN_hys}		0.15		V	
Maximum ON Duty		(5)	D_{MAX}		85		%	V_{IN}=12V
Minimum ON Period		(5)	$T_{ON(MIN)}$		200		nsec	V_{IN}=12V
Thermal shutdown threshold temperature		(5)	TSD	151	165		°C	V_{IN}=12V
Thermal shutdown restart hysteresis of temperature		(5)	TSD_hys		15		°C	V_{IN}=12V
ON Resistance of Hi-side SW MOSFET		(5)	RonH		250		mΩ	V_{IN}=12V
ON Resistance of Lo-side SW MOSFET		(5)	RonL		200		mΩ	V_{IN}=12V

(5) Guaranteed by design,not tested

2. Block Diagram & Pin Functions

2.1 Block Diagram

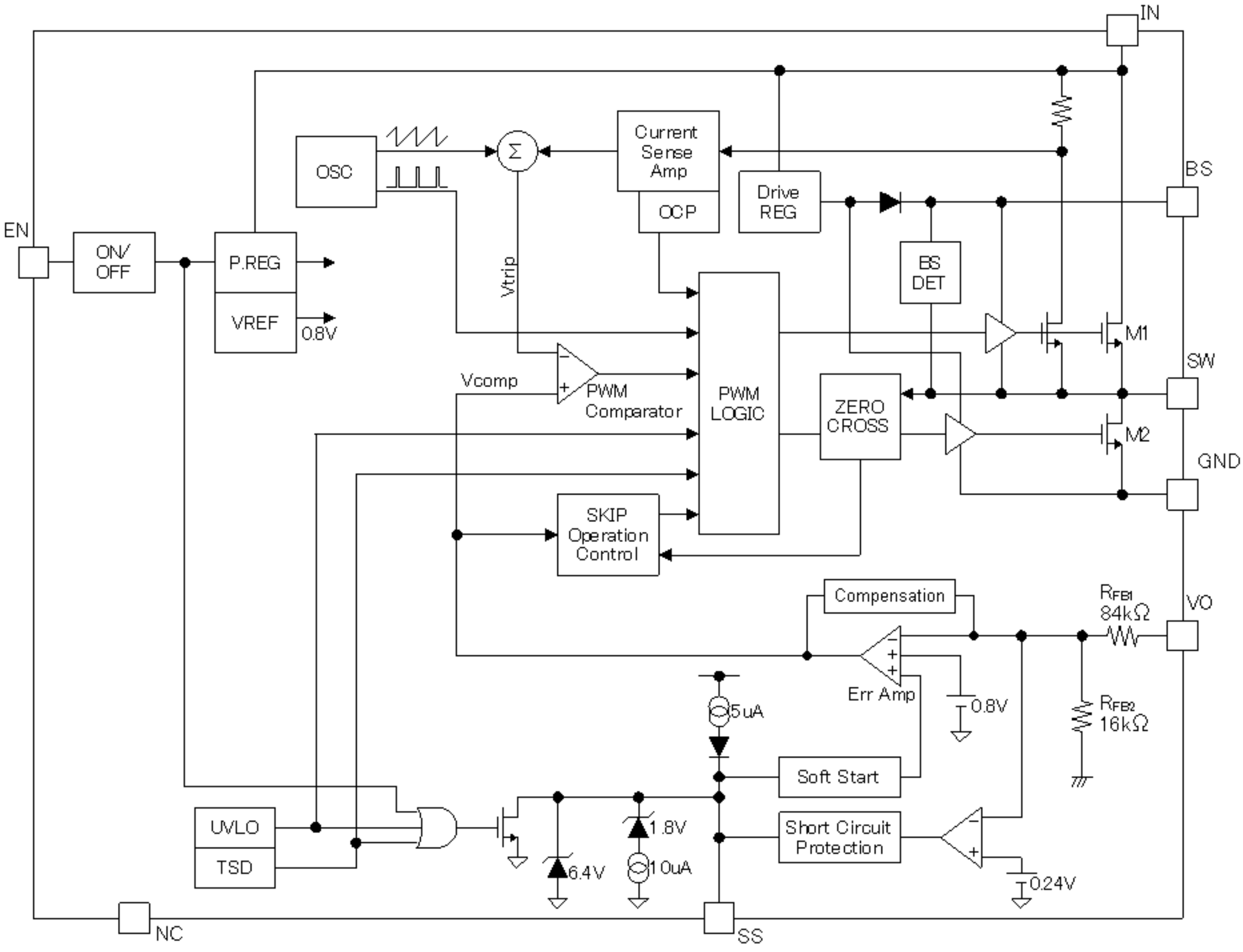


Fig. 2-1 NR263S Block Diagram

2.2 Pin Assignments & Functions

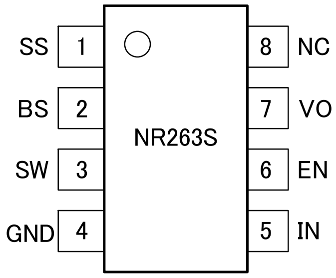


Fig. 2-2 Pin Assignments

Table.4 Terminal Functions

Pin No.	Symbol	Functions
1	SS	Soft-start control input To set the soft-start period, connect to a capacitor C_{SS} between SS and AGND terminal
2	BS	Boost Input A BS terminal supplies the drive power of the internal PowerMOSFET Connect a capacitor between the SW terminal and the BS terminal
3	SW	Power switching output SW supplies power to the output Connect the LC filter between SW and the output Note that a capacitor C_{BS} is required between SW and BS to supply the power the High-side driver
4	GND	Ground terminal By the synchronous rectification, the switching current flows
5	IN	Power Input Supply power to the IC
6	EN	Enable signal input Drive EN Pin high to turn ON the regulator, low to turn it OFF
7	VO	Feedback signal input terminal to compare Output voltage The feedback threshold (V_{REF}) is 5.0V Connect the V_O terminal directly to the output voltage V_O.
8	NC	No connection

3. Typical Application Circuit

Standard connection is shown in Fig3-1.

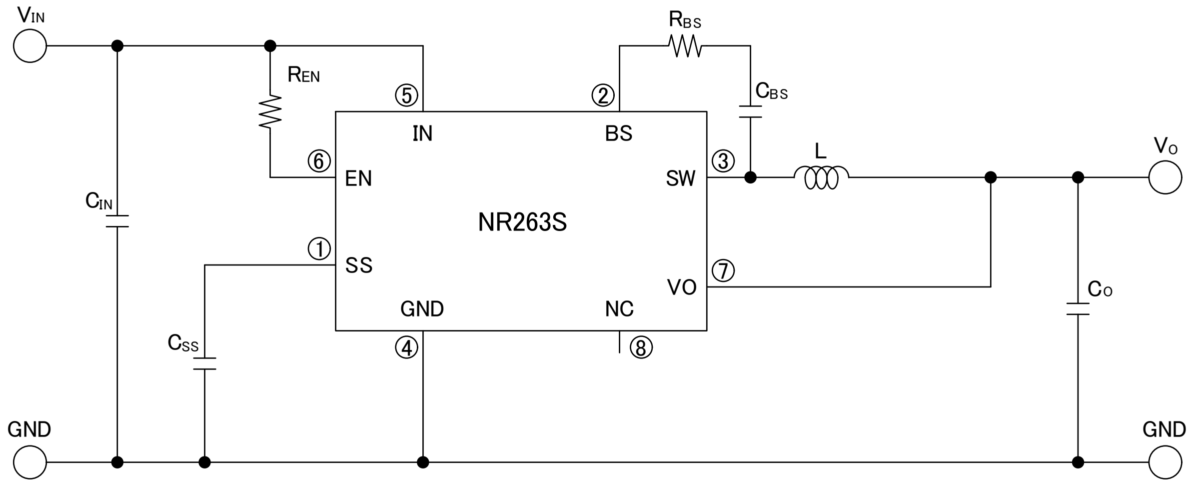


Fig. 3-1 NR263S Standard connection

C_{IN}: 10µF / 25V
R_{EN}:100kΩ
C_O: 22µF / 16V
R_{BS}:≦10Ω
C_{BS}: 0.1µF
C_{SS}: 0.1µF

L: 6.8µH

*As for the circuit diagram of the Demo-Board, please refer to the Demo-Board circuit diagram of the "8.2.2 mounting board pattern example" section.

4. Allowable package power dissipation

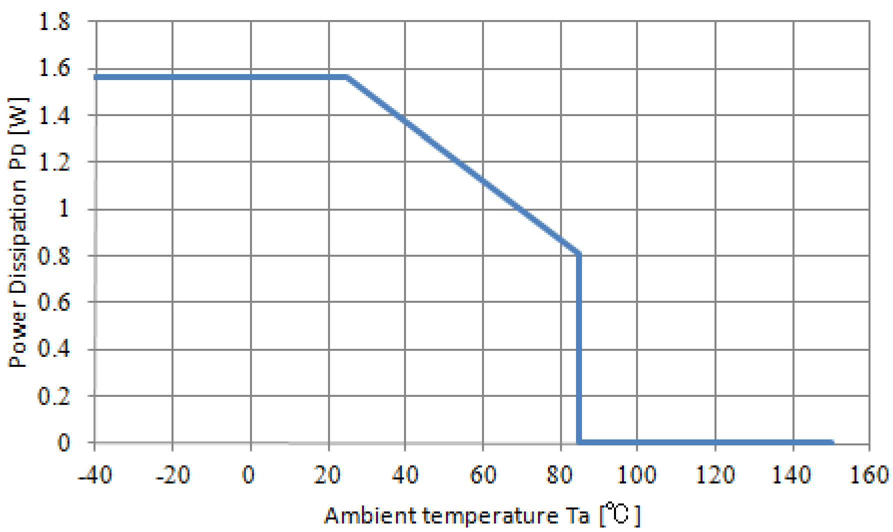


Fig. 4-1 Allowable package powe disspation of NR263S

Notes:

1) Because the Fig5 is defined in "PD=1.56[W]" at "Tj=150 [°C]", please keep enough margin when you use. (Our Demo-board implementation in the Fig21)
2) Losses can be calculated by the following equation. In addition, efficiency ηx will vary depending on the conditions of the input voltage, output current. By measuring the ηx in the actual operation, assigns a numerical value to the equation (1) , as a ηx remain of percent display.

$$P_D = V_O \times I_O \left(\frac{100}{\eta x} - 1\right) - \left\{I_O{}^2 \times L(DCR)\right\} \qquad (1)$$

Main sources of heat generation are an inductor which is flowing the load current , and the IC which has the PowerMOSFET and the control circuit.
By subtracting the steady loss of the inductor from the overall efficiency, the loss of the IC is calculated by equation (1).

If following situations are ...V_O = 5[V], I_O = 1[A] continuous, the inductor DCR = 80[mΩ],
the Loss of IC when the overall efficiencyis 90 percent,
it will be 0.476[W] from the equation (1).

V_O: Output voltage

V_{IN}: Input voltage

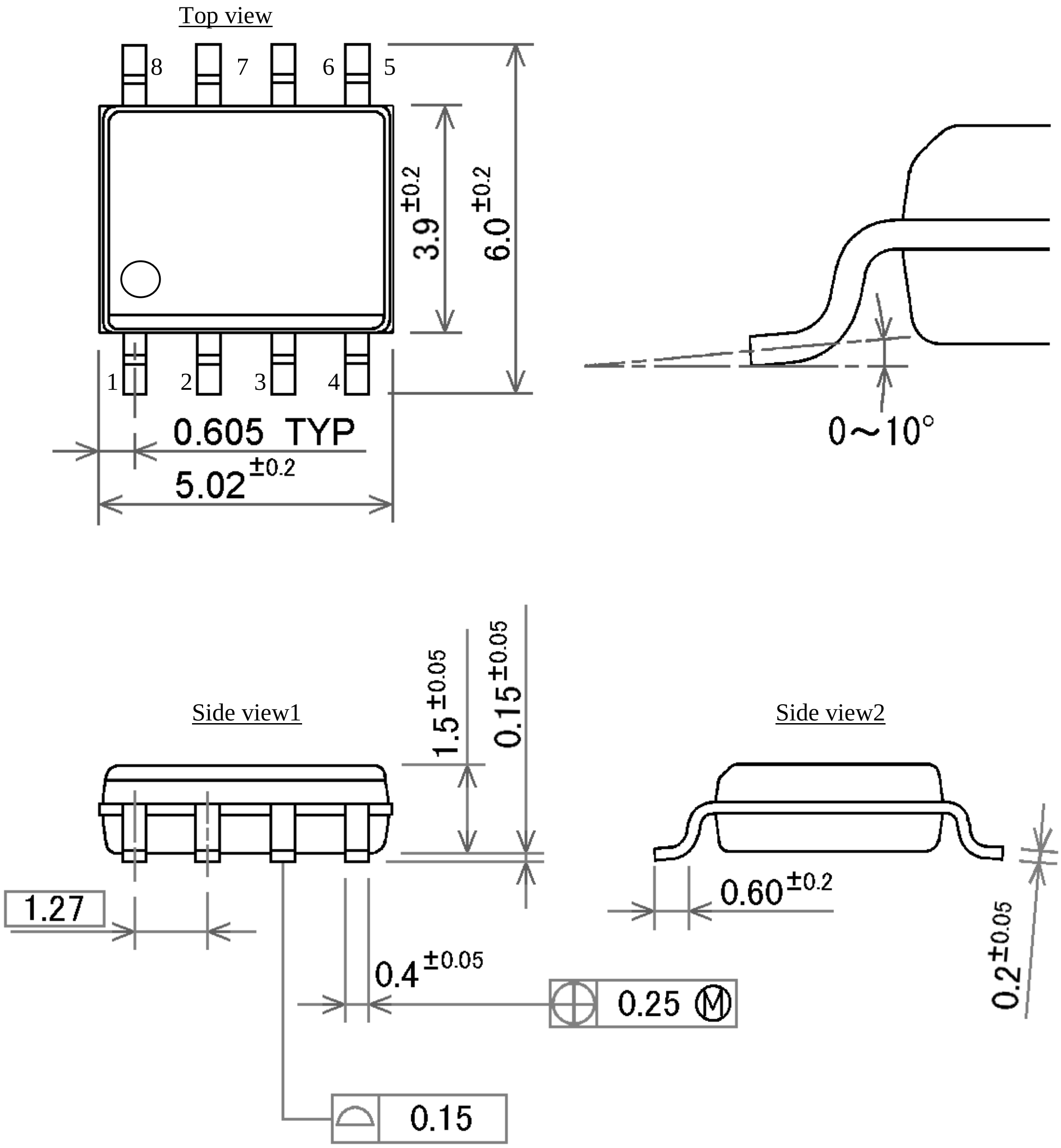
I_O: Output current

ηx: Efficiency(%)

L(DCR) : DC serial resistance of inductor (Ω)

5. Package Outline

5.1 Outline, Size



Notes:
1) Dimension is in millimeters (mm)
2) Drawing is not to scale.

Fig. 5-1 SOP8 Package outline

6. Marking

As for the Marking, the product name and lot number, those are laser marking to mold package surface.

*1. Product name
*2. Lot number (3 digits)
The 1st letter : Last one digit of the year (Y)
The 2nd letter : manufacturing Month (M)
Jan - Sep : 1 – 9
Oct : O
Nov : N
Dec : D
The 3rd letter : manufacturing Week (W)
First week - Fifth week : 1 - 5

*3. Our control number (4 digits)

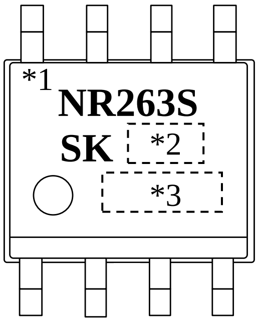


Fig. 6-1 Marking Specification

7. Operational Descriptions

The Characteristic value of, unless otherwise noted, it writes the TYP value in accordance with the NR263S specifications.

7.1 PWM(Pulse Width Modulation) Output Control

The PWM control circuit of the NR263S consists of the current sense amplifier, the error amplifier, the PWM comparator, the slope superimposing circuit. The Vtrip is the drain current feedback signal detected by current sense amplifier. And the V_{COMP} is the error amplification signal generated by the error amplifier with the output voltage and the reference voltage. By comparing with the Vtrip and the V_{COMP} in the PWM comparator, it performs control of the ON-Duty. In the slope superimposition circuit, by superimposing the slope signal with respect to the current feedback signal Vtrip, it can avoid the sub-harmonic oscillation that occur at ON-Duty 50% or more.

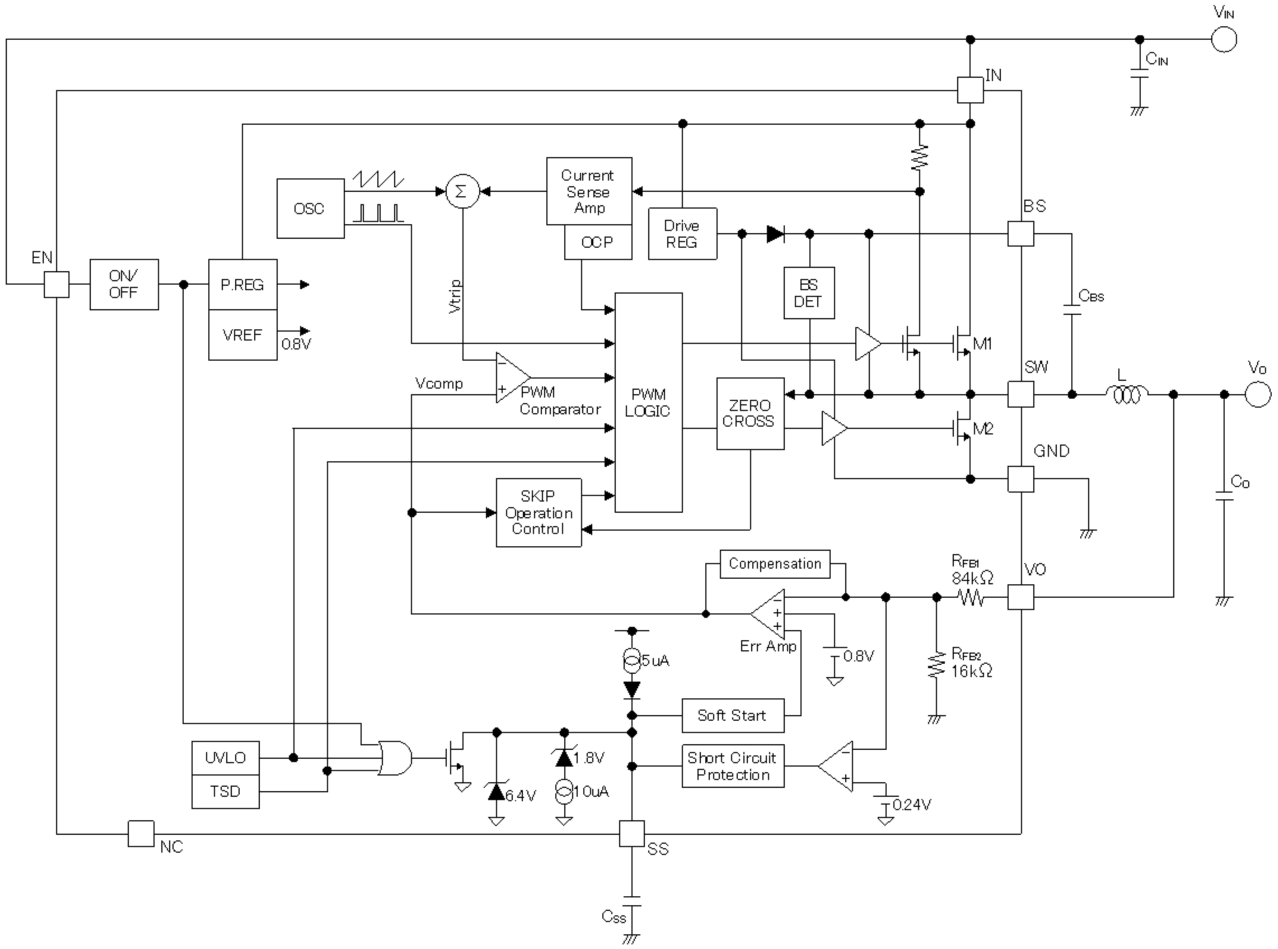


Fig. 7-1 Basic Structure of Buck Regulator with PWM Control by Current mode Control

When the UVLO was released or, the EN terminal voltage exceeded threshold, the SS terminal voltage starts to rise. In the period until the SS terminal voltage reaches to 0.6V (typ), to drive the High-side driver and the High-side switch (the following M1), by turning on the Low-side switch (the following M2), the boost capacitor C_{BS} is charged. After that, the switching operation is started when the SS terminal voltage exceeds 0.6V (typ). M1 and M2 are the switching-MOSFET for suppling the power to the Output. By M1&M2 repeating ON and OFF alternately, and energy is supplied to the Output stage. In the period when M1 turns on, the current of Inductor L increase, and the output of the current sense amplifier is raised, too. In the PWM comparator, the error amplifier output V_{COMP} signal is compared with the Vtrip signal which is the addition of the current sense amplifier signal and the slope compensation signal. When the Vtrip exceeds the V_{COMP}, M1 turns OFF, and M2 turns ON, the regenerative current of the inductor L flows via M2 from the GND. Then, upon receiving a set signal from the oscillator OSC, M1 is turned ON again.

7.2 UVLO and Enable Function

In the condition that the EN terminal is connected to the IN terminal, when the input voltage V_{IN} is increased beyond 6V(typ.), the UVLO is released and started the switching operation. And, in the condition that the input voltage V_{IN} is applied beyond 6V(typ.), when the EN terminal voltage exceeds 1.1V (typ.), it is started the switching operation.

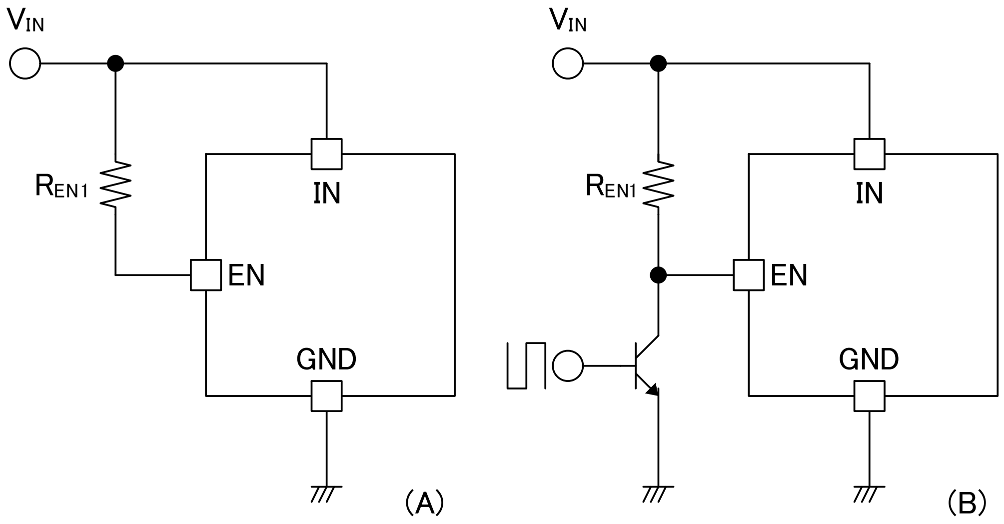


Fig. 7-2 Remote ON/OFF by EN terminal

The Fig7-2 (B) is the option of the "Remote ON/OFF control" by using the EN terminal. By using switch such as Open-collector and, by removing the EN terminal voltage V_{EN} to GND level (Low), it is possible to turn OFF. In case of without ON / OFF operation by external signal, please use the Fig7-2 (A) connection. It is started by the applying of the V_{IN}, and it is stopped by shut-off of the V_{IN}. R_{EN1} is recommended 100[kΩ].

7.3 Soft-start Function

By connecting a capacitor between the SS terminal and the GND terminal, when the input voltage is supplied to the IC, the soft-start function will be effective.The output voltage (Vo) is ramped up by the charging voltage level of Css. Because the internal constant current source I_{SS} supplied from the SS terminal is 5 μA, the soft-start period depends on the charging time constant of the C_{SS}. When the charging of C_{SS} is started by the constant current I_{SS}, the SS terminal voltage V_{SS} is linearly increased. The soft-start period is the time that the V_{SS} passes between the "Soft-start start threshold voltage V_{SS1}(=0.6V)" and "Soft-start completion threshold voltage V_{SS2}(=1.4V)". During the Soft-start, the rise-time is controlled by controlling the OFF period of PWM control. The rise time $t_{\_SS}$ and the delay time $t_{\_delay}$ are calculated in the following equations…

$$t_{ss} = C_{SS} \times (V_{SS2} - V_{SS1})/I_{SS} \qquad (2)$$

Note: V_{SS1}(=0.6V) $\leqq V_{SS} \leqq$ V_{SS2} (=1.4V), I_{SS}=5μA

$$t_{\_delay} = C_{SS} \times V_{SS1}/I_{SS} \qquad (3)$$

Note: 0V $\leqq V_{SS} < V_{SS1}$ (0.5V), I_{SS}=5μA

The rise time of the output voltage Vo is " $t_{\_delay}$ + t_{SS} ".

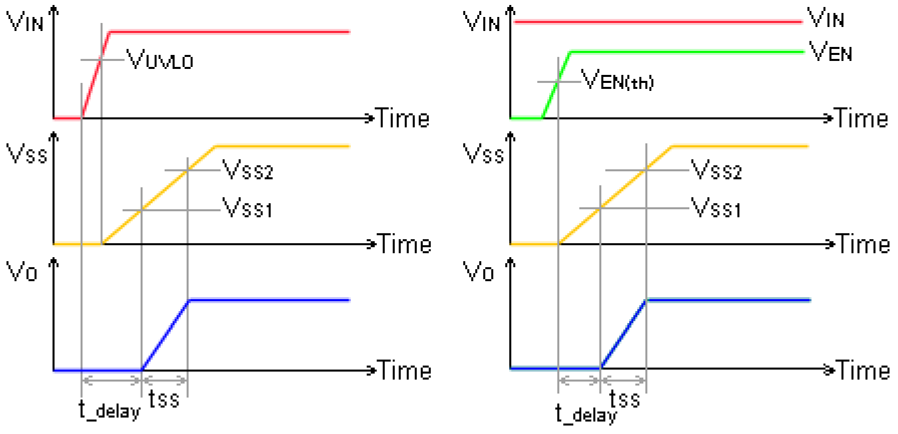


Fig. 7-3 The timing chart of the Soft-start in the normal startup

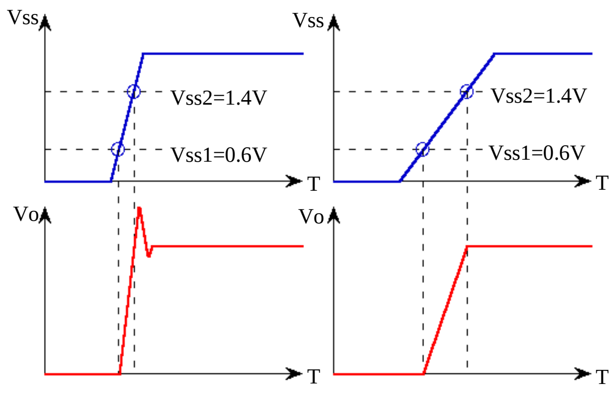


Fig. 7-4 The occurrence of the overshoot on Vo rising waveform

Adjust the capacitance of C_{SS} so that the excessive overshoot may not occur on the Rising-Waveform of the output voltage Vo at the start-up. The overshoot occurs when tss is short.If the soft-start is finished before the constant voltage control follows Vo rising speed,it may become such waveform of Fig7-4. When a capacitance of the C_{SS} is increased, though the overshoot will not occur , please understand that the start-up time is longer. In actual operation, please confirm the Rising-waveform, and adjust the capacitance of the C_{SS}.

Note: About C_{SS} discharge to restart
It is explained about discharging of the C_{SS} capacitor when this IC is restarted such as ON/OFF operation in the EN terminal. When it was restarted, there is a case where the voltage is remaining in the soft-start capacitor C_{SS}. In this IC, it has adopted the forced discharge sequence as shown in the Fig7-5. By the internal impedance, after once discharging the SS terminal voltage to 0.6V or less, and then resume the soft-start.
Discharge of the capacitor Css, it is discharged by the internal impedance 600 Ω (typ) in the IC.

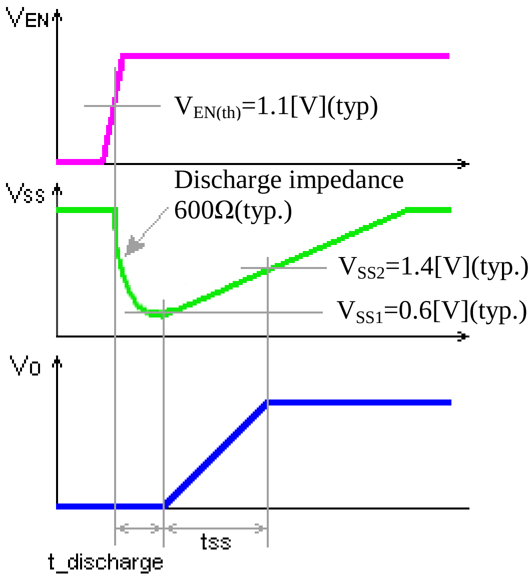


Fig. 7-5 Discharge of the capacitor Css at restart

Under the condition that the voltage is remaining in the Css, after the ON-signal is inputted, it takes the time of "t_discharge+tss" until Vo-waveform rise and stabilize. The soft-start capacitor Css has been charged to the internal regulator voltage 1.8V.
It considers the discharge from the condition that the soft-start capacitor C_{SS} has been charged up to 1.8V in the steady condition. The SS terminal voltage V_{SS} at optional time t after the start of discharge will be calculated by the equation (4). For the time t_discharge that the V_{SS} is discharged to 0.6 V from 1.8 V, it can be calculated by equation (5).

$$V_{SS}[V] = 1.8[V] \times EXP(-t[s]/C_{SS}[F] \times 600[\Omega]) \qquad (4)$$

$$t_{\_discharge}[s] = -C_{SS}[F] \times 600[\Omega] \times \ln(0.6[V]/1.8[V]) \qquad (5)$$

When there is a mode for continuous "ON/OFF" operation, consider delay by discharging of the C_{SS}.

7.4 Over current and Short circuit protection Function (OCP & HICCUP)

An OCP characteristic is shown in the Fig7-6. The "drooping type" over-current-protection is equipped in the NR263S. As for the over-current-protection circuit,this IC detects a peak current to flow to the switching-transistor. When peak current exceeds setup value, a Ton-period of the transistor is made to shorten forcibly, and an output voltage V_O is made to decrease, and an output current is restricted. In this case, by the decline of the output voltage V_O, when a VO-terminal- voltage V_O decreases to 3.5V 70% of the internal-reference -voltage (5V) , by the reducing of the switching-frequency (the F_{DOWN} mode),the "drooping characteristic" is improved in the low output voltage.As shown in the Fig12, Moreover, when a VO-terminal-voltage V_O decreases more and it becomes under 30% of the internal reference voltage (*5V→1.5V), the Soft-start capacitor C_{SS} is charged by internal current source I_{SS}=5μA.When a SS-terminal-voltage V_{SS} rises to 2.2V, the interval-operation mode (HICCUP) becomes effective, and the continuous-switching-operation is canceled. After that, the soft-start capacitor C_{SS} is discharged by the constant current (=-2.5[μA]) , and the suspension-period of interval-operation is set up. The soft-start is restarted when a SS-terminal-voltage V_{SS} decreases to 0.23[V]. The interval-operation mode (HICCUP) is maintained due to this repetition. By becoming the interval-operation mode, part stress such as heat-generation can be eased. An output voltage is resumed to normal condition automatically when over-current condition is canceled. * When a HICCUP function is invalidated, the short-current becomes continuously such as a characteristic of the red line in the Fig7-7.

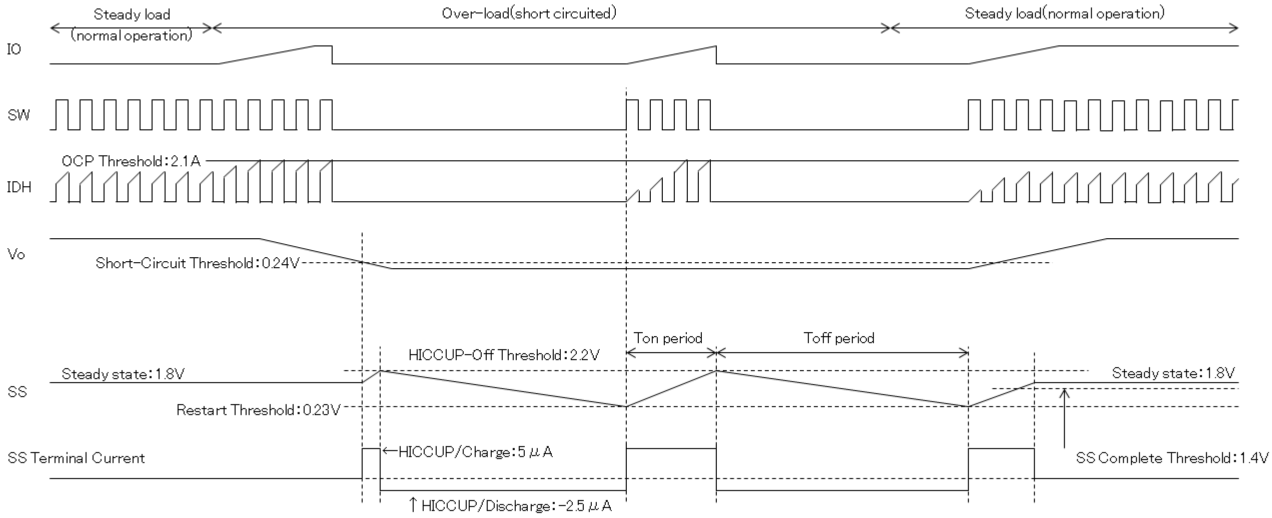


Fig. 7-6 OCP (HICCUP Mode) Timing Chart

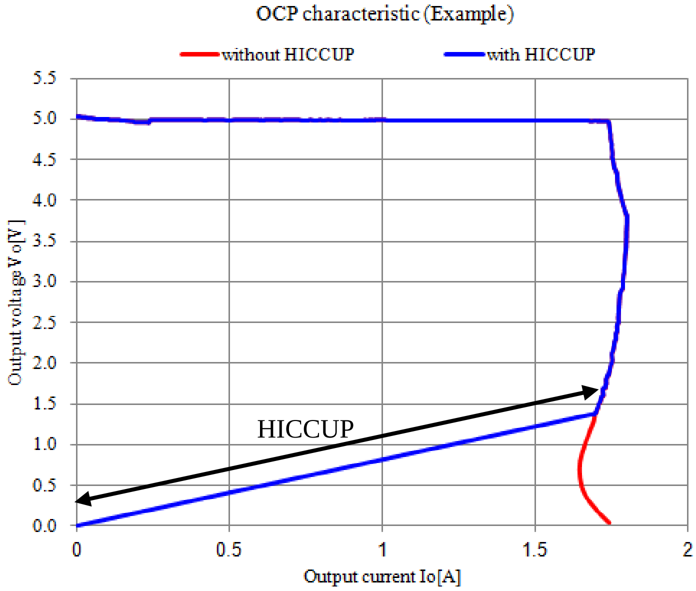


Fig. 7-7 OCP characteristic curve (Condition example :V_{IN}=12V, V_O=5V)

7.5 Thermal Shutdown (TSD)

The thermal shutdown circuit detects the IC junction temperature. When the junction temperature exceeds the rated value (around 165°C), it shuts-down the output transistor and turns the output OFF. If the junction temperature falls below the thermal shutdown rated value by around 15°C, the operation returns automatically.
* (Thermal Shutdown Characteristics)
Notes
The circuit protects the IC against temporary heat generation. It does not guarantee the operation including reliabilities under the continuous heat generation conditions, such as short circuit for a long time.

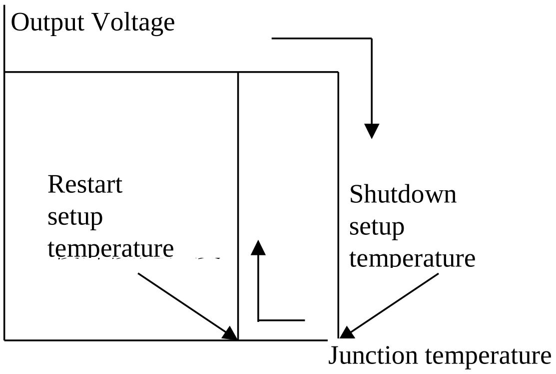
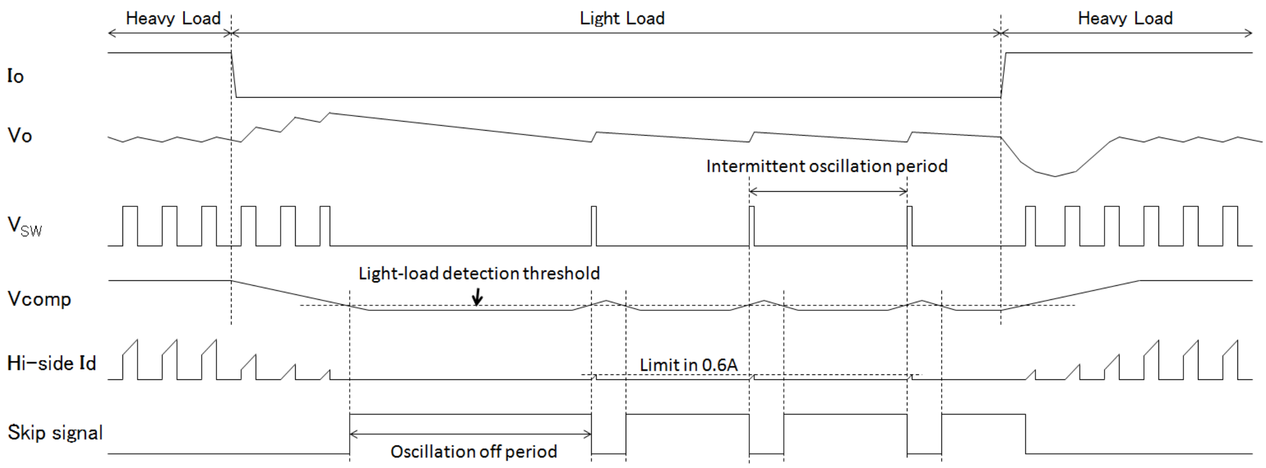


Fig. 7-8 TSD Operation

7.6 About the "Pulse-Skip-Mode" in the Light-load condition

A NR263S is equipped with the "Pulse-Skip-Mode (naming of our company) " to realize high efficiency in Light-load. The more load current decrease,it is controlled so that a COMP voltage V_{COMP} may decrease.
In the condition that the load-current decreases and the V_{COMP} is under the Vskip (Vskip=Light-load detection threshold), the operation changes to the Pulse-Skip-Mode when the discontinuous-condition of inductor-current is longer than the internal timer setup. In the Pulse-Skip-Mode, the peak value of the "Hi-side MOSFET Drain-current (=IL_P)" is limited to about 600mA. And, the variable-frequency-operation is done that changes the switching-frequency corresponding to the load. The more switching-frequency decreases, the efficiency in the light-load condition is possible to improve because the switching-loss decreases in the Hi-side MOSFET and the Lo-side MOSFET. And, when the load condition changes from light-load to heavy-load,the operation changes from the Pulse-Skip-Mode to the normal PWM switching mode in a moment.



Notes:
*The V_{COMP}, the Skip signal, and, the light-load detection threshold Vsk will not be able to confirm directly from the outside of the package.
*The pulse-skip mode can't be intentional cancellation by the external signal.

Fig. 7-9 Timing chart of the Pulse-Skip-Mode

In addition, pulse-skipping mode frequency as described above will be decreased. There is also a case to be audible frequency band (20kHz or less). Pulse skip frequency F_{skip} can be roughly calculated by the following equation.

$$F_{skip} \approx \frac{2 \times I_O[A] \times 5[V] \times (V_{IN}[V] - 5[V])}{(I_{LP}[A])^2 \times L[H] \times V_{IN}[V]} \qquad (6)$$

In actual operation confirmation of the standby-light load, if the audible-noise by the operation of an audible-frequency-range occurs, please adjust the inductance(L) of the inductor in reference to the equation (6). However, if the Fskip becomes higher, power consumption will increase. Please be careful. In pulse skipping operation, the IL_P of equation (6) is limited to a constant value determined by the input voltage V_{IN} and use inductor inductance L. But, it has the input voltage dependence such as Fig7-10. If you wish to calculate the Fskip, please pick up the value of the IL_P from Fig7-10 and substitute the IL_P to equation (6).

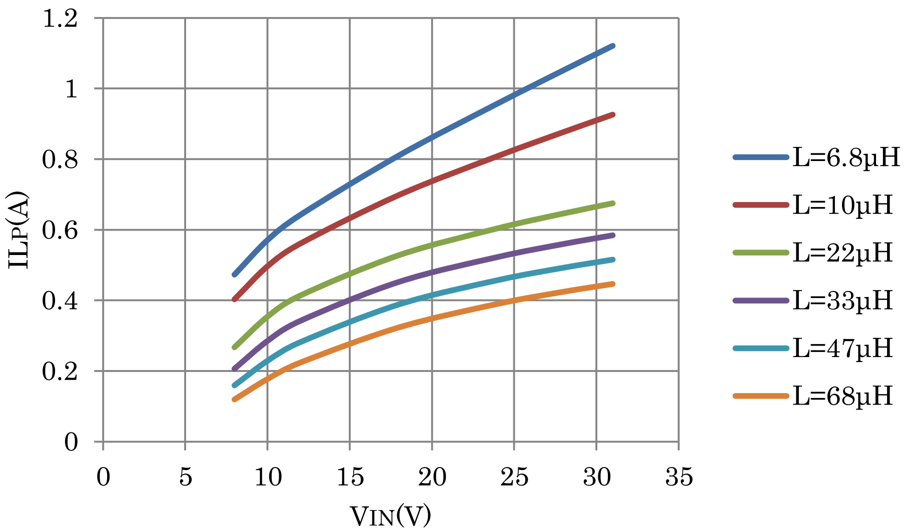


Fig. 7-10 V_{IN} vs. IL characteristics (with inductance L variation)

8. Design Notes

8.1 External Components

All components are required for matching to the condition of use.

8.1.1 Inductor L1

The Inductor is one of the most important components in the Buck regulators. In order to maintain the stabilized regulator operation, the Inductor should be carefully selected so it must not saturate or overheat excessively at any conditions. Please select an inductor with care to six items listed below.

- It is for switching regulator use only

Because the coil for the noise filter (For EMI Countermeasure) has large loss and large heat generation, please do not use.

- Avoidance of sub-harmonic oscillation

Under the peak detection current control, when the control Duty is more than 0.5 in use conditions, the inductor current may fluctuate at a frequency that is an integer multiple of switching operation frequency. This phenomenon is the known as sub-harmonic oscillation and this phenomenon theoretically occurs in the peak detection current control mode. In order to stabilize the operation, although the inductor current compensation is made internally, the inductance corresponding to the output voltage should be selected as an application. Specifically, for slope compensation amount is fixed in the IC, it is necessary to moderate the slope of the inductor current. The ripple portion of Inductor current ΔI_L and the peak current IL_P are calculated from the following equations:

$$\Delta I_L = \frac{(V_{IN} - V_O) \times V_O}{L \times V_{IN} \times f} \quad (6)$$

$$IL_P = \frac{\Delta I_L}{2} + I_O \quad (7)$$

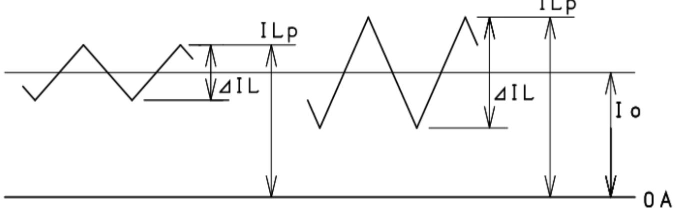


Fig. 8-1 Relationship between the inductance and ripple current ΔI_L

According to the equations, if the inductance of the inductor L is small, both ΔIL and ILp is increased. Consequently, the inductor current becomes very steep if inductance is too small, so that the operation of the converter might become unstable. It is necessary to take care of an inductance decrease due to magnetic saturation such as in overload and load shortage.

(Inductance L calculation in case of "D≧0.5")

The duty control is represented by the ratio of the output voltage V_O and the input voltage V_{IN}. The control duty will be 0.5 or more in case that the input voltage V_{IN} is 10V or less. If the inductor current is used as the continuous current mode (CCM) in this input / output condition, the ΔI_L in equation (9) is recommended the setting of less than 0.2A in order to avoid the sub-harmonic oscillation (Slope relaxation of the inductor current).

$$L[H] \geqq \frac{(V_{IN}[V] - V_O[V]) \times V_O]}{\Delta I_L[A] \times V_{IN}[V] \times F_{SW}[Hz]} \quad (9)$$

(Inductance L calculation in case of "D＜0.5")

In the case of "D<0.5", the settable range of the ΔI_L becomes "0.2≦ΔI_L≦1A".

6.8μH that is a reference constant in the Typical Application Circuit is roughly the upper limit of the settable range of the ΔI_L. It is a setting that is able to give the smallest inductance L. If the ΔI_L becomes smaller, the necessary inductance L will be larger. Please calculate the inductance L using the equation (9) in the range of "ΔI_L=0.2A-1A".

- ΔI_L / Io ratio

  When the ΔI_L/Io ratio is increased, the Inductance decreases.However, there is a matter of trade-off, for example, the output ripple voltage increases.When the ΔI_L/Io ratio is decreased, required inductance increases, and the outer shape of the Inductor becomes larger. Setting of the ΔI_L/Io ratio to 0.2 or 0.3 is conventionally regarded as a setting for good cost performance.

- Diameter of the wire winding

  When the Inductance is increased, if the core-size of the Inductor is identical, the number of turns of windings will increase, and the diameter of wire windings will be thinner. Because the DC resistance DCR also increases, the large current can't to flow. If the DCR is in priority, the core size of the Inductor enlarges.

- DC superposition characteristics
  Depending on the material or shape of the core, the inductance of inductor has DC superposition characteristics that decreases gradually by the flowing DC current. Be sure to confirm if the inductance value is significantly lower than the design value when making the maximum load current for practical use flow. Obtain the data of the DC superposition characteristics including graphs from the manufacturer of the coil to understand the characteristics of the Inductor used in advance. In doing so, important parameters are:

  1) Saturation point...At what ampere does magnetic saturation occur?
  2) Inductance fluctuation with the practical load current
  For example, for using it up to 1 A in the actual load Io, it can not use the Inductor which the saturation point is such as 0.5 A. In addition, in spite of having an inductance of 10 μH at the no-load, please pay caution for the thing which has the characteristic that it decreases to such as 5μH by the superposition current of 1A.

- Less noise

  If the core is the open magnetic circuit type shaped like a drum, the magnetic flux passes outside the Inductor, so that the peripheral circuit might be damaged due to noise. Use the Inductor which has a core/structure of the low-leakage magnetic flux type. For details, consult the manufacturer of the Inductor.

- Heat generation

  In actuality, when using the coil for mounting the PCB, heat generation of the coil main body might be influenced by peripheral parts. In most cases, temperature rise of the coil includes the Inductor's own heat generation, and there are temperature limitations such as below:
  1) onboard(Cars) grade product: 150°C
  2) highly-reliable product: 125°C
  3) general product: 85-100°C

  Be sure to evaluate heat generation because temperature rise differs when the PCB on which the Inductor is mounted is designed differently.In general, Inductors with a smaller DCR value on the specification sheet have smaller loss.
  * Select the most appropriate one in consideration of the conditions of use, mounting, heat dissipation, etc.

8.1.2 Input Capacitor C_{IN}

Please use the ceramic capacitor to the input capacitor. It will lower the input impedance and it will contribute to the stable operation of the IC. The input capacitor C_{IN} must be arranged in as much as possible the shortest distance to between IN - GND of the IC. Even if there is a smoothing capacitor C_F in the transformer secondary side rectifying and smoothing circuit, please place the C_{IN} in the immediate vicinity of the IC. As a point of C_{IN} selection, it will include the following:

- Satisfaction of the withstand voltage and, that capacitance change with respect to the applied voltage is low
- The rate of capacity change in the ambient temperature range to be used is small
- Parts temperature which contains the heat-generation is must satisfy the specifications of the maximum operating temperature
- Its impedance Z is sufficiently low in the temperature conditions and using frequency

* Please query the product information of the capacitor manufacturer.
* Even in the ceramic capacitor, in case of the insertion parts having a lead, its impedance will be higher than surface-mounted type, therefore please be careful.
* In generally, in case of ceramic capacitors, the allowable ripple current is not included in the specification. But,because it has the equivalent series resistance ESR inside, the ceramic capacitor occurs slightly heat-generation by flowing ripple current. Therefore there is a need to comply with the maximum operating temperature containing the heat generation. In this case, also please consider the heat conduction from the heat generating parts of the surrounding.
Select the most suitable parts which has a margin in consideration of the use condition, the mounting condition, the radiation condition, and so on.

8.1.3 Output Capacitor C_O

In the current control mode, the feedback loop which detects the inductor current is added to the voltage control mode. The stable operation is achieved by adding inductor current to the feedback loop without considering the effect of secondary delay factor of LC filter. It is possible to reduce the capacitance of LC filter that is needed to make compensations for the secondary delay, and the stable operation is achieved even by using the low ESR capacitor (ceramic capacitor).
The output capacitor C_O comprises the LC low-pass filter with the Inductor L1 and works as the rectifying capacitor of switching output. The current equal to ripple portion ΔI_L of the Inductor current charges and discharges the output capacitor. The equivalent serial resistance ESR exists in the ceramics capacitor, and the voltage multiplied by ESR and ΔI_L becomes the output ripple voltage and it appears as $V_{Oripple}$.

$$V_{Oripple} = ESR(C_O)[\Omega] \times \Delta I_L[A] \qquad (10)$$

To suppress output ripple voltage $V_{O\ ripple}$ to any value, the required ESR conditions in the ceramic capacitor can be calculated by the following equation (10).

$$ESR(C_O)[\Omega] < V_{Oripple}[V]/\Delta I_L[A] \qquad (11)$$

Therefore, if the ripple portion of the inductor current ΔI_L is small, the output ripple voltage $V_{O\ ripple}$ will be relatively small. If the ΔI_L is large, as parallel connection of the ceramic capacitor, it may be necessary to reduce the ESR. As a point of C_O selection, it will include the following:
In the same way as the input capacitor C_{IN}, as the point of C_O selection, it will include the following:

- Satisfaction of the withstand voltage and, that capacitance change with respect to the applied voltage is low
- The rate of capacity change in the ambient temperature range to be used is small
- Parts temperature which contains the heat-generation is must satisfy the specifications of the maximum operating temperature
- Its impedance Z is sufficiently low in the temperature conditions and using frequency

*Please query the product information of the capacitor manufacturer
*Even in the ceramic capacitor, in case of the insertion parts having a lead, its impedance will be higher than surface-mounted type, therefore please be careful.
*In generally, in case of ceramic capacitors, the allowable ripple current is not included in the specification. But,because it has the equivalent series resistance ESR inside, the ceramic capacitor occurs slightly heat-generation by flowing ripple current. Therefore there is a need to comply with the maximum operating temperature containing the heat generation. In this case, also please consider the heat conduction from the heat generating parts of the surrounding.

Select the most suitable parts which has a margin in consideration of the use condition, the mounting condition, the radiation condition, and so on.

8.2 Pattern Design

High current paths in the circuit are marked as bold lines in the circuit diagram below. These paths are required for wide and short trace as possible. In addition, the pattern trace which is the signal system GND, and the pattern trace which the main circuit current flows, please to so that it does not become common impedance.

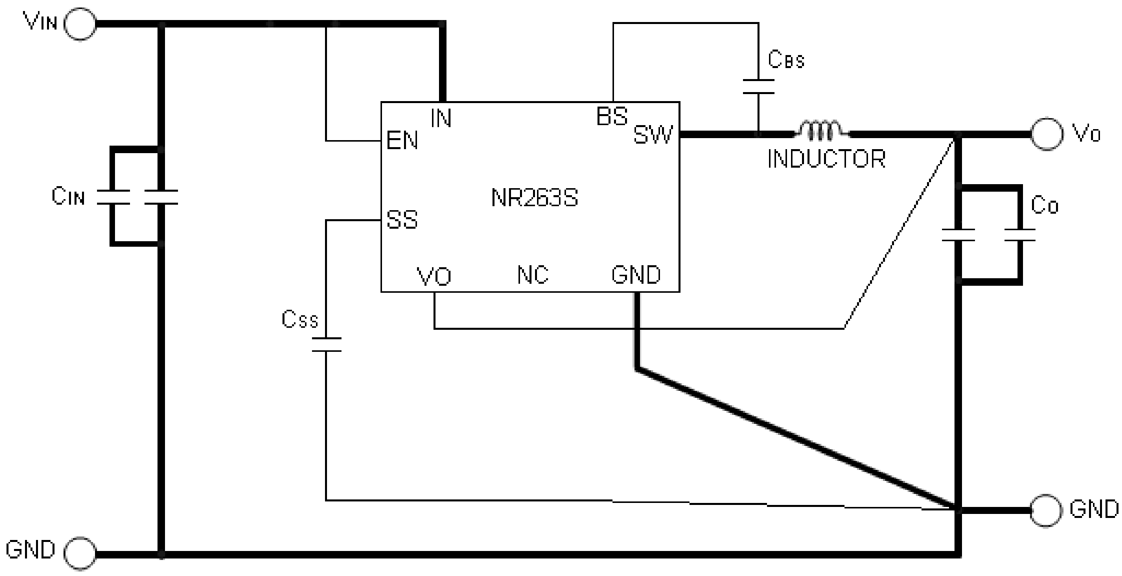
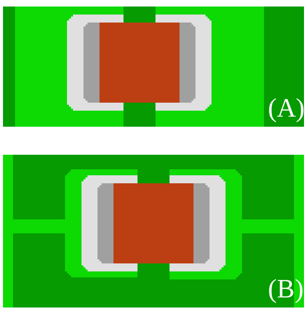


Fig. 8-2 Note points in the wiring pattern

8.2.1 Input / Output Capacitors(C_{IN},C_O)

The input capacitor C_{IN} and the output capacitor C_O are required to connect to the IC as short as possible.
Think about the image to connect it between the pins of the IC ideally and directly.
In such cases as the secondary side of the switching power supply, when there is a filter capacitor on the input side in advance, though it is possible that it is included with a input capacitor for NR263S, in case of long distance between filter capacitor and NR263S , it is necessary to connect as “line-bypass-capacitor”,aside from the one for the filter.
The ripple current flows to the capacitor of input and output, you must make Low impedance and ESR.
When you design a circuit board, set to shorter length the pattern of input and output capacitor.
In the same way,consideration is necessary for route of the capacitor pattern.



(A)･･･Recommended Pattern
(B)･･･No good pattern example

Fig. 8-3 C_{IN},C_O pattern example

8.2.2 PCB Layout & Recommended Land Pattern

The pattern example of the printed circuit board for our Demo Board is shown in the Fig8-6. (Double sided PCB)

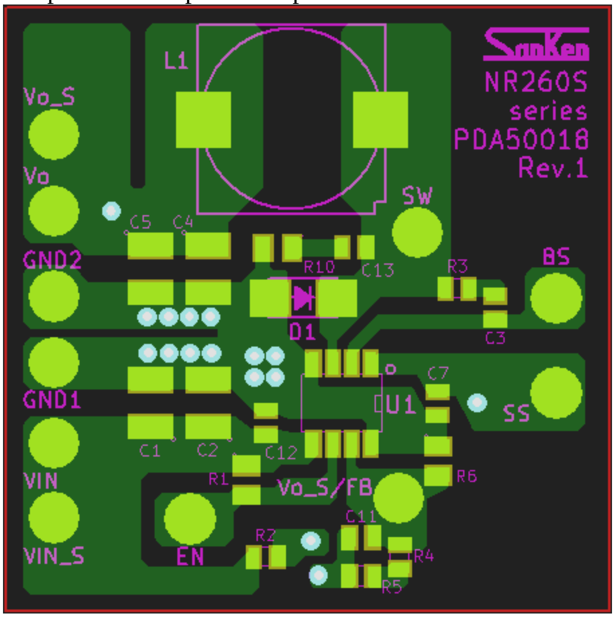


Fig. 8-4 Component mounting side (surface)

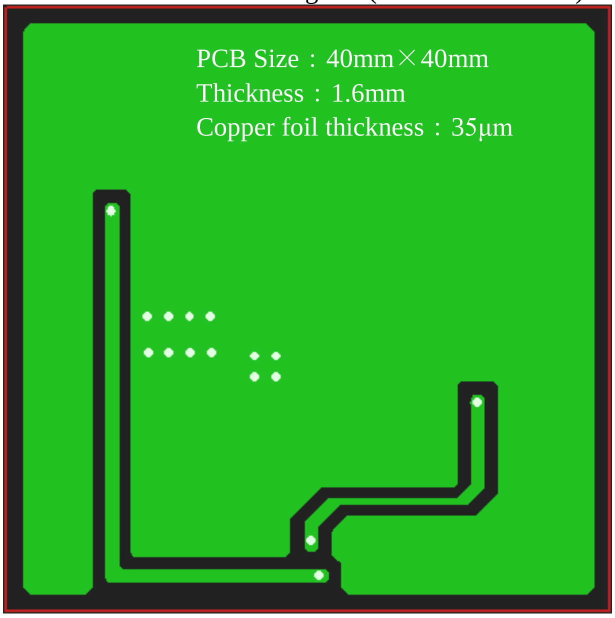


Fig. 8-5Back side (see from surface)

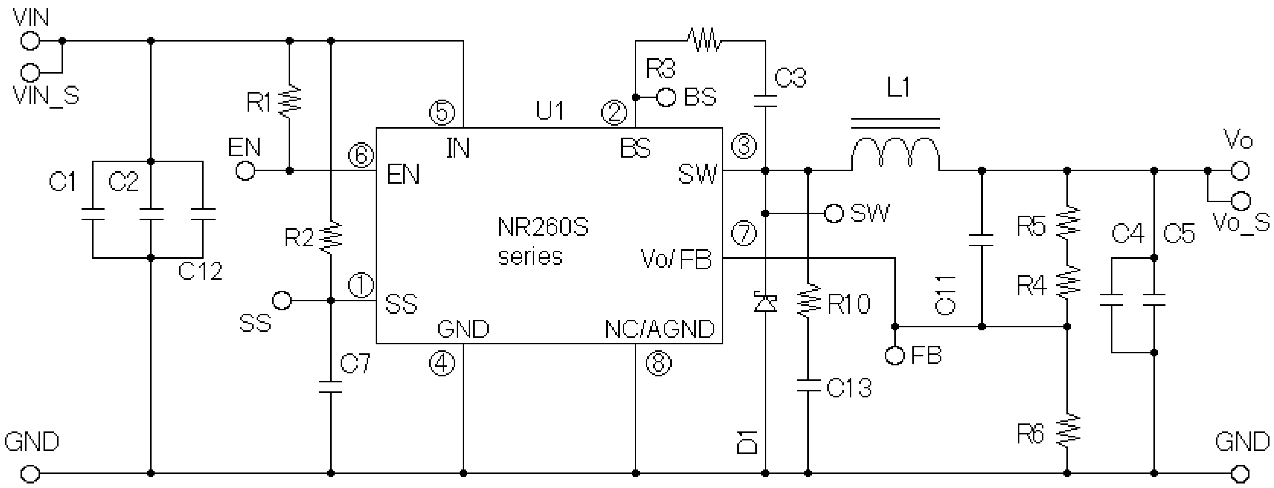


Fig. 8-6 Our demo board circuit diagram for NR260S series

(In reference for NR263S)

C1,C2:10μF/25V C3:0.1μF C4,C5:22μF/16V C7:0.047μF R3:≦10Ω

R1:100kΩ R4 & R5:Short R6:Open L1:6.8μH

*Part number will match the silk-prints of the demo board.

*Optional Parts

C11：Phase advance capacitor･･･For experiment

C12：Bypass capacitor (IN to AGND&PGND)･･･For experiment

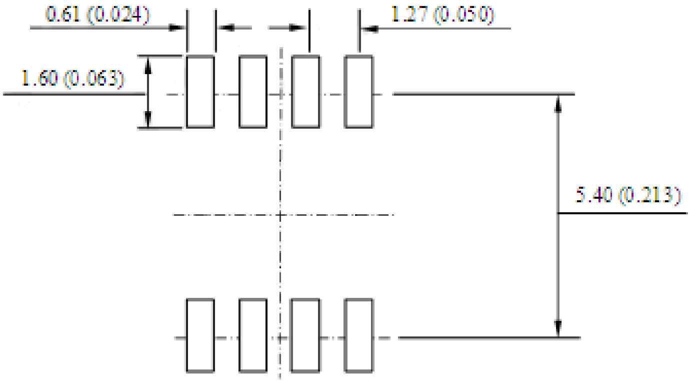
C13：Snubber circuit capacitor･･･For experiment, R10：Snubber circuit resistor･･･For experiment

R2：Open (R2 is not used in the NR260S series)

R3：Resistor for spike noise reduction･･･For experiment

D1：The Schottky barrier diode for Efficiency improvement･･･For experiment

It is recommended a Schottky barrier diode having a smaller V_F than the parasitic diode V_F of the Lo-side MOSFET.



Notes:
1) Dimension is in millimeters, *Dimensions in brackets are in inches
2) Drawing is not to scale

Fig. 8-7 Foot printing for SOP8(recommended land Pad)

8.3 Applied Design

8.3.1 Spike Noise Reduction(1)

The addition of the BS serial resistor
The "turn-on switching speed" of the internal Power-MOSFET can be slowed down by inserting R_{BS} (option) of the Fig8-10.It is tendency that Spike noise becomes small by reducing the switching-speed. Set up 10-ohm as an upper limit when you use R_{BS}.
*Attention
1) When the resistance value of R_{BS} is enlarged by mistake too much, the internal power-MOSFET becomes an under-drive,it may be damaged worst.
2) The "defective starting-up" is caused when the resistance value of R_{BS} is too big.
*The BS serial resistor R_{BS} is R3 in the Demonstration Board.

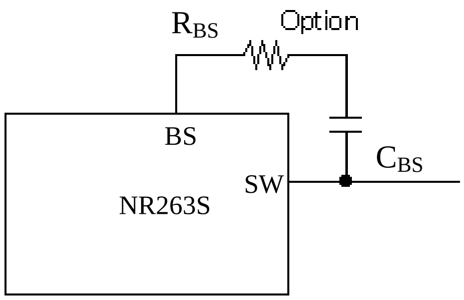


Fig. 8-8 The addition of the BS serial resistor

8.3.2 Spike Noise Reduction(2)

The addition of the Snubber circuit
In order to reduce the spike noise, it is possible to compensate the output waveform and the recovery time of internal parasitic diode by connecting a capacitor and resistor parallel to the internal parasitic diode (snubber method). This method however may slightly reduce the efficiency.
* For observing the spike noise with an oscilloscope, the probe lead (GND) should be as short as possible and connected to the root of output capacitor. If the probe GND lead is too long, the lead may act like an antenna and the observed spike noise may be much higher and may not show the real values.
*The snubber circuit parts are C13 and R10.

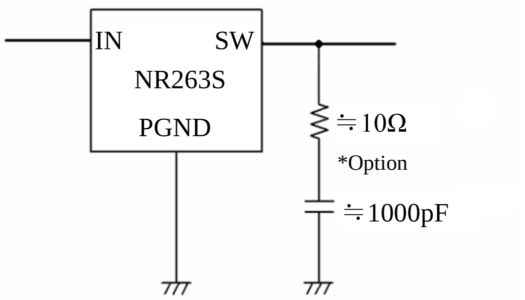


Fig. 8-9 The addition of the Snubber circuit

8.3.3 Attention about the insertion of the bead-core

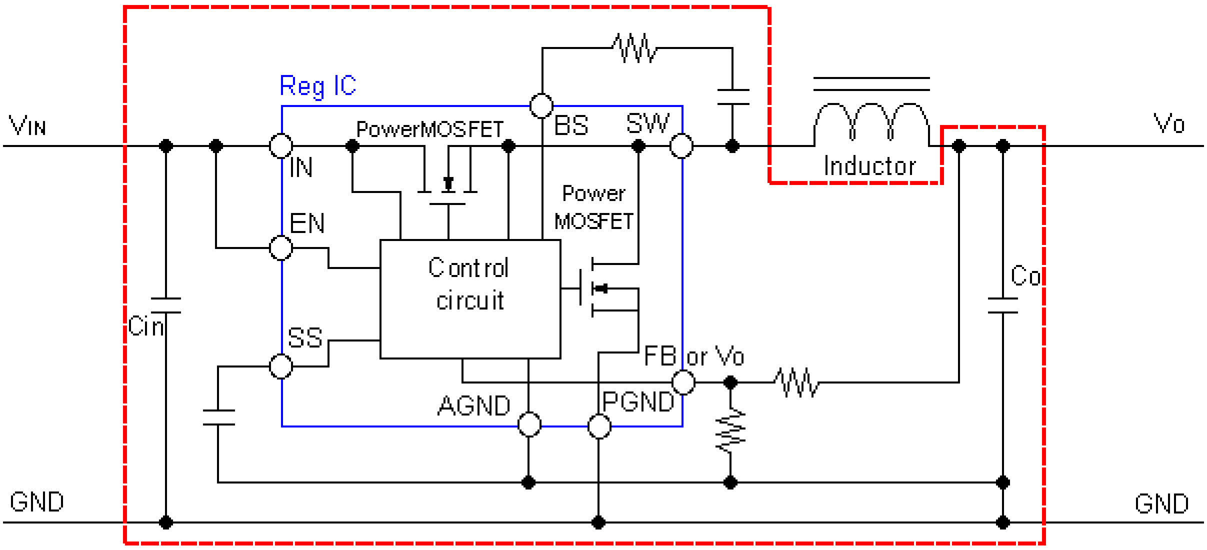


Fig. 8-10 Bead core insertion prohibited area

In the area surrounded by the red dotted line within the Fig8-12, don't insert the bead-core such as Ferrite-bead.
As for the pattern-design of printed-circuit-board, it is recommended that the parasitic-inductance of wiring-pattern is made small for the safety and the stability.
When bead-core was inserted, the inductance of the bead-core is added to parasitic-inductance of the wiring-pattern.
By this influence, the surge-voltage occurs often, or , AGND & PGND of IC becomes unstable, and also, negative voltage occurs often.
Because of this, faulty operation occurs in the IC. The IC has the possibility of damage in the worst case.
About the Noise-reduction, fundamentally, Cope by "The addition of BS serial resistor" and "The addition of CR snubber circuit".

8.3.4 Reverse Bias Protection

A diode for reverse bias protection may be required between input and output in case the output voltage is expected to be higher than the input Pin voltage (a common case in battery charger applications).

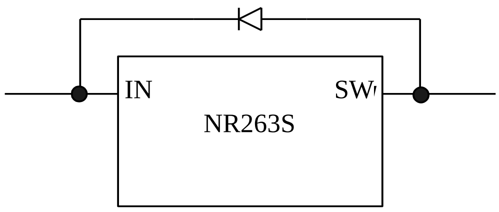


Fig. 8-11 Reverse bias protection diode

8.3.5 Overvoltage protection of VO terminal

If the hot-swap is done by such as load-line connector when the DC / DC converter circuit is in operation, the surge voltage due to hot-swap will occur on the Vo output circuit. In your use condition, please be careful so that the voltage applied to the VO terminal does not exceed the absolute maximum rating (6V). For problems such as the reverse-flow from the external circuit, please take measures. Nevertheless, if you can not suppress an overvoltage factors by the surge voltage such as when the hot-swap was done, please protect the VO terminal by inserting the R_{VO} as shown in Fig8-14. The resistance of R_{VO} as a guide is defined as 100Ω. And, by inserting of the R_{VO} (= 100Ω) to the sensing line, the output voltage V_O(=5V(typ)) will rise further +5mV equivalent.

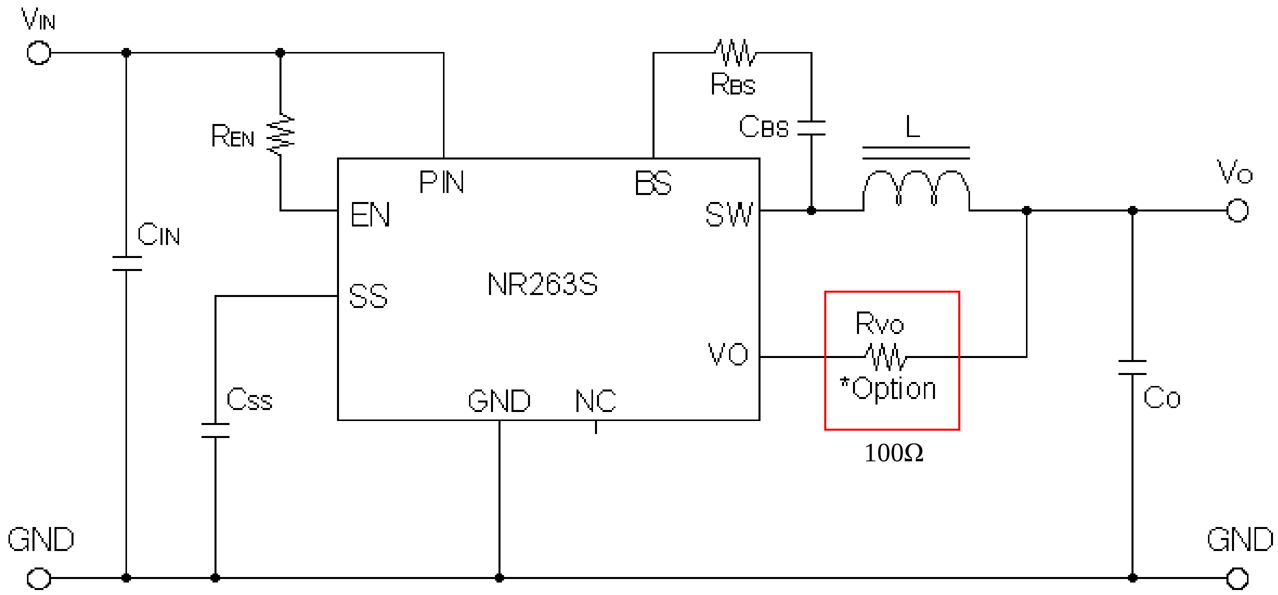
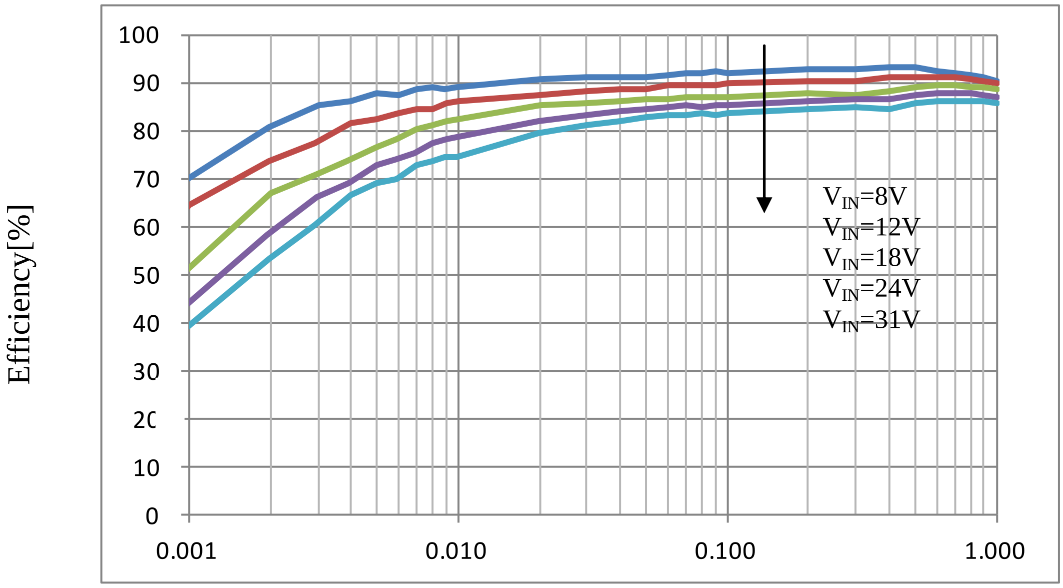


Fig. 8-12 The resistor R_{VO} for overvoltage protection of theVO terminal

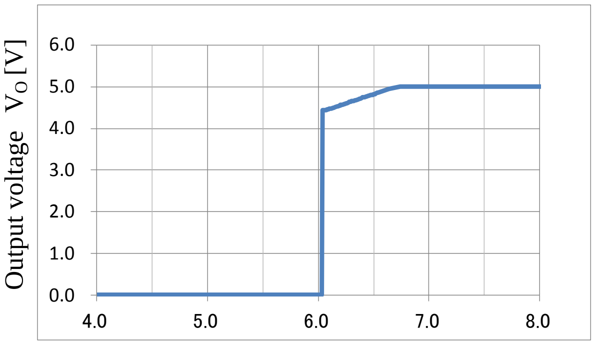
9. Typical characteristics (Ta=25°C)

(1)Efficiency



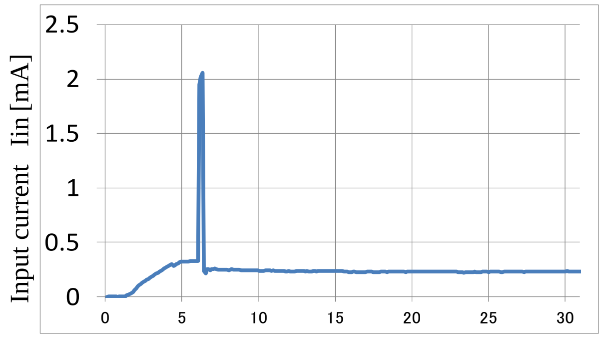
Output Current Io [A]
Fig. 9-1

(2) Output startup Io=1A



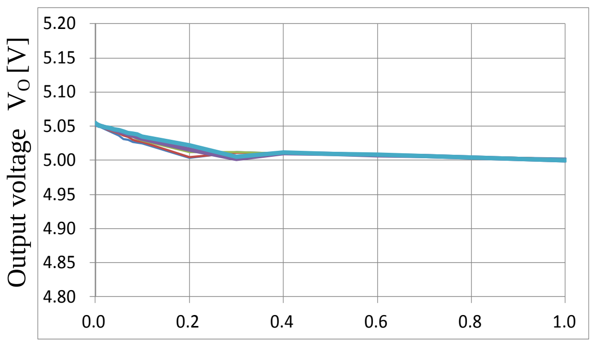
Input voltage V_{IN} [V]
Fig. 9-3

(4) Supply Current : I_{IN}



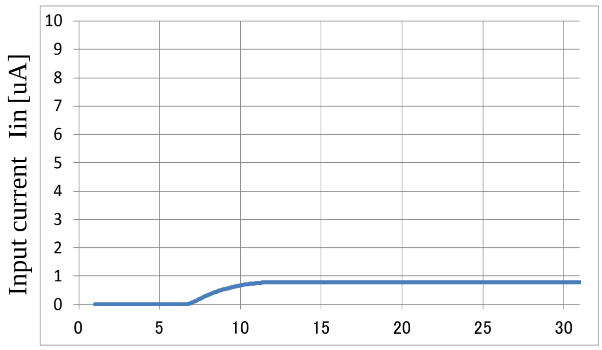
Input voltage V_{IN} [V]
Fig. 9-2

(3) Load Regulation : V_{Load}



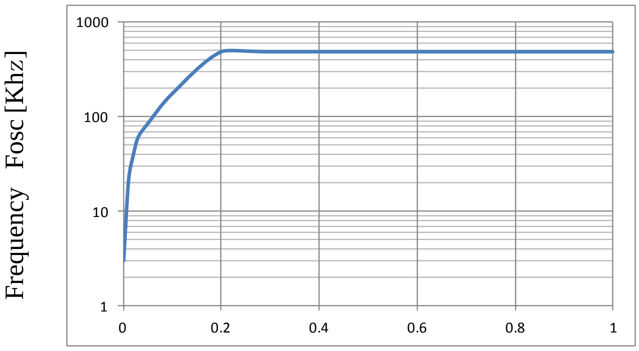
Output current Io [A]
Fig. 9-4

(5) Shutdown Supply Current : $I_{in(off)}$



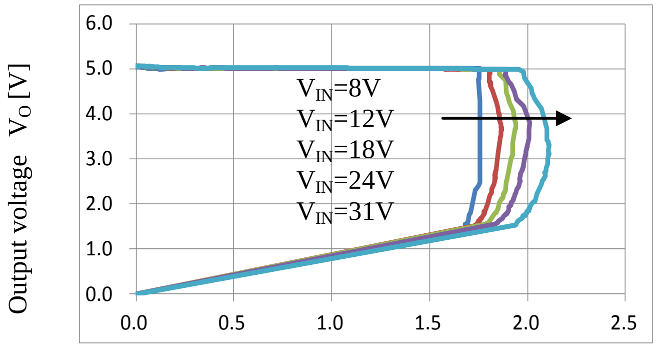
Input voltage V_{IN} [V]
Fig. 9-5

(6)Switching frequency : Fosc



Output current Io [A]
Fig. 9-7

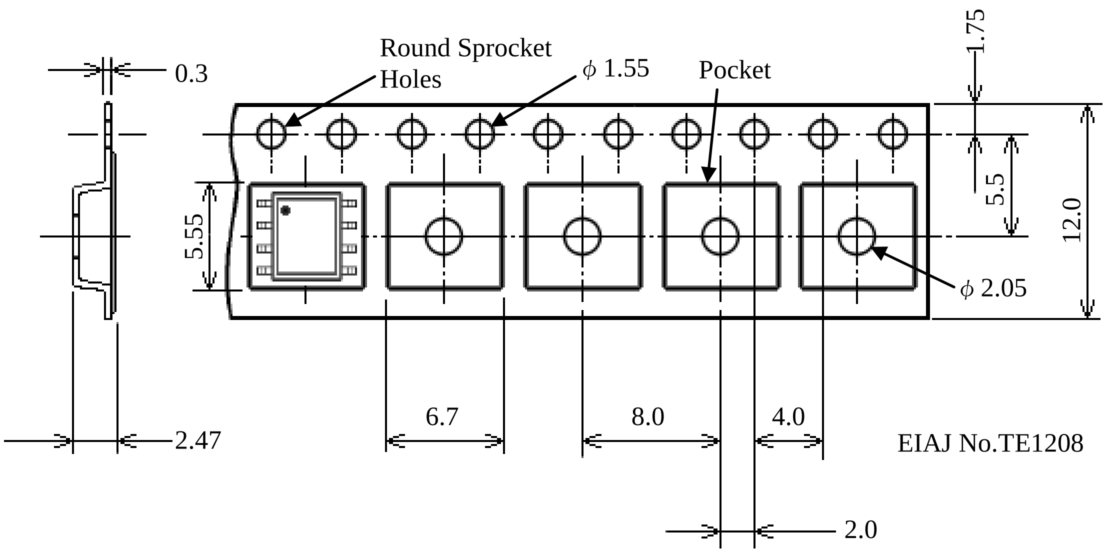
(7)Over current protection



Output current Io [A]
Fig. 9-6

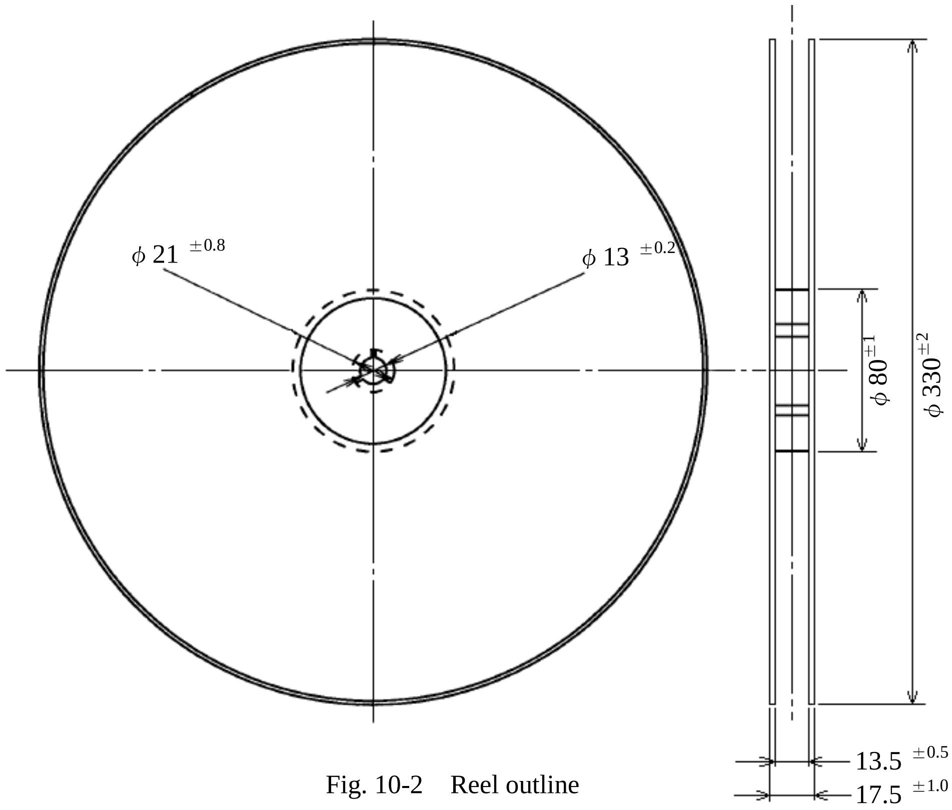
10. Packing specifications

10.1 Taping & Reel outline



Notes:
1) All dimensions in millimeters (mm)
2) Surface resistance : under $10^9\Omega$
3)Drawing is not to scale

Fig. 10-1 Taping outline



Notes:
1) All dimensions in millimeters (mm)
2) Drawing is not to scale

EIAJ No.RRM-12DC

Quantity (TBD)
4000pcs／reel

Fig. 10-2 Reel outline

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