

SBOS187C – OCTOBER 2001 – REVISED JULY 2005

4-20mA, TWO-WIRE TRANSMITTER
"Smart" Programmable with Signal Conditioning

FEATURES

- COMPLETE TRANSMITTER + RTD LINEARIZATION
- TWO-WIRE, 4-20mA OUTPUT
- VOLTAGE OUTPUT (0.5V to 4.5V)
- ELIMINATES POTENTIOMETERS AND TRIMMING
- DIGITALLY CALIBRATED
- 5V SUB-REGULATOR OUTPUT
- SERIAL SPI™ BUS INTERFACE
- SSOP-24 PACKAGE

APPLICATIONS

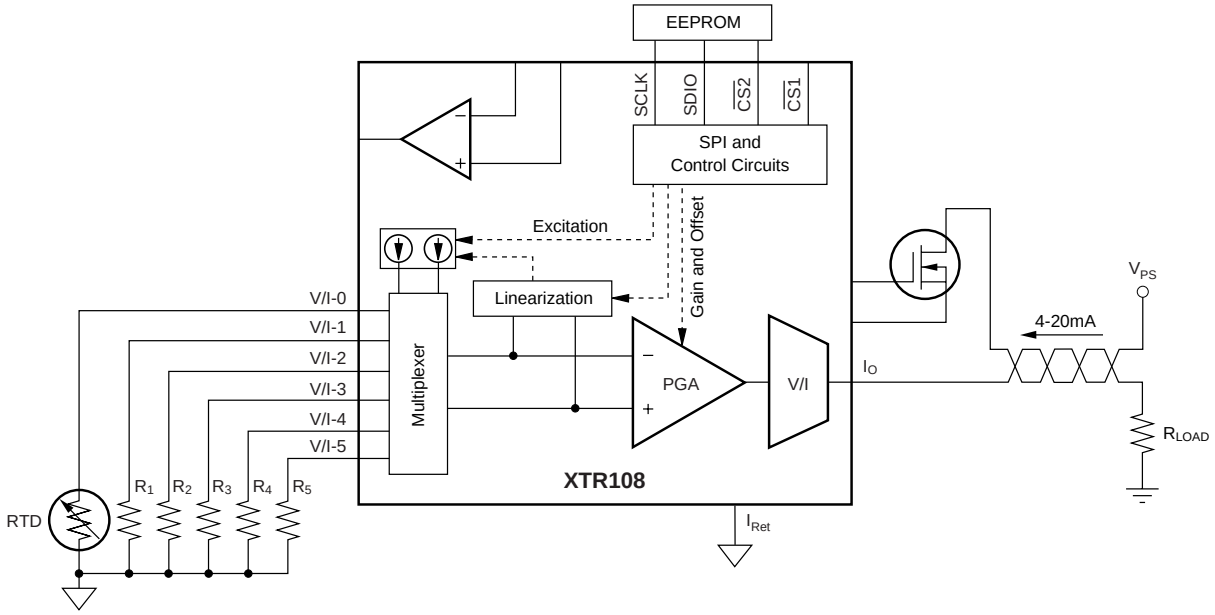
- REMOTE RTD TRANSMITTERS
- PRESSURE BRIDGE TRANSMITTERS
- STRAIN GAGE TRANSMITTERS
- SCADA REMOTE DATA ACQUISITION
- WEIGHING SYSTEMS
- INDUSTRIAL PROCESS CONTROL

DESCRIPTION

The XTR108 is a "smart," programmable, 4-20mA, two-wire transmitter designed for temperature and bridge sensors. Zero, span, and linearization errors in the analog signal path can be calibrated via a standard digital serial interface, eliminating manual trimming. Non-volatile external EEPROM stores calibration settings.

The all-analog signal path contains an input multiplexer, autozeroed programmable-gain instrumentation amplifier, dual programmable current sources, linearization circuit, voltage reference, sub-regulator, internal oscillator, control logic, and an output current amplifier. Programmable level shifting compensates for sensor DC offsets. Selectable up- and down-scale output indicates out-of-range and burn-out per NAMUR NE43. Automatic reset is initiated when supply is lost.

Current sources, steered through the multiplexer, can be used to directly excite RTD temperature sensors, pressure bridges, or other transducers. An uncommitted op amp can be used to convert current into a voltage. The XTR108 is specified for –40°C to +85°C.



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ABSOLUTE MAXIMUM RATINGS(1)

Loop Supply Voltage, V_{PS}	Dependent on External FET
XTR Supply Voltage, External V_S (Referenced to I_{RET} Pin)	+5.5V
Input Voltage to Multiplexer (Referenced to I_{RET} Pin)	0V to V_S
Output Current Limit	Continuous
Storage Temperature Range	–55°C to +125°C
Junction Temperature	+165°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
XTR108EA	SSOP-24	DBQ	–40°C to +85°C	XTR108EA	XTR108EA	Rails
"	"	"	"	"	XTR108EA/2K5	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**

At T_A = +25°C, V_{PS} = 24V, and Supertex DN2540 external depletion-mode FET transistor, unless otherwise noted, all voltages measured with respect to I_{RET} pin.

PARAMETER	CONDITIONS	XTR108EA MIN	XTR108EA TYP	XTR108EA MAX	UNITS
V_{IN} TO I_{OUT} TRANSFER FUNCTION	$I_O = V_{IN}$ (Span) + 4mA				
Output					
Specified Range		4		20	mA
Over-Scale Limit Resolution	Digital Select: 21-28.5mA		0.5		mA
Fault Over-Scale Level(1)	Above Over-Scale Selected		+1.0		mA
Under-Scale Limit Resolution	Digital Select: 2.2-3.6mA		0.2		mA
Fault Under-Scale Level(1)	Below Under-Scale Selected		–0.4		mA
Output for Zero Input					
Zero Error, Unadjusted	V_{IN} = 0V		±50		µA
vs Temperature			±0.2	±1.5	µA/°C
vs Loop-Supply Voltage, V_{LOOP}	V_{LOOP} = 7.5V to 24V		0.02		µA/V
vs Common-Mode Voltage	V_{CM} = 0.2V to 3.5V		±1		µA/V
Adjustment Resolution, Zero Input			1.8		µA/Step
Adjustment Range, Zero Input			±4		mA
Span(2)	Span = I_O/V_{IN}				
Initial, Unadjusted			±1		%
Drift (vs Temperature)			40		ppm/°C
Span Adjustment Resolution			0.05		%
Span Adjustment Range					
PGA + Output Amplifier(3)	R_{VI} = 6.34kΩ	49.3		3150	mA/V
Nonlinearity, Ideal Input	Full-Scale V_{IN} = 50mV		0.01		%
PGA					
Autozeroing Internal Frequency			6.5		kHz
PGA Offset Voltage (RTI)(4)	V_{CM} = 1V		±10	±50	µV
vs Temperature			±0.02		µV/°C
vs Supply Voltage, V_S	V_S = 4.5V to 5.5V		±0.5		µV/V
vs Common-Mode Voltage	V_{CM} = 0.2V to 3.5V		105		dB
Common-Mode Input Range		0.2		V_S – 1.5	V
Input Bias Current			50		pA
vs Temperature			Doubles/10°C		pA
Input Offset Current			10		pA
vs Temperature			Doubles/10°C		pA

ELECTRICAL CHARACTERISTICS (Cont.)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**

At T_A = +25°C, V_{PS} = 24V, and Supertex DN2540 external depletion-mode FET transistor, unless otherwise noted, all voltages measured with respect to I_{RET} pin.

PARAMETER	CONDITIONS	XTR108EA MIN	XTR108EA TYP	XTR108EA MAX	UNITS
PGA (Cont.)					
Input Impedance: Differential			30 || 6		GΩ || pF
Input Impedance: Common-Mode			50 || 20		GΩ || pF
Voltage Noise, 0.1Hz to 10Hz			6		µVp-p
PGA Gain					
Gain Range Steps	6.25, 12.5, 25, 50, 100, 200, 400	6.25		400	V/V
Initial Error	Gain = 6.25, 12.5, 25, 50		±0.5	±2.5	%
	G = 100, 200		±0.5	±3	%
	G = 400		±0.8	±3.5	%
vs Temperature			±30		ppm/°C
Output Voltage Range[5]	R_{LOAD} = 6.34kΩ to I_{RET}	0.2		4.5	V
Typical Operating Range	for 4-20mA XTR Output		0.5 to 2.5		V
Capacitive Drive			200		pF
Short-Circuit Current			+6/–9		mA
ZERO OFFSET DACS					
Zero-Code Output Level	V_{CM} = 1V, V_{IN} = 0V				
RTO[6] of Current Amplifier	$R_{V/I}$ = 6.34kΩ		4.116		mA
RTO[6] of PGA			522		mV
Coarse DAC, 256 Steps			7 Bits + Sign		
Adjustment Range	Relative to Zero-Code Level				
RTO[6] of Current Amplifier			–3.77 to +3.77		mA
RTO[6] of PGA			–470 to +470		mV
Step Size					
RTO[6] of Current Amplifier			0.029		mA
RTO[6] of PGA			3.7		mV
Linearity			±0.5		LSB
Fine DAC, 256 Steps	Relative to Zero-Code Level		7 Bits + Sign		
Adjustment Range					
RTO[6] of Current Amplifier			–236 to +236		µA
RTO[6] of PGA			–29.4 to +29.4		mV
Step Size					
RTO[6] of Current Amplifier			0.0018		mA
RTO[6] of PGA			0.23		mV
Linearity			±1		LSB
Noise, RTO[6]	f = 0.1Hz to 10Hz		1.1		µAp-p
CURRENT AMPLIFIER					
Current Gain		49	50	51	A/A
Current Gain Drift			10		ppm/°C
CURRENT SOURCES, I_{REF1} AND I_{REF2}					
Zero-Code Output Level, Each	R_{SET} = 12.1kΩ	480	493	510	µA
Coarse DAC, 256 Steps			7 Bits + Sign		
Adjustment Range[7]			–195 to +195		µA
Step Size			1.54		µA
Fine DAC, 256 Steps			7 Bits + Sign		
Adjustment Range[7]			–12.2 to +12.2		µA
Step Size			96		nA
Linearity					
Coarse			±0.2		LSB
Fine			±0.5		LSB
vs Temperature			±35		ppm/°C
Matching			±0.2		%
vs Temperature			±10		ppm/°C
Compliance Voltage, Positive[5]		V_S – 2	V_S – 1.5		V
Output Impedance			100		MΩ
Current Noise	f = 0.1Hz to 10Hz		0.015		µAp-p
LINEARIZATION DAC					
Linearization Range, 256 Steps			8 Bits		
Max Linearization Coefficient	$\Delta I_{REF}/\Delta V_{IN}$, R_{LIN} = 15.8kΩ		0.99		µA/mV
Step Size			3.9		nA/mV
SUB-REGULATOR, V_S	Supply Voltage for XTR				
Voltage		4.8	5.1	5.4	V
vs Temperature			±50		ppm/°C
vs Loop-Supply Voltage	V_{LOOP} = 7.5V to 24V		±0.03		mV/V

ELECTRICAL CHARACTERISTICS (Cont.)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**

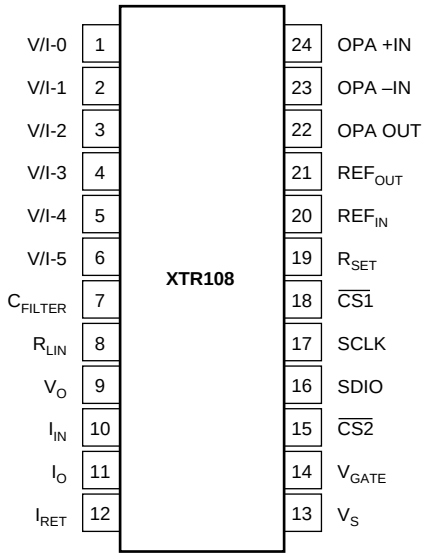
At T_A = +25°C, V_{PS} = 24V, and Supertex DN2540 external depletion-mode FET transistor, unless otherwise noted, all voltages measured with respect to I_{RET} pin.

PARAMETER	CONDITIONS	XTR108EA MIN	XTR108EA TYP	XTR108EA MAX	UNITS
OVER- AND UNDER-SCALE LIMITING					
Over-Scale DAC: 16 Steps			4		Bits
Adjustment Range					
RTO(6) of Current Amplifier	R_{VI} = 6.34kΩ		20.7 to 28.1		mA
RTO(6) of PGA			2.625 to 3.563		V
Step Size					
RTO(6) of Current Amplifier			0.49		mA
RTO(6) of PGA			62.5		mV
Accuracy			±10		%
Under-Scale DAC: 8 Steps			3		Bits
Adjustment Range					
RTO(6) of Current Amplifier	R_{VI} = 6.34kΩ		2.17 to 3.55		mA
RTO(6) of PGA			275 to 450		mV
Step Size					
RTO(6) of Current Amplifier			0.195		mA
RTO(6) of PGA			25		mV
Accuracy			±5		%
VOLTAGE REFERENCE, V_{REF}					
Internal Bandgap			1.193		V
vs Temperature			±5	±50	ppm/°C
UNCOMMITTED OP AMP					
Input					
Offset Voltage	V_{CM} = 2V		±2		mV
vs Temperature			±3		µV/°C
vs Common-Mode Voltage			90		dB
Open-Loop Gain			110		dB
Common-Mode Input Range			0 to 3.5		V
Output Voltage Range	R_L = 10kΩ to V_S/2	0.2		V_S – 0.2	V
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels					
V_{IL}		0		0.8	V
V_{IH}		3.5		V_S	V
V_{OL}	I_{OL} = 300µA			0.4	V
V_{OH}	I_{OH} = –300µA	V_S – 1			V
Input Current					
I_{IH} ($\overline{CS1}$)	3.5 < V_{IN} < V_S	–200	–120	10	µA
I_{IL} ($\overline{CS1}$)	0 < V_{IN} < 0.8	–20	–6	10	µA
I_{IH}, I_{IL} (SCLK, DIO)	0 < V_{IN} < V_S	–20	–6	10	µA
INTERNAL OSCILLATOR					
Frequency, f_{OSC}			210		kHz
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operating		–55		+125	°C
θ_{JA}, Junction to Ambient			100		°C/W
LOOP SUPPLY					
Voltage Range	with Supertex DN2540	7.5			V
Quiescent Current	R_{SET} Open, L_{IN}Reg = 0, No Sensor Current(8)(9)		0.5		mA

NOTES: (1) Over-scale and under-scale complies with NAMUR NE43 recommendation. (2) Span adjustment is determined by PGA gain and sensor excitation. (3) Span can be digitally adjusted in three ways: PGA gain, current reference Coarse, and current reference Fine. (4) RTI = Referred to Input. (5) Current source output voltage measured with respect to I_{RET}. (6) RTO = Referred to Output. (7) Excitation DAC range sufficient to adjust span fully between PGA gain steps. (8) Output current into external circuitry is limited by an external MOS power FET. (9) Measured with over- and under-scale limits disabled.

PIN CONFIGURATION

Top View **SSOP**



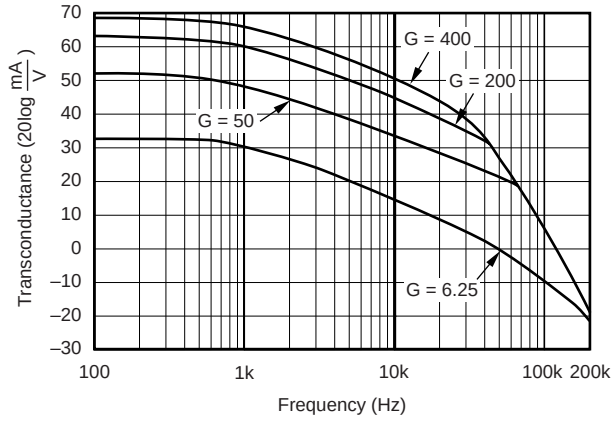
PIN ASSIGNMENTS

PIN	NAME	FUNCTION
V/I-0	MUX Input Channel 0 and/or I_{REF} Out	MUX Input to PGA and/or I_{REF} to Sensor
V/I-1	MUX Input Channel 1 and/or I_{REF} Out	MUX Input to PGA and/or I_{REF} to Sensor
V/I-2	MUX Input Channel 2 and/or I_{REF} Out	MUX Input to PGA and/or I_{REF} to Sensor
V/I-3	MUX Input Channel 3 and/or I_{REF} Out	MUX Input to PGA and/or I_{REF} to Sensor
V/I-4	MUX Input Channel 4 and/or I_{REF} Out	MUX Input to PGA and/or I_{REF} to Sensor
V/I-5	MUX Input Channel 5 and/or I_{REF} Out	MUX Input to PGA and/or I_{REF} to Sensor
C_{FILTER}	Filter Capacitor	Filter to Reduce Chopper Noise in Autozeroing PGA
R_{LIN}	Linearization	Linearization Range Adjustment Resistor
V_O	PGA Output	PGA Amplified Output of Differential Sensor Input
I_{IN}	Current Input	Input to Output Current Amplifier
I_O	Output Current	4-20mA Current for Output Loop
I_{RET}	Return Current	Return for All External Circuitry Current
V_S	Voltage Regulator	Supply Voltage for XTR and External Circuitry, If Used
V_{GATE}	Gate Voltage	Gate Voltage for External MOSFET Transistor
$\overline{CS2}$	Chip Select 2	Select for XTR Serial Port to External EEPROM (Output from XTR Only)
SDIO	Serial Data Input/Output	Serial Data Input or Output
SCLK	Serial Clock	Serial Clock
$\overline{CS1}$	Chip Select 1	Select for External µC Serial Port (Input to XTR Only)
R_{SET}	Resistor for Reference	Sets Current Reference
REF_{IN}	Voltage Reference Input	Voltage Reference Input to XTR
REF_{OUT}	Voltage Reference Output	Voltage Reference Output from Internal Bandgap
OPA OUT	Uncommitted Op Amp Output	Uncommitted Op Amp Output
OPA –IN	Uncommitted Op Amp Negative Input	Uncommitted Op Amp Negative Input
OPA +IN	Uncommitted Op Amp Positive Input	Uncommitted Op Amp Positive Input

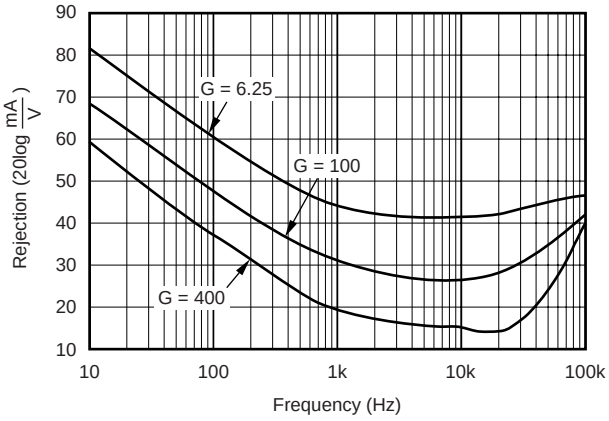
TYPICAL CHARACTERISTICS

At T_A = +25°C, V+ = 24V, unless otherwise noted. R_{VI} = 6.34kΩ.

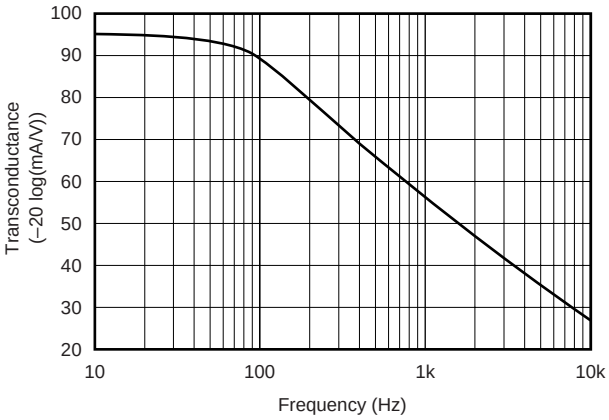
TRANSCONDUCTANCE vs FREQUENCY



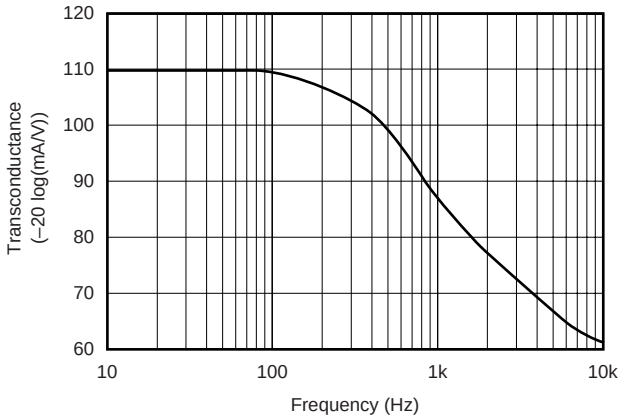
COMMON-MODE REJECTION vs FREQUENCY



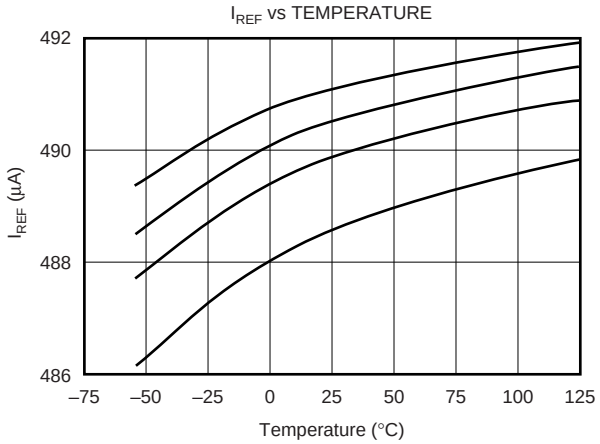
I_{ZERO} V_{LOOP} REJECTION RATIO vs FREQUENCY



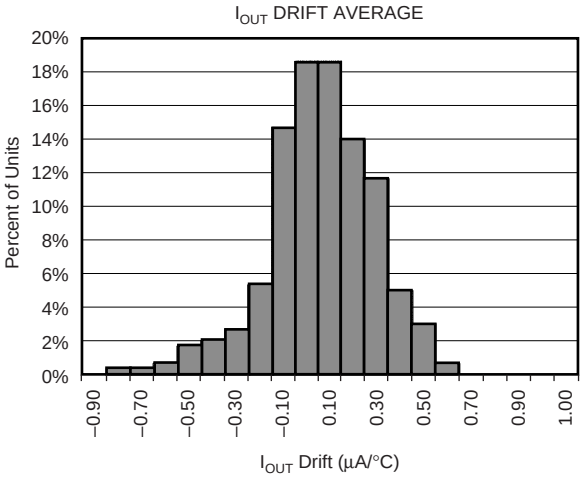
I_{REF} V_{LOOP} REJECTION RATIO vs FREQUENCY



I_{REF} vs TEMPERATURE



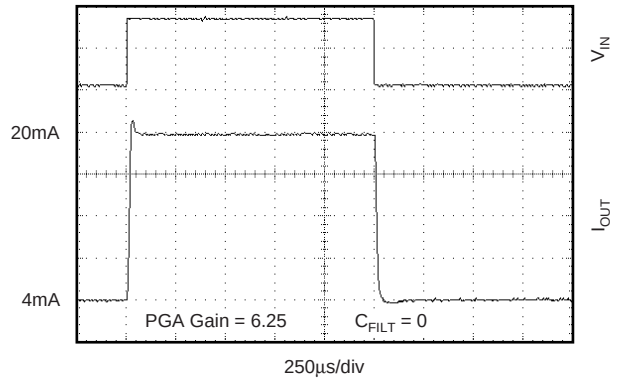
I_{OUT} DRIFT AVERAGE



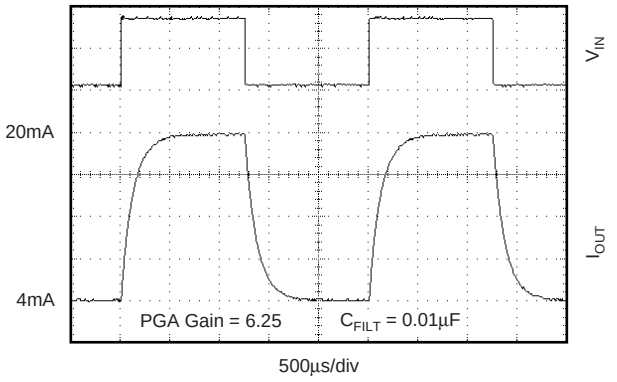
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V+ = 24V, unless otherwise noted. R_{VI} = 6.34kΩ.

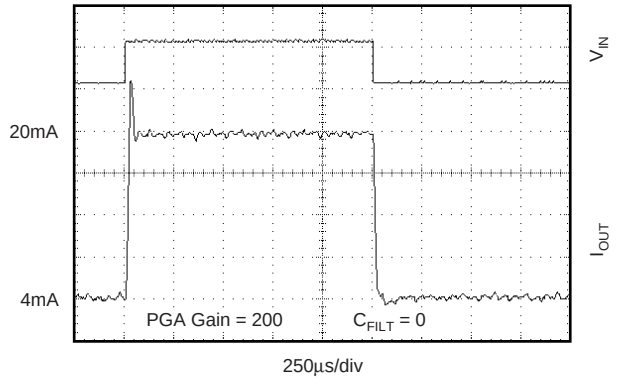
LARGE INPUT STEP RESPONSE



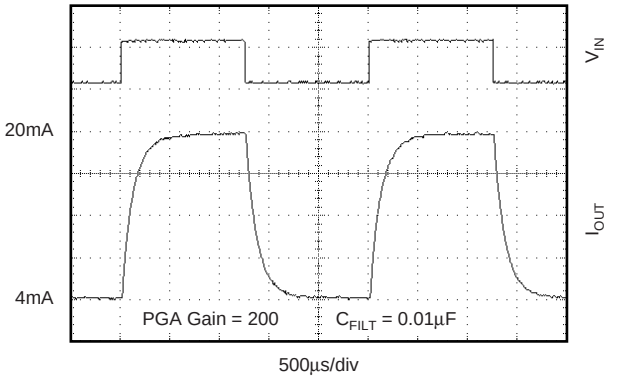
LARGE INPUT STEP RESPONSE



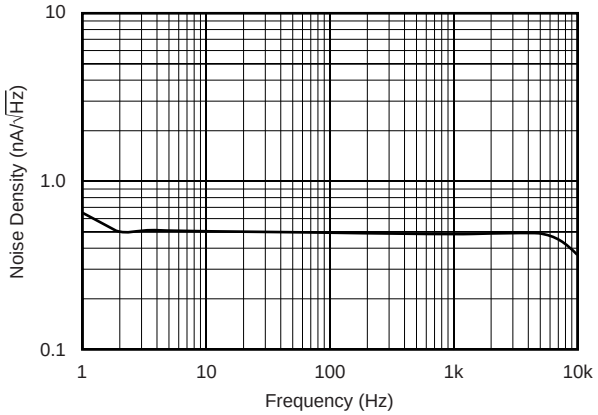
SMALL INPUT STEP RESPONSE



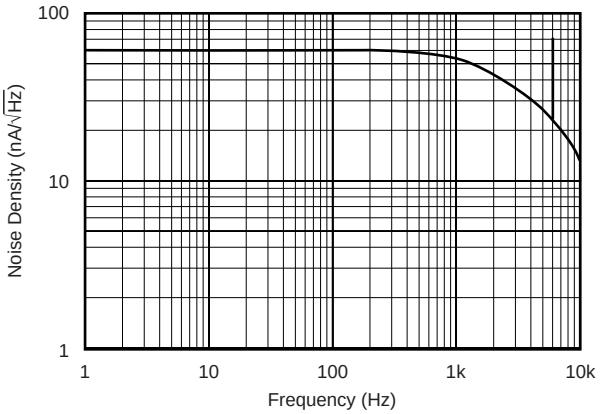
SMALL INPUT STEP RESPONSE



I_{REF} NOISE POWER

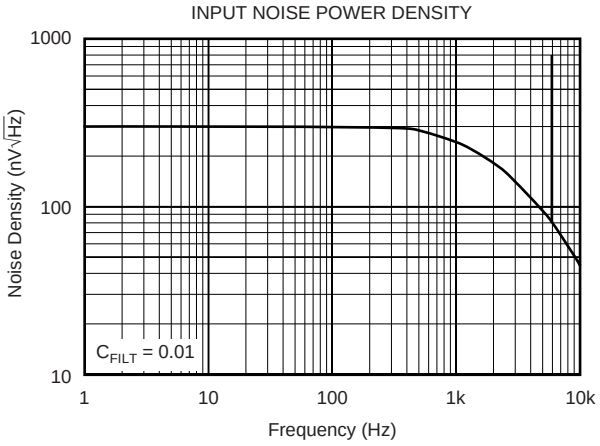


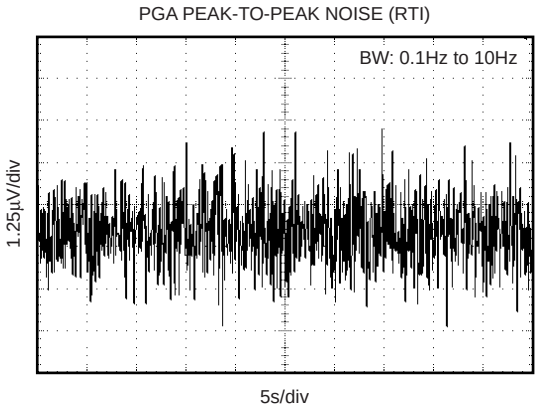
I_{ZERO} CURRENT NOISE POWER



TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V+ = 24V, unless otherwise noted. R_{VI} = 6.34kΩ.





OVERVIEW

The XTR108 is a 4-20mA current-loop transmitter that allows the user to digitally adjust the gain, offset, and linearity correction of the analog output to calibrate the sensor. The digital data for adjustment are stored in an external EEPROM device.

The analog signal path is composed of a compound multiplexer (MUX), programmable gain instrumentation amplifier (PGA), and an output current amplifier. Analog support functions include digitally controlled current sources for sensor excitation, PGA offset control, linearization, voltage reference, and voltage regulator.

The digital interface communicates with external devices for calibration and to store the resultant data in an SPI compatible EEPROM. A complete system is shown in Figure 1. The XTR108 serial interface is SPI compatible and only requires four connections to the calibration controller: a serial clock (SCLK), a serial data line (SDIO), a chip select line ($\overline{CS1}$), and a ground sense line. All logic signals to the XTR108 must be referenced to the potential of the ground sense line (I_{RET} pin on the XTR108).

Within this entire system there may exist three different "GND" voltage levels. In addition, the voltage difference between the I_{RET} and I_O potential will depend on the output current level. It is not certain that the "GND" potential of the calibration system will be at the same potential of either the I_{RET} or I_O potential, and therefore the isolation couplers are shown in Figure 1. All voltages specified for the XTR108 are with reference to the I_{RET} pin.

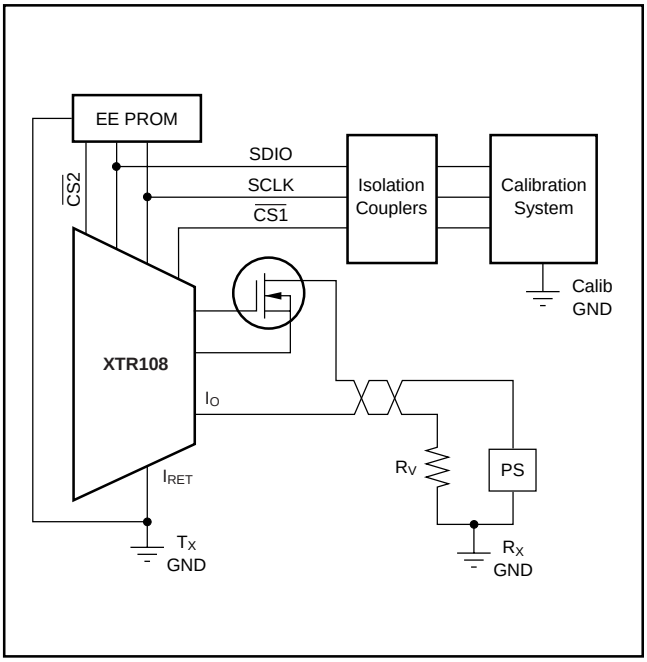


FIGURE 1. Complete System Level Configuration with Three Unique Ground Voltage Levels.

The XTR108 also needs to communicate with the external EEPROM device independently from the calibration controller to retrieve the calibration constants during normal operation. The XTR108 provides a second chip select function ($\overline{CS2}$) for the EEPROM device to facilitate this communication.

THEORY OF OPERATION

REFERENCE

The XTR108 has an on-board precision bandgap voltage reference with output at pin 21 (REF_{OUT}). The value of the reference is factory-trimmed to 1.193V, with a typical temperature drift of 5ppm/°C. Pins 21 (REF_{OUT}) and 20 (REF_{IN}) must be connected together to use the internal reference.

External circuitry, such as a voltage excited sensor or an Analog-to-Digital Converter (ADC), can be connected to the REF_{OUT} pin. The unbuffered REF_{OUT} is capable of sourcing current but not sinking.

If the application necessitates, an external reference can be connected to the XTR108 REF_{IN} pin, as long as the reference does not exceed 1.4V. The REF_{IN} pin has a high input impedance with the input current not exceeding a few nanoamps.

INPUT MULTIPLEXER

The XTR108 input multiplexer is a full 6 by (2+2) cross-point switch. The current references and PGA inputs can be independently connected to any of the six external pins, including simultaneous connections to the same pin. This allows a great flexibility in the sensor excitation and input configuration. The input pins must not be driven below the I_{RET} potential or above V_S.

See Figure 2 for an RTD sensor connected to pin $V_{IN}0$ with both I_{REF} supplied and PGA V_{IN+} sensed at that pin. The other five input pins are used for a bank of R_Z resistors that can be selected during the calibration process for a particular measurement range.

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

The programmable gain instrumentation amplifier has seven voltage-gain settings in binary steps from 6.25V/V to 400V/V. The input common-mode range of the PGA is 0.2V to 3.5V above the I_{RET} potential.

Normally, in the application for 4-20mA transmitters, the PGA output voltage range should be set to V_{ZERO} = 0.5V and V_{FS} = 2.5V. Connecting a resistor (R_{VI} = 6.34kΩ) between pin 9 (V_O) and pin 10 (I_{IN}) converts this voltage to the signal for the output amplifier that produces a 4-20mA scale current output. In this mode, the PGA voltage gain converts to an overall transconductance in the range of 50mA/V to 3200mA/V (approximately). Table I shows the gain to transconductance relationship.

VOLTAGE GAIN V/V	6.25	12.5	25	50	100	200	400
OUTPUT TRANSCONDUCTANCE mA/V	49	99	197	394	789	1577	3155
FULL-SCALE DIFFERENTIAL V_{IN} mV	320	160	80	40	20	10	5

TABLE I. PGA Gain, Corresponding Loop Transductance and Input Full-Scale Differential Voltage.

If over-scale and under-scale limiting is disabled, the PGA can be used with rail-to-rail voltage output, for example, in applications that require a 0.5V to 4.5V voltage scale.

The PGA uses advanced auto-zero circuit techniques to achieve high DC precision, and reduce mismatches and errors within the chip such as input offset, offset temperature drift, and low-frequency noise (see the input noise typical characteristic).

The basic clock frequency of the auto-zero loop is about 6.5kHz. Due to the switching nature of the auto-zero circuit, the output of the PGA can have a noticeable clock feed-through ripple in higher gains. This noise can be reduced by the addition of a 0.01µF capacitor between pin 7 (C_{FILTER}) and the local ground, pin 12 (I_{RET}). This creates a one-pole low-pass filter with –3dB frequency at about 1.5kHz. If wider bandwidth or faster settling time is needed, the C_{FILTER} can be reduced or eliminated at the expense of higher glitch amplitude at the output. Please refer to the typical step response traces for settling time comparisons.

ZERO DACS

Two output-referred, 8-bit Digital-to-Analog Converters (DACs) (coarse and fine with a pedestal) set the zero level of the PGA output. They allow setting a desired zero-scale output level and compensate the initial offset at the PGA input due to the sensor and resistor mismatches, sensor non-idealities, etc. Both coarse and fine DACs are bidirectional and allow the output level to be set above or below a preset pedestal.

Output signals of the DACs, $I_{Z\ COARSE}$ and $I_{Z\ FINE}$, are summed with the pedestal, $I_{Z\ PROGRAM}$. Each of the DACs has 8-bit resolution (256 steps) with 4-bit overlap between the coarse and fine DACs. This means that one LSB of the coarse DAC is equal to 16 fine LSBs, and the full-scale range of the fine DAC is equal to 16 coarse LSBs. This effectively produces 12-bit adjustment resolution.

This overlap allows the user to set pre-calculated values before the calibration, using the coarse DAC only and adjust the zero output level with the fine DAC during the calibration process see Table II for the equations for calculating the value of the output when zero differential voltage is applied at the PGA input. For the adjustment range, LSB sizes, and linearity values of the Zero DACs, please refer to the electrical characteristics table.

Note that a DAC can be set to a value that produces an output below the under-scale level. In this case, the under-scale limit will prevent the output from getting to the desired value. The value of the minimum scale should not be set so low that the PGA voltage output, V_O, goes below its specified range of 0.2V from I_{RET}.

ADJUSTABLE OVER-SCALE AND UNDER-SCALE LIMITING CIRCUIT

The XTR108 incorporates circuitry to set adjustable limits at the output in cases when the sensor signal goes above or below its range. There are 16 levels for over-scale limit adjustment (4-bit DAC) and 8 levels for the under-scale (3-bit DAC).

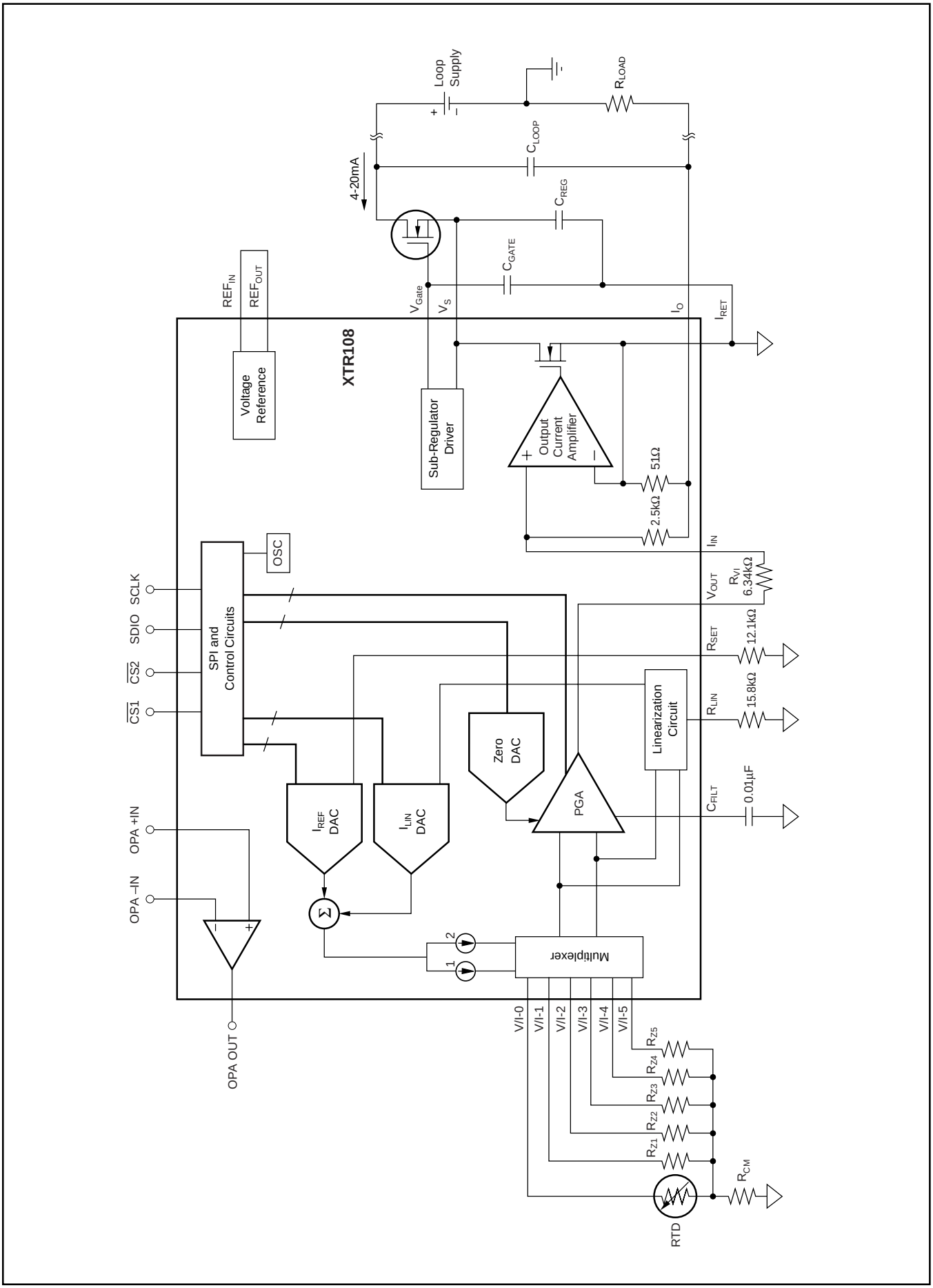


FIGURE 2. XTR108 Internal Block Diagram.

	VOLTAGE REFERRED TO V_O PIN WITH RESPECT TO I_{RET}	CURRENT REFERRED TO I_{OUT} PIN
OVERALL	$V_{ZERO} = V_{Z\ PROGRAM} + V_{Z\ COARSE} + V_{Z\ FINE}$	$I_{ZERO} = I_{Z\ PROGRAM} + I_{Z\ COARSE} + I_{Z\ FINE}$
PROGRAM	$V_{Z\,PROGRAM} = \frac{3.5V_{REF}}{8}$	$I_{Z\,PROGRAM} = \frac{175V_{REF}}{8R_{VI}}$
COARSE DAC	$V_{Z\,COARSE} = \frac{V_{REF}}{80} \bullet \frac{N_{13}}{4}$	$I_{Z\,COARSE} = \frac{5V_{REF}}{8R_{VI}} \bullet \frac{N_{13}}{4}$
FINE DAC	$V_{Z\,FINE} = \frac{V_{REF}}{80} \bullet \frac{N_{12}}{64}$	$I_{Z\,FINE} = \frac{5V_{REF}}{8R_{VI}} \bullet \frac{N_{12}}{64}$
NOTE: N_{13} and N_{12} are assigned decimal values of registers 13 and 12, respectively.		

TABLE II. Equations for Calculating Zero Output.

The circuit is designed for compliance with NAMUR NE43 recommendation for sensor interfaces. The limit levels are listed in Tables VII and VIII. Because of the large step sizes, units that use this feature should be checked if the value is critical. The under-scale limit circuit will override the Zero DAC level if it is set lower and there is not enough sensor offset at the PGA input.

It may be necessary to disable limiting if the XTR108 is used in applications other than a 4-20mA transmitter, where the PGA output is between 0.5V and 4.5V.

SENSOR FAULT DETECTION CIRCUIT

To detect sensor burnout and/or short, a set of four comparators is connected to the inputs of the PGA. If any of the inputs are taken outside of the PGA's common-mode range, the corresponding comparator sets a sensor fault flag that causes the PGA output to go either to the upper or lower error limit. The state of the fault condition can be read in the digital form from register 3. The direction of the analog output is set according to the "Alarm Configuration Register" (see Table X). The level of the output is produced as follows: if the over-scale/under-scale limiting is enabled, the error levels are: over-scale limit +2LSBs of the over-scale DAC, about 1mA referred to I_{OUT} or 0.125V referred to V_O, of under-scale limit –2LSBs of the under-scale DAC, about 0.4mA referred to I_{OUT} or 0.05V referred to V_O. If the over-scale/under-scale limiting is disabled, the PGA output voltage will go to within 150mV of either positive or negative supply (V_S or I_{RET}), depending on the alarm configuration bit corresponding to the error condition.

OUTPUT CURRENT AMPLIFIER + R_{VI} RESISTOR

To produce the 4-20mA output, the XTR108 uses a current amplifier with a fixed gain of 50A/A. The voltage from the PGA is converted to current by the external resistor, R_{VI}. Pin I_{RET}, the common potential of the circuit (substrate and local ground), is connected to the output and inverting input of the amplifier. This allows collecting all external and internal supply currents, sensor return current, and leakage currents from the different parts of the system and accounting for them in the output current. The current from R_{VI} flows into the pin I_{IN} that is connected to the noninverting input and therefore, is at ground potential as well. The ratio of two matched internal resistors determines a current gain of this block. Note that the I_{OUT} pin is always biased below the substrate potential.

EXCITATION CURRENT DACS AND R_{SET} RESISTOR

Two matched adjustable reference current sources are available for sensor excitation. The defining equations are given in Table III. Both current sources are controlled simultaneously by the coarse and fine DACs with a pedestal.

The external resistor R_{SET} is used to convert the REF voltage into the reference current for the sensor excitation DACs. The total current output of the DACs is split, producing two references: I_{REF1} and I_{REF2}. Both of the current references match very closely over the full adjustment range without mismatched differential steps. Both current reference outputs must be within the compliance range, i.e.: one reference cannot be floated since it will change the value of the other current source.

The recommended value of R_{SET} is 12.1kΩ for use with 100Ω RTD sensors. This generates $I_{REF1,\,2}$ = 492µA currents when both coarse and fine DACs are set to zero. The value of the R_{SET} resistor can be increased if lower reference currents are required, i.e.: for 1000Ω RTD or a bridge sensor.

	REFERENCE CURRENT
OVERALL	$I_{REF1,\,2} = I_{REF\ PROGRAM} + I_{REF\ COARSE} + I_{REF\ FINE}$
PROGRAM	$I_{REF\,PROGRAM} = \frac{5V_{REF}}{R_{SET}}$
COARSE DAC	$I_{REF\,COARSE} = \frac{V_{REF}}{R_{SET}} \bullet \frac{N_{11}}{64}$
FINE DAC	$I_{REF\,FINE} = \frac{V_{REF}}{R_{SET}} \bullet \frac{N_{10}}{1024}$
NOTE: N_{11} and N_{10} are the decimal values of registers 11 and 10, respectively.	

TABLE III. Equations for Calculating the Values of Each Reference Current.

Similar to the Zero DACs, the outputs of the fine and coarse DAC are summed together with the pedestal $I_{REF\ PROGRAM}$. Each of the excitation DACs has 8-bit resolution (256 steps) with 4-bit overlap between the coarse and the fine. This

means that one LSB of the coarse DAC is equal to 16 fine LSBs, and the full-scale range of the fine DAC is equal to 16 coarse LSBs. This effectively produces 12-bit adjustment resolution. This allows the user to set pre-calculated values before the calibration, using the coarse DAC only and adjust the reference current output level with the fine DAC during the calibration process.

LINEARIZATION CIRCUIT AND R_{LIN} RESISTOR

The XTR108 incorporates circuitry for correcting a second-order sensor nonlinearity. A current proportional to the voltage at the input of the PGA is added to the sensor excitation. The R_{LIN} resistor is used to convert this voltage into current. By appropriately scaling this current using the linearization DAC, parabolic sensor nonlinearity can be improved by up to a 40:1 ratio, as shown in Figure 3. The linearization coefficient (ratio of the reference current change to the input voltage) is expressed in μA/mV as follows:

$$G_{LIN} = \frac{\Delta I_{REF}}{V_{IN}} \bullet \frac{N_{14}}{16 \bullet R_{LIN}}$$

where N_{14} is the decimal value from register 14.

The recommended value of the resistor is 15.8kΩ, for use with 100Ω RTD sensors. This value produces a full-scale linearization coefficient of about 1mA/V. Please see the section below on using the XTR108 with an RTD temperature sensor. If the sensor excitation is scaled down by increasing the value of R_{SET}, the value of R_{LIN} should be scaled proportionally.

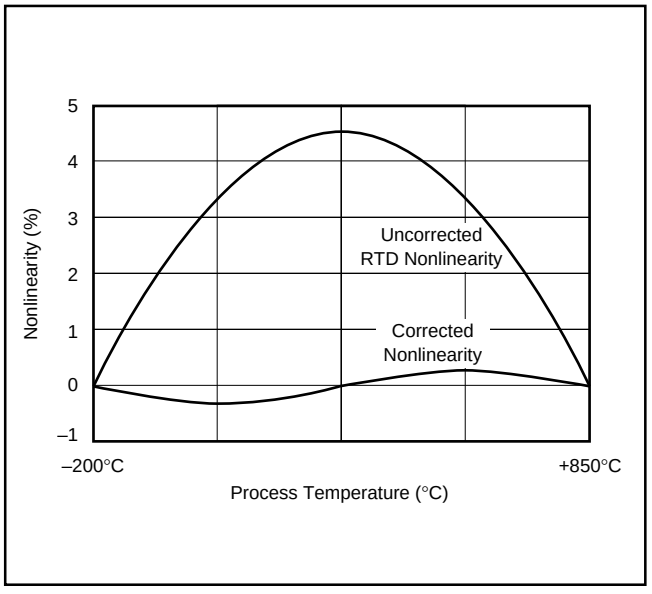


FIGURE 3. Pt100 Nonlinearity Correction Using the XTR108.

SUB-REGULATOR WITH EXTERNAL MOSFET

The XTR108 is manufactured using a low-voltage CMOS process with maximum supply voltage limited to 5.5V. For applications in a 4-20mA current loop, a special sub-regulator circuit is incorporated in the device that requires an external n-channel depletion-mode MOS transistor and three capacitors, see Figure 2.

A number of third-party suppliers make n-channel depletion-mode MOSFETs. A list of devices tested by Texas Instruments, Inc. is shown in Table IV with the capacitor values recommended for those devices.

MANUFACTURER	MOSFET MODEL	C_{GATE} VALUE
Supertex	DN2535, DN2540 DN3535, DN3525	220pF 1000pF
Siliconix	ND2012, ND2020	220pF
Infineon	BSP149	1000pF

TABLE IV. Recommended Gate Capacitor Values For Selected MOSFETs.

The capacitors C_{LOOP} (0.01μF), C_{REG} (2.2μF), and C_{GATE} are required for the regulator loop stability and supply bypass. They should be placed in close proximity to the XTR108 on the PCB. An additional 1μF capacitor may be used to bypass the supply of an EEPROM chip.

If a MOSFET other than those listed in Table IV is used, the value of C_{GATE} should be adjusted such that there is no overshoot of V_S during power-up and supply glitches. Any V_S overshoot above 7.5V may damage the XTR108 or deteriorate its performance.

LOOP VOLTAGE

The XTR108 transmitter minimum loop voltage can somewhat be effected by the choice of the external MOSFET. The devices are tested to 7.5V compliance with Supertex DN2540; choosing other MOSFETs can change this value slightly.

The maximum loop voltage is limited by the power dissipation on the MOSFET as well as its breakdown voltage. Possible ambient temperatures and the power dissipation should be taken into account when selecting the MOSFET package. The external MOSFET can dissipate a considerable amount of power when running at high loop supply. For example, if V_{LOOP} = 24V and I_{OUT} = 20mA, the DC power dissipated by the MOSFET is:

$$P_{MOSFET} = I_{OUT} (V_{LOOP} - V_S) = 380m\Omega$$

For a SOT-89 package soldered on an FR5 board, this will cause a 30°C rise in the temperature. The power dissipation gets significantly higher when the circuit is driven into an over-scale condition. Therefore, special attention should be paid to removing the heat from the MOSFET, especially with small-footprint packages such as SOT-89 and TO-92. Please follow manufacturer's recommendations about the package thermal characteristics and board mounting.

UNCOMMITTED OP AMP

For added flexibility in various applications, the XTR108 has an on-chip uncommitted operational amplifier. The op amp has rail-to-rail output range. The input range extends to I_{RET} potential.

The uncommitted amplifier can be used for a variety of purposes, such as voltage sensor excitation, buffering the REF_{OUT} pin, four-wire RTD connection, or sensing the bridge voltage for temperature compensation.

POWER-GOOD/POWER-ON RESET

In case of a supply brownout condition or short interruption, the XTR108 power-good detection circuit will initiate a chip reset that will cause all registers to be reset to 0's and a cycle of EEPROM read to begin. The circuit generates a reset if V_S droops below 1.5V and then recovers up to the normal level.

USING THE XTR108 IN VOLTAGE OUTPUT MODE

The XTR108 can be used not only in 4-20mA current loops, but also as a low-power, single-supply, "smart" sensor-conditioning chip with voltage output. In this mode, the I_{RET} pin must be connected below ground ($-200mV < I_{RET} < -25mV$). This negative voltage is required to overcome the input offset voltage of the output current amplifier and prevent it from turning on and drawing excessive current. An application circuit that generates this negative voltage using the XTR108 clock output and a simple charge pump is shown in the application section.

The sub-regulator with an external MOSFET may or may not be used. If the circuit is powered externally, the supply voltage must be in the range of 5V ±0.5V.

CONTROL REGISTERS

Table V shows the registers that control the analog functions of the XTR108.

DESCRIPTION OF CONTROL REGISTERS

Address = 0: Control Register 1

If the RST bit is set to '1' in a write operation, all the registers in the XTR108 will be returned to their power-on reset condition. The RST bit will always read as a '0'. CSE, the checksum error bit, is read only and will be set to '1' if a checksum error has been detected. This bit is cleared by a reset operation or by detection of a valid checksum. The remaining bits are reserved and must be set to '0'.

Address = 3: Fault Status Register

This register is a read-only register. If the input voltage to the PGA exceeds the linear range of operation, the XTR108 will indicate this error condition (typically caused by a sensor fault) by setting the under-scale or over-scale error level depending on the state of the Alarm Configuration Register (Address = 7). Information on the nature of the fault may be read in digital form from this register, as shown in Table VI. The remaining bits will be set to '0'.

BIT	FAULT MODE
F0	Negative Input Exceeds Positive Limit.
F1	Negative Input Exceeds Negative Limit.
F2	Positive Input Exceeds Positive Limit.
F3	Positive Input Exceeds Negative Limit.

TABLE VI. Register 3, Fault Status Register.

Instruction	D7	D6	D5	D4	D3	D2	D1	D0	
Read/Write	R/$\overline{W}$	0	0	0	A3	A2	A1	A0	Read/Write Operation
EEPROM Mode	0	1	1	1	1	1	1	1	Assert $\overline{CS2}$ Ignore Serial Data/A

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0		
0	RST	CSE	0	0	0	0	0	0	Read/Write	Control Register 1
1	0	0	0	0	0	0	0	0	Reserved	
2	0	0	0	0	0	0	0	0	Reserved	
3	0	0	0	0	F3	F2	F1	F0	Read Only	Fault Status Register
4	0	0	0	0	0	0	0	RBD	Read/Write	Control Register 2
5	FD	US2	US1	US0	OS3	OS2	OS1	OS0	Read/Write	Over/Under-Scale Register
6	0	0	0	0	0	G2	G1	G0	Read/Write	PGA Gain
7	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read/Write	Alarm Config. Register
8	0	VP2	VP1	VP0	0	VN2	VN1	VN0	Read/Write	PGA Input Config. Register
9	0	IB2	IB1	IB0	0	IA2	IA1	IA0	Read/Write	I_{REF} Output Config. Register
10	FG7	FG6	FG5	FG4	FG3	FG2	FG1	FG0	Read/Write	Fine I_{REF} Adjust Register
11	CG7	CG6	CG5	CG4	CG3	CG2	CG1	CG0	Read/Write	Coarse I_{REF} Adjust Register
12	FZ7	FZ6	FZ5	FZ4	FZ3	FZ2	FZ1	FZ0	Read/Write	Fine Zero Adjust Register
13	CZ7	CZ6	CZ5	CZ4	CZ3	CZ2	CZ1	CZ0	Read/Write	Coarse Zero Adjust Register
14	L7	L6	L5	L4	L3	L2	L1	L0	Read/Write	Linearization Adjust Register
15	S7	S6	S5	S4	S3	S2	S1	S0	Read/Write	Checksum Register

TABLE V. Analog Control Registers.

Address = 4: Control Register 2

If the RBD bit is set to '1', the automatic read-back from the EEPROM will be disabled after a valid checksum byte is received in Register 15. This bit is read from the EEPROM during a read-back by the XTR108 and allows the user to program the XTR108 to read the EEPROM data once (instead of continuously), and then disables the automatic read-back function. The XTR108 will continuously read the EEPROM if RBD is set to '0'. The remaining bits in this register must be set to '0'.

Address = 5: Over- and Under-Scale Register

This register sets the magnitude of the over-scale current limit and the magnitude of the under-scale current limit. The threshold level, as shown in Table VII and VIII, is the normal analog (no error condition) output limit. If an input voltage to the PGA exceeds the linear operation range, the output will be programmed to either the over-scale error level or the under-scale error level. The over-scale error level is 10mA greater than the over-scale threshold level. The under-scale error level is 0.4mA less than the under-scale threshold level. The FD bit will disable the over-scale and under-scale limiting function as well as the PGA fault indication error levels.

Address = 6: PGA Gain Register

This register sets the gain of the programmable-gain amplifier. The unused bits must always be set to '0'. The gain step to register content is given in Table IX.

Address = 7: Alarm Configuration Register

This register configures whether the XTR108 will go over-scale or under-scale for various detected fault conditions at the input of the PGA. Table X defines each of the bits.

If a bit corresponding to the particular error is set to '1', the output will go over-scale when it occurs and if a bit corresponding to the particular error is set to '0', the output will go under-scale.

OS3	OS2	OS1	OS0	V_O OVER-SCALE THRESHOLD	I_O OVER-SCALE THRESHOLD R_{VI} = 6.34kΩ
0	0	0	0	2.625V	20.7mA
0	0	0	1	2.6875V	21.2mA
0	0	1	0	2.75V	21.7mA
0	0	1	1	2.8125V	22.2mA
0	1	0	0	2.875V	22.7mA
0	1	0	1	2.9375V	23.2mA
0	1	1	0	3.0V	23.7mA
0	1	1	1	3.0625V	24.2mA
1	0	0	0	3.125V	24.6mA
1	0	0	1	3.1875V	25.1mA
1	0	1	0	3.25V	25.6mA
1	0	1	1	3.3125V	26.1mA
1	1	0	0	3.375V	26.6mA
1	1	0	1	3.4375V	27.1mA
1	1	1	0	3.5V	27.6mA
1	1	1	1	3.5625V	28.1mA

TABLE VII. Register 5, Over-Scale Threshold.

US2	US1	US0	V_O UNDER-SCALE THRESHOLD	I_O UNDER-SCALE THRESHOLD R_{VI} = 6.34kΩ
0	0	0	450mV	3.55mA
0	0	1	425mV	3.35mA
0	1	0	400mV	3.15mA
0	1	1	375mV	2.96mA
1	0	0	350mV	2.76mA
1	0	1	325mV	2.56mA
1	1	0	300mV	2.37mA
1	1	1	275mV	2.17mA

TABLE VIII. Register 5, Under-Scale Threshold.

G2	G1	G0	PGA VOLTAGE GAIN	SIGNAL PATH TRANSCONDUCTANCE R_{VI} = 6.34kΩ
0	0	0	6.25V/V	49mA/V
0	0	1	12.5V/V	99mA/V
0	1	0	25V/V	197mA/V
0	1	1	50V/V	394mA/V
1	0	0	100V/V	789mA/V
1	0	1	200V/V	1577mA/V
1	1	0	400V/V	3155mA/V
1	1	1	Reserved	

TABLE IX. Register 6, PGA Gains.

BIT	AC	AC	AC	AC	AC	AC	AC	AC
#	7	6	5	4	3	2	1	0
V_{INN}	h	l	l	h	n	n	l	h
V_{INP}	l	h	l	h	l	h	n	n

NOTES: 'h' = input exceeds positive common-mode range, 'l' = input exceeds negative common-mode range, and 'n' = input pin is within the CM range.

TABLE X. Register 7, Alarm Configuration Register.

Address = 8: PGA Input Configuration Register

This register connects the inputs of the PGA to the various multiplexed input pins. Tables XI and XII show the relationship between register, contents, and PGA inputs.

VP2	VP1	VP0	PGA POSITIVE INPUT
0	0	0	PGA V_{IN+} Connected to V/I-0
0	0	1	PGA V_{IN+} Connected to V/I-1
0	1	0	PGA V_{IN+} Connected to V/I-2
0	1	1	PGA V_{IN+} Connected to V/I-3
1	0	0	PGA V_{IN+} Connected to V/I-4
1	0	1	PGA V_{IN+} Connected to V/I-5
1	1	0	Reserved
1	1	1	Reserved

TABLE XI. Register 8, PGA Positive Input Selection.

VN2	VN1	VN0	PGA NEGATIVE INPUT
0	0	0	PGA V_{IN-} Connected to V/I-0
0	0	1	PGA V_{IN-} Connected to V/I-1
0	1	0	PGA V_{IN-} Connected to V/I-2
0	1	1	PGA V_{IN-} Connected to V/I-3
1	0	0	PGA V_{IN-} Connected to V/I-4
1	0	1	PGA V_{IN-} Connected to V/I-5
1	1	0	Reserved
1	1	1	Reserved

TABLE XII. Register 8, PGA Negative Input Selection.

Address = 9: I_{REF} Output Configuration Register

This register connects the reference currents to the various multiplexed input pins. I_{REF} connection codes are given in Table XIII.

Address = 10: Fine I_{REF} Adjust Register

This register sets the code to the 8-bit Fine DAC that adjusts the magnitude of both reference currents. The DAC output value has a bipolar range (for each reference current) and can be calculated using the equations in Table III.

IA2	IA1	IA0	I_{REF} CONNECTION
0	0	0	$I_{REF}1$ Connected to V/I-0
0	0	1	$I_{REF}1$ Connected to V/I-1
0	1	0	$I_{REF}1$ Connected to V/I-2
0	1	1	$I_{REF}1$ Connected to V/I-3
1	0	0	$I_{REF}1$ Connected to V/I-4
1	0	1	$I_{REF}1$ Connected to V/I-5
1	1	0	Reserved
1	1	1	Reserved
IB2	**IB1**	**IB0**	**I_{REF} CONNECTION**
0	0	0	$I_{REF}2$ Connected to V/I-0
0	0	1	$I_{REF}2$ Connected to V/I-1
0	1	0	$I_{REF}2$ Connected to V/I-2
0	1	1	$I_{REF}2$ Connected to V/I-3
1	0	0	$I_{REF}2$ Connected to V/I-4
1	0	1	$I_{REF}2$ Connected to V/I-5
1	1	0	Reserved
1	1	1	Reserved

TABLE XIII. Register 9, I_{REF} Output Configuration.

Address = 11: Coarse I_{REF} Adjust Register

This register sets the code to the 8-bit coarse DAC that adjusts the magnitude of both reference currents. The nominal value for the reference current (both Coarse and Fine adjust set to '0') is $I_{PROGRAM}$ • 5. See Table III for formulas.

Address = 12: Fine Zero-Adjust Register

This register sets the code to the 8-bit Fine DAC that adjusts the magnitude of the zero output currents. Equations are given in Table II. Negative numbers are in Binary Two's Complement.

Address = 13: Coarse Zero-Adjust Register

This register sets the code to the 8-bit Coarse DAC that adjusts the magnitude of zero-output current. See Table II for equations. Negative numbers are given in Binary Two's Complement.

Address = 14: Linearization Adjust Register

This register sets the code to the 8-bit DAC that adjusts the magnitude of the linearization feedback current. Value is unipolar to 255.

Address = 15: Checksum Register

This register contains the checksum byte that is used to validate the data read from the EEPROM. If a write occurs to this register, and the checksum is invalid, an error condition will set (CSE = '1'). If the checksum is valid, the error condition will be cleared (CSE = '0').

If a checksum error is detected, the XTR108 will program itself to the lowest under-scale error level.

SERIAL INTERFACE

PROTOCOL

The XTR108 has an SPI-compatible serial interface. The data is transmitted MSB first in 8-bit bytes. The first byte is an instruction byte in which the first bit is a read/write flag ('0' = write, '1' = read), the lowest four bits are the register address and the remaining three bits are set to zero. The second, and all successive bytes, are data. During a write operation, the successive data bytes are written to successive registers within the XTR108. The address is automatically incremented at the completion of each byte. The SDIO line is always an input during a write operation. During a read operation, the SDIO line becomes an output during the second and successive bytes. As in the case of a write operation, the address is automatically incremented at the completion of each byte. Each communication transaction is terminated when $\overline{CS1}$ is de-asserted. The $\overline{CS2}$ line remains de-asserted during read and write operations.

The calibration controller also needs to be able to read from and write to the external EEPROM device. This is accomplished by sending a special instruction code (0x7F) to the XTR108. At the completion of this instruction byte, the XTR108 will assert the $\overline{CS2}$ line to select the EEPROM device and ignore all data on the SDIO line until $\overline{CS1}$ is de-asserted and reasserted. The $\overline{CS2}$ line will also be de-asserted when $\overline{CS1}$ is de-asserted. This allows the calibration controller to communicate with the EEPROM device directly. The calibration controller then has control over the timing required to write data to the EEPROM device.

In normal operation, the XTR108 reads data from the EEPROM device to retrieve calibration coefficients. This is accomplished by the read-back controller on the XTR108. The read-back controller is clocked by an on-chip oscillator and provides stimulus to the EEPROM device over the SCLK, SDIO, and $\overline{CS2}$ lines to perform the read operation, while simultaneously providing stimulus to the serial interface controller in the XTR108. The read-back controller defaults to being active when the XTR108 is powered on and will be continuously active unless disabled. (It will start a new read operation as soon as the previous operation is completed, see Figure 4.) A control bit (RBD) is provided to allow the XTR108 to read the EEPROM once and then stop.

The read-back controller will abort a read-back operation when the $\overline{CS1}$ line is asserted. The calibration controller must wait at least 40µs after setting the $\overline{CS1}$ line LOW before the first rising edge of SCLK occurs.

For an external controller to write directly to the XTR108 (sensor calibration operation) or load data into the EEPROM, it is necessary to interrupt the default read-back mode. For both of these modes, the SCLK direction must be reversed. See Figure 5 for the timing of this operation. First, the SCLK line must be pulled LOW for at least 20ns (t_{10}). Then $\overline{CS1}$ is set LOW. The XTR108 will set DIO to a tri-state within 20ns (t_{13}) and $\overline{CS2}$ HIGH within 50ns (t_{12}). After a delay of at least 40µs (t_{11}), the external system will start communication with a rising edge on SCLK.

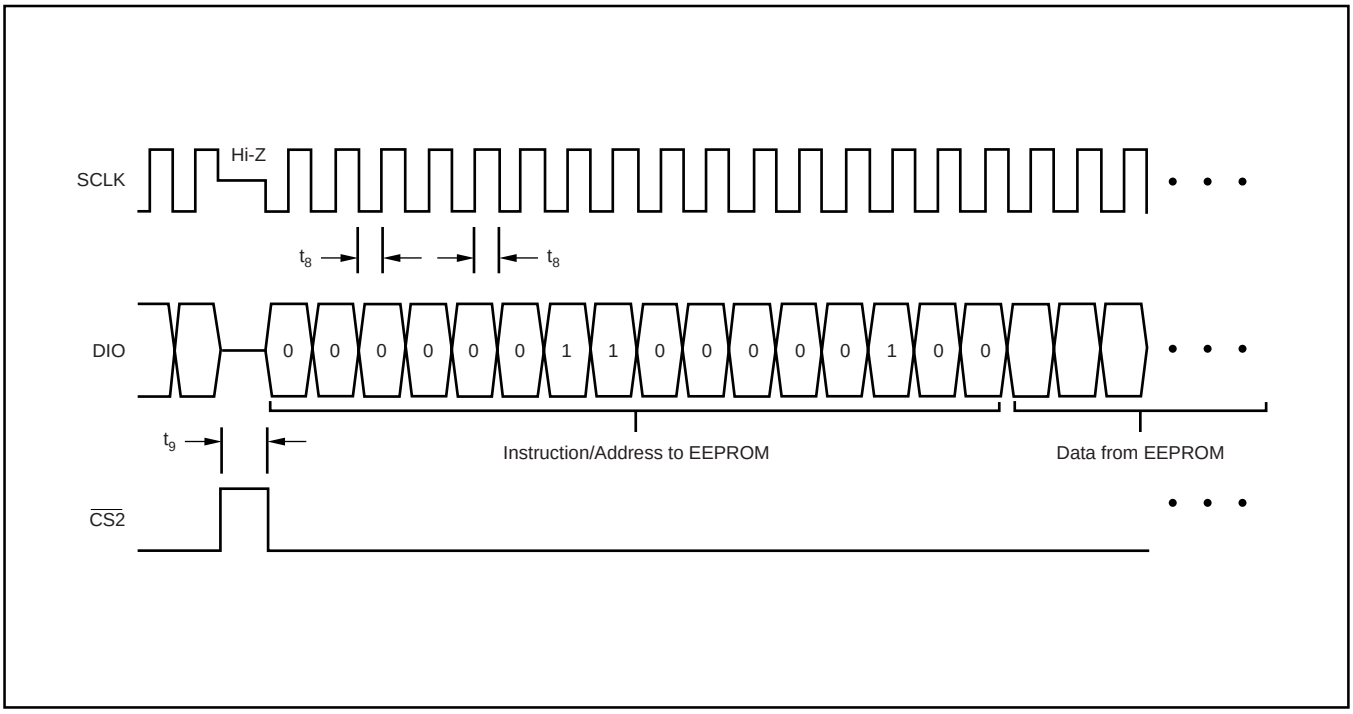


FIGURE 4. Timing Diagram for the XTR108 Continuous Readback Cycle. (See Table XIV for timing key.)

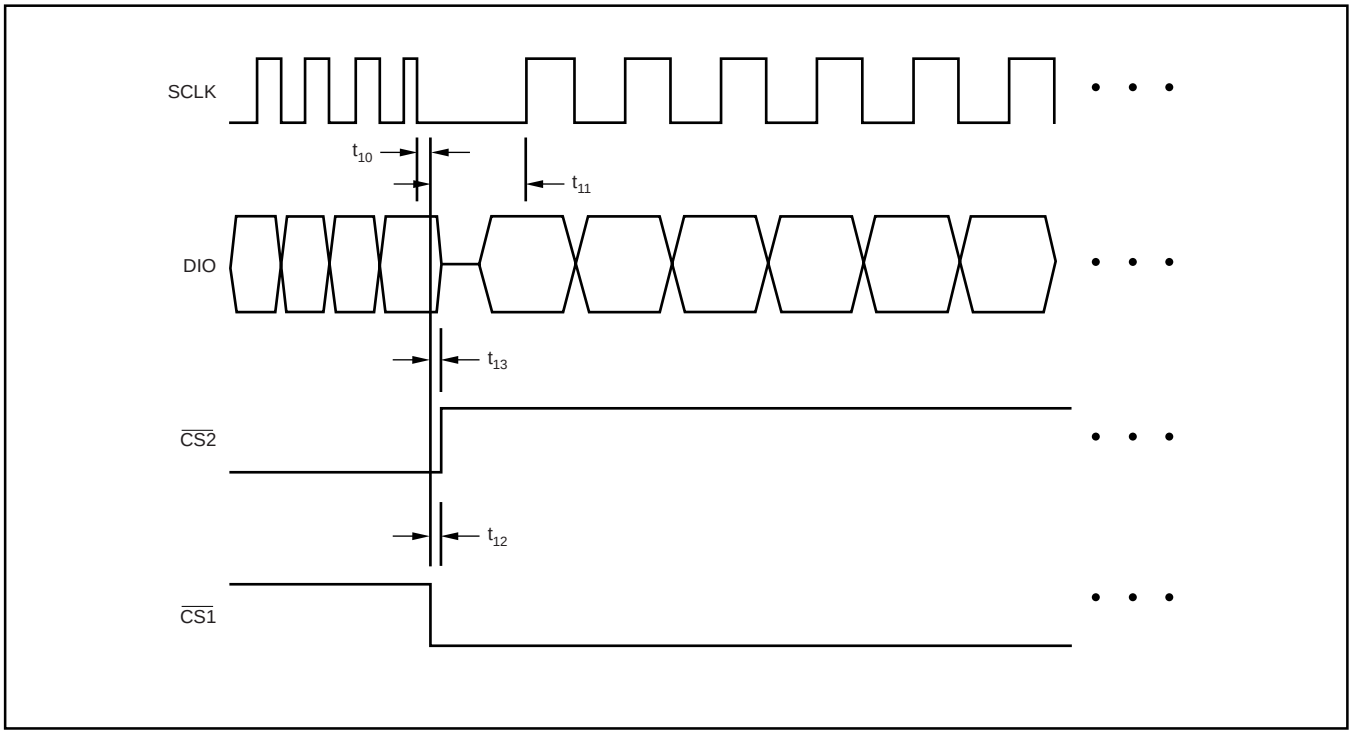


FIGURE 5. Interrupting an XTR108 EEPROM Readback Cycle. (See Table XIV for timing key.)

As long as $\overline{CS1}$ is held LOW, the external system can write to the EEPROM. See Figure 7 for this timing. Releasing $\overline{CS1}$ will allow the XTR108 to resume in the read-back mode.

For interactive calibration operations, the first command to the XTR108 should set bit 0, Register 4 (RBD). This will disable the read-back mode. It will be possible to write to the various registers and cycle $\overline{CS1}$. If RBD is not set, then as soon as $\overline{CS1}$ is released, the XTR108 will read the EEPROM contents which will overwrite the data just loaded. Figure 6 shows read and write timing.

To be compatible with SPI EEPROM devices, the XTR108 latches input data on the rising edge of SCLK. Output data transitions on the falling edge of SCLK. All serial interface transactions must be framed by $\overline{CS1}$. $\overline{CS1}$ must be asserted to start an operation, and it must be de-asserted to terminate an operation.

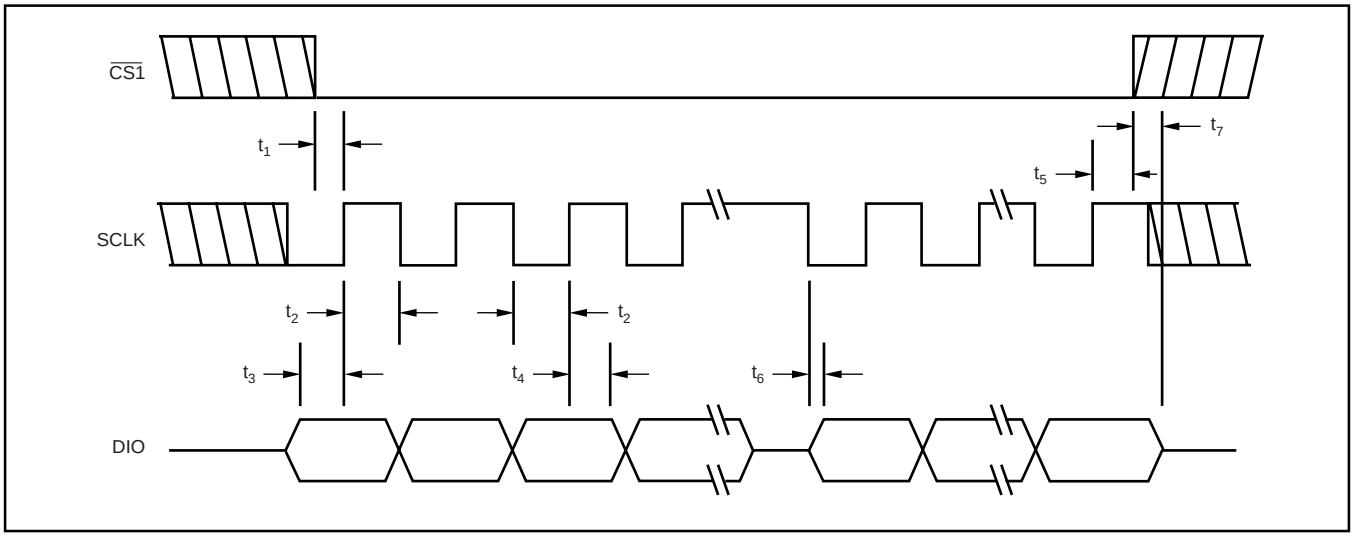


FIGURE 6. Timing Diagram for Writing to and Reading From the XTR108 with EEPROM Readback Disabled. (See Table XIV for timing key.)

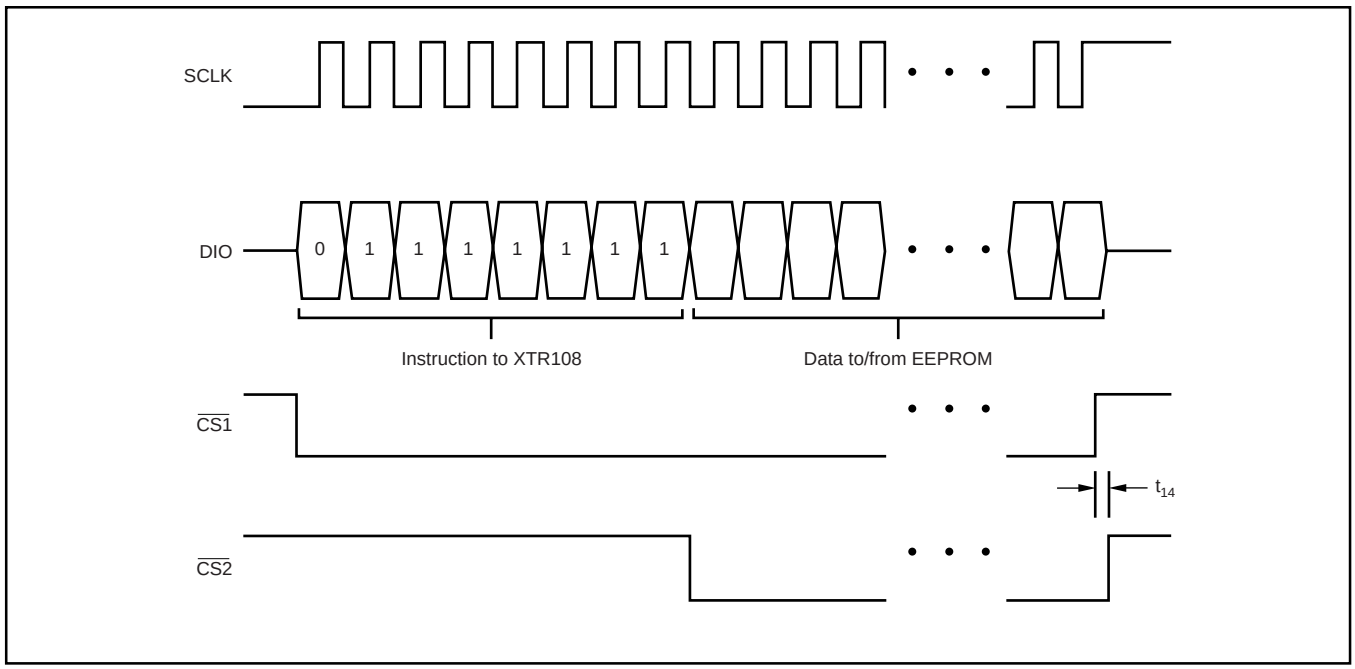


FIGURE 7. Writing to and Reading From the EEPROM Device From External Controller. (See Table XIV for timing key.)

SPEC	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	$\overline{CS1}$ LOW to SCLK Rising Setup Time	2.0			ns
t_2	SCLK Pulse Width HIGH and LOW	100			ns
t_3	DIO to SCLK Rising Setup Time	20			ns
t_4	DIO to SCLK Rising Hold Time	20			ns
t_5	$\overline{CS1}$ to Last SCLK Rising Hold Time	20			ns
t_6	SCLK Falling to DIO Driven Valid by XTR108	0		50	ns
t_7	$\overline{CS1}$ to DIO Tri-State	0		20	ns
t_8	SCLK Pulse Width During EEPROM Readback		5		us
t_9	$\overline{CS2}$ HIGH Between Successive EEPROM Readbacks		10		us
t_{10}	SCLK Driven LOW Before $\overline{CS1}$ LOW When Interrupting XTR108 Readback from EEPROM	20			ns
t_{11}	$\overline{CS1}$ LOW to SCLK Rising Setup Time When Interrupting XTR108 EEPROM Readback	40			us
t_{12}	$\overline{CS1}$ Falling to $\overline{CS2}$ HIGH	0		50	ns
t_{13}	$\overline{CS1}$ Falling to DIO Tri-State	0		20	ns
t_{14}	$\overline{CS1}$ Rising to $\overline{CS2}$ HIGH	0		20	ns
	XTR108 EEPROM Update Rate in Continuous Readback Mode		0.9		kHz

TABLE XIV. Timing Diagram Key.

EEPROM DATA STORAGE

The XTR108 automatically reads data from an SPI-compatible EEPROM device. The models 25C040 from MicroChip and the AT25010 from Atmel have been tested and are known to work. Equivalent devices with an SPI interface can be expected to work. The XTR108 will read data from addresses 4 through 15 of the EEPROM. The address in the EEPROM is the same as the address for the corresponding data in the XTR108. The XTR108 will not write data to the EEPROM. The external calibration controller is responsible for writing data to the EEPROM.

CHECKSUM FUNCTION

To validate the data from the EEPROM device, the XTR108 calculates a checksum on the incoming serial-data stream during each write operation. The value written to the EEPROM that will be transferred to register 15 during an EEPROM read operation must be such that the sum of the data in registers 4 through 15 totals 0xFF (255). The sum is calculated by performing an add/accumulate function on all of the data bytes of a read operation. An end-around carry is used during the add/accumulate operation. If a carry-out was generated in the previous add operation, it is used as a carry-in for the next add operation for the checksum operation. The following code shows how the value of register 15 could be calculated:

```
Sum = 0
FOR Index = 4 TO 14
  Sum = Sum + Data [Index]
  IF Sum > 255 THEN
    Sum = Sum – 255
NEXT Index
Data [15] = 255 – Sum
```

For a test or calibration operation, it may be necessary to write to a few select registers. This may be accomplished without writing to register 15. To accomplish this, write to the necessary registers and release $\overline{CS}1$. There is no need to update register 15.

If the command is to disable the automatic read-back function by setting the RDB bit in register 4, it is necessary to rewrite the entire register set data with a correct checksum value in register 15. The automatic read-back mode will be disabled upon successful checksum operation.

The checksum error flag is also cleared when the XTR108 is reset (i.e.: at power ON). Write operations that do not write to the checksum register will have no effect on the checksum error flag. By locating the checksum register after the last configuration register and including the checksum register in the EEPROM read operation, the data is validated by the checksum function.

EEPROM DATA SECURITY

Since the data in the EEPROM directly affects the analog output of the XTR108, the data in the EEPROM needs to be secure from accidental write operations. SPI EEPROM devices have a write-protect function on one of the pins. An additional connection to the calibration controller would be required if the write-protect pin is used to prevent accidental write operations. SPI EEPROM devices require a special write enable instruction to be executed to write data to the EEPROM. It is unlikely that this would accidentally be written to the EEPROM device and then be followed by a valid write operation. Further security can be obtained by using an SPI EEPROM device that has internal write-protect control bits. These bits are nonvolatile and must be cleared before write operations are allowed.

SURGE PROTECTION

Remote connections to current transmitters can sometimes be subjected to voltage surges. It is prudent to limit the maximum surge voltage applied to the XTR108 with various zener diodes and surge-clamping diodes specially designed for this purpose. Since the maximum voltage on the XTR108 loop is limited by the external MOSFET breakdown voltage, usually more than 200V, the requirement to the clamping devices are not very strict. For example, a 50V protection diode will assure proper transmitter operation at normal loop voltages without significant leakage yet provide an appropriate level of protection against voltage surges. In case of prolonged (seconds and longer) overvoltage, lower voltage clamps may be used to limit the power dissipation on the transmitter.

Most surge-protection zener diodes have a diode characteristic in the forward direction that will conduct excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge protection diode is used, a series diode or diode bridge should be used for protection against reversed connections.

REVERSE-VOLTAGE PROTECTION

The XTR108's low compliance rating (7.5V) permits the use of various voltage protection methods without compromising operating range. Figure 8 shows a diode bridge circuit which allows normal operation even when the voltage connection lines are reversed. The bridge causes a two diode drop (approximately 1.4V) loss in loop supply voltage. This results in a compliance voltage of approximately 9V—satisfactory for most applications. If 1.4V drop in loop supply is too much, a diode can be inserted in series with the loop supply voltage and the V+ pin. This protects against reverse output connection lines with only a 0.7V loss in loop supply voltage.

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency interference. RF energy can be rectified by the sensitive input circuitry of the XTR108 causing errors. This generally appears as an unstable output current that varies with the position of loop supply or input wiring.

If the RTD sensor is remotely located, the interference may enter at the input terminals. For integrated transmitter assemblies with short connection to the sensor, the interference more likely comes from the current loop connections.

Bypass capacitors on the input reduce or eliminate this input interference. Connect these bypass capacitors to the I_{RET} terminal, see Figure 9. Although the DC voltage at the I_{RET} terminal is not equal to 0V (at the loop supply, V_{PS}) this circuit point can be considered the transmitter's "ground." The 0.01µF capacitor connected between V_{LOOP} and I_O may help minimize output interference.

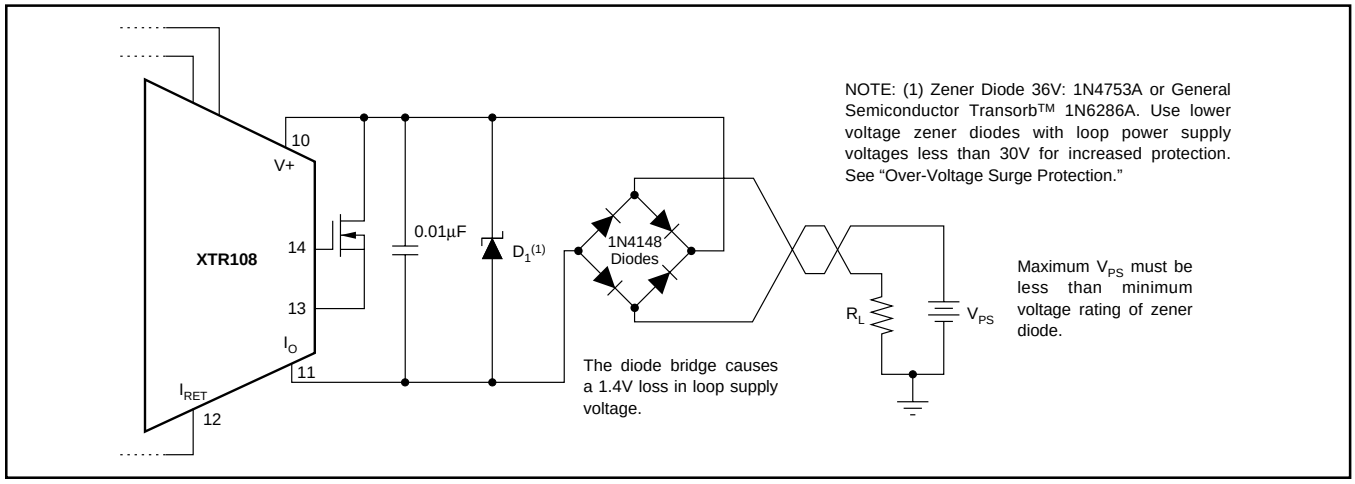


FIGURE 8. Reverse Voltage and Over-Voltage Protection.

RTD APPLICATION

The values to be entered into the DAC control registers are given by the formulas in Table XV.

EXCITATION CURRENT I_{REF}

Coarse DAC code

$$N_{11} = \text{round}\left(\frac{64 \bullet I_{REF} R_{SET}}{V_{REF}} - 320\right)$$

Fine DAC Code

$$N_{10} = \text{round}\left(\frac{1024 \bullet I_{REF} R_{SET}}{V_{REF}} - 5120 - 16 \bullet N_{11}\right)$$

ZERO OUTPUT I_{ZERO}

Coarse DAC Code

$$N_{13} = \text{round}\left(\frac{32 \bullet I_{ZERO} R_{VI}}{5 \bullet V_{REF}} - 140\right)$$

Fine DAC Code

$$N_{12} = \text{round}\left(\frac{512 \bullet I_{ZERO} R_{VI}}{5 \bullet V_{REF}} - 2240 - 16 \bullet N_{13}\right)$$

LINEARIZATION COEFFICIENT G_{LIN}

Lin DAC Code

$$N_{14} = \text{round}\left(16 \bullet G_{LIN} R_{LIN}\right)$$

TABLE XV. Equations for DAC Code Calculation.

This procedure allows calculation of the parameters needed to calculate the DAC codes for an RTD sensors application.

Standard RTD Polynomials:

$$R_t = R_O\left[1 + At + Bt^2 + C(t - 100°C)t^3\right] \text{ for } -200°C < t < 0°C$$

$$R_t = R_O\left[1 + At + Bt^2\right] \text{ for } 0°C < t < 850°C$$

$A = 3.9083e-3$

$B = -5.775e-7$

$C = -4.183e-12$

R_O – base RTD value at 0°C (100Ω or 1kΩ)

TABLE XVI. Standard RTD Descriptive Equations.

1) For a chosen temperature range, using an industry-standard polynomial set as shown in Table XVI, calculate RTD values at min, max, and the middle temperatures:

$$\left(R_{MIN}, R_{MAX}, \text{ and } R_{MID}\right)$$

2) Calculate a relative nonlinearity B_V using the RTD values from above:

$$B_V = \frac{R_{MID} - \frac{R_{MAX} + R_{MIN}}{2}}{R_{MAX} - R_{MIN}}$$

3) Pick an external zero resistor, R_Z closest to R_{MIN}. Selecting R_Z greater than R_{MIN} will cause a voltage offset that must be corrected by the PGA zero adjustment.

4) Calculate the linearization coefficient::

$$G_{LIN} = \frac{2B_V}{\left(0.5 + B_V\right) R_{MAX} - \left(0.5 - B_V\right) R_{MIN} - 2B_V R_Z}$$

If the value of G_{LIN} is larger than $G_{LIN\ MAX}$ = (16/R_{LIN}) the external resistor R_{LIN} has to be changed. If G_{LIN} is significantly smaller (> 10 times) than $G_{LIN\ MAX}$, the R_{LIN} value should be increased to minimize the DAC quantization errors. For 100Ω RTD sensors the required linearization coefficients are in the range from 0.3 to 0.6 mA/V (1/kΩ) for all measurement ranges. Therefore an external R_{LIN} value of 15.8kΩ is good setting the full-scale $G_{LIN\ MAX}$ ~ = 1mA/V. For 1kΩ RTD's the R_{LIN} should be increased proportionally.

5) Choose the output zero and full-scale level values, for instance: $I_{OUT_{MIN}}$ = 4mA, $I_{OUT_{MAX}}$ = 20mA.

6) Choose PGA gain from the available list and calculate the initial excitation current using:

$$I_{REF_{1,2}} = \frac{\left(I_{OUT_{MAX}} - I_{OUT_{MIN}}\right) \bullet \left(1 - G_{LIN}\left(R_{MAX} - R_Z\right)\right) \bullet R_{VI}}{50 \bullet A_{PGA} \bullet \left(R_{MAX} - R_{MIN}\right)}$$

Important: the PGA gain value should be chosen such that the I_{REF} value is within ±35% of $5V_{REF}/R_{SET}$ to allow room for calibration adjustments without having to go to another span step.

7) The required DAC zero offset current value can be calculated by:

$$I_{ZERO} = I_{OUT_{MIN}} - \frac{50 \bullet A_{PGA} I_{REF}\left(R_{MIN} - R_Z\right)}{R_{VI}}$$

Example:
Measurement Range: T_{MIN} = –20°C, T_{MAX} = 50°C; 100Ω RTD.

1) R_{MIN} = 92.16Ω, R_{MAX} = 119.40Ω, R_{MID} = 105.85Ω;
2) Sensor relative nonlinearity: B_V = 0.0026;
3) Choosing R_Z = 90.9Ω (closest to R_{MIN} 2% value);
4) Linearization coefficient: G_{LIN} = 0.3804mA/V;
5) 4-20mA output span;
6) PGA voltage gain A_{PGA} = 200, sensor excitation current $I_{REF1,2}$ = 368.39mA;
7) Zero offset DAC: I_{ZERO} = 3.268mA

CALIBRATION PROCEDURE FOR RTD SENSORS

Step 1 Initial parameters calculation.

- Using the procedure above, compute I_{REF}, A_{PGA}, I_{ZERO}, and G_{LIN} based on T_{MIN}, T_{MAX}, and nominal values of R_Z, R_{SET}, and R_{VI}. Use the equation in Table XV to calculate the DAC register values.
- Configure the input MUX, write PGA gain, reference, and offset DAC registers of the XTR108 with calculated settings. Note: write G_{LIN} = 0 (no linearization) to XTR108 at this step;

Step 2 Measurement.

- Set RTD resistor value (or oven temperature) to minimum scale, measure output signal I_{MEAS1};
- Set RTD resistor value (or oven temperature) to maximum scale, measure output signal I_{MEAS2};

Step 3.

- Calculate corrections using the following equations:

$$I_{REF_A} = \frac{\left(I_{MEAS2} - I_{MEAS1}\right) R_{VI}}{50 A_{PGA}\left(R_{MAX} - R_{MIN}\right)}$$

$$R_{Z_A} = R_{MIN} + \frac{\left(I_{ZERO} - I_{MEAS1}\right) R_{VI}}{50 A_{PGA} I_{REFA}}$$

$$G_{LINA} = \frac{2B_V}{\left(0.5 + B_V\right)R_{MAX} - \left(0.5 - B_V\right)R_{MIN} - 2B_V R_{ZA}}$$

$$I_{REF_B} = \frac{\left(I_{OUT_{MAX}} - I_{OUT_{MIN}}\right) \bullet \left(1 - G_{LIN_A}\left(R_{MAX} - R_{Z_A}\right)\right) \bullet R_{VI}}{50 \bullet A_{PGA} \bullet \left(R_{MAX} - R_{MIN}\right)}$$

$$\Delta I_{REF} = \left(I_{REF} - I_{REF_A}\right) + \left(I_{REF} - I_{REF_B}\right)$$

$$\text{Adjusted } I_{REF} \text{ fine DAC Code}: N_{10_A} = N_{10} + \text{round}\left(\frac{1024 \bullet \Delta I_{REF} R_{SET}}{V_{REF}}\right)$$

$$\Delta I_{ZERO} = I_{OUT_{MIN}} - I_{ZERO} - \frac{50 \bullet A_{PGA} I_{REF_B}\left(R_{MIN} - R_{Z_A}\right)}{R_{VI}}$$

$$\text{Adjusted } I_{ZERO} \text{ fine DAC Code}: N_{12_A} = N_{12} + \text{round}\left(\frac{512 \bullet \Delta I_{ZERO} R_{VI}}{5 \bullet V_{REF}}\right)$$

This takes into account resistor value deviations, all offsets and gain errors of the coarse DACs and PGA. If the adjusted abs(N_{12A}) > 128 or abs(N_{10A}) > 128, adjust the coarse DAC first, then recalculate the fine DAC value;

- Update all the DAC register value, including linearization DAC.

Step 4 (optional).

Measure output signal I_{MEAS3} with maximum RTD value still connected to the input from step 2;

Step 5 (optional).

Compute G_{LIN} correction and update LinDAC register;

Step 6 (optional).

Make verification measurements at min- and max-input signal; If linearity check is needed: make a measurement at mid-scale; write EEPROM data.

Step 7.

Set the desired over-scale, under-scale signal limits and sensor burnout indication configuration. Verify and adjust the over-scale and under-scale levels by applying the positive and negative overdriving differential signals to the PGA inputs.

SAMPLE ERROR ANALYSIS

Table XVII shows a detailed computation of the error accumulation. The sample error budget is based on a typical RTD circuit (Pt100, 200°C measurement span). Note that these calculations are based on typical characteristics where no maximum or minimum characteristic is available. The assumption is made that all errors are positive and additive. As the various error sources are independent, a closer approximation to nominal performance might be to accumulate the errors with a root-sum-square calculation.

SAMPLE ERROR CALCULATION

RTD value at 4mA Output ($R_{RTD\ MIN}$) 100Ω: RTD Measurement Range 200°C; Ambient Temperature Range (ΔT_A) 20°C; Supply Voltage Change (ΔV_+) 5V; Common-Mode Voltage Change (ΔCM) 0.1V.
Chosen XTR108 parameters: PGIA gain = 50; I_{REF} = 518.9µA; Full-scale V_{IN} = 40mW. Register 06 = 0_H03; Register 11 = 0_H11; Register 13 = 0_HFC; Register 14 = 0_H70.

ERROR SOURCE	ERROR EQUATION	SAMPLE ERROR CALCULATION	CALIBRATED ERROR (ppm of Full Scale)
INPUT			
Input Offset Voltage	Note (1)		0
vs Common Mode	$CMRR \cdot \Delta CM/(V_{IN\ MAX}) \cdot 10^6$	5µV/V • 0.1V/0.04V • 10^6	12.5
Input Bias Current	Note (1)		0
Input Offset Current	Note (1)		0
		Total Input Error:	**12.5**
EXCITATION			
Current Reference Accuracy	Note (1)		0
vs Common Mode	$\Delta CM/R_{OUT} \cdot R_{RTD\ MIN}/(V_{IN\ MAX}) \cdot 10^6$	0.1V/100MΩ • 100Ω/40mV	2.5
Current Reference Matching	Note (1)		
DAC Resolution and Linearity	$1LSB_{FINE} \cdot R_{RTD\ MIN}/(V_{IN\ MAX}) \cdot 10^6$	96nA • 100Ω/40mV • 10^6	240
		Total Excitation Error:	**242.5**
GAIN			
Span	Note (1)		0
Nonlinearity	Nonlinearity (%)/100% • 10^6	0.01%/100% • 10^6	100
		Total Gain Error:	**100**
OUTPUT			
Zero Output	Note (1)		0
vs Supply	$(I_{ZERO}$ vs $V_+) \cdot \Delta V_+/16mA \cdot 10^6$	Note (2)	6
DAC Resolution and Linearity	$2LSB_{FINE}/16mA \cdot 10^6$	2 • 1.8µA/16mA • 10^6	225
		Total Output Error:	**231**
DRIFT (ΔT_A = 20°C)			
Input Offset Voltage	Drift • $\Delta T_A/(V_{IN\ MAX}) \cdot 10^6$	0.02µV/°C • 20°C/40mV • 106	10
Current Reference Accuracy	Drift • ΔT_A	35ppm • 20°C	700
Current Reference Matching	Drift • $\Delta T_A \cdot I_{REF} \cdot R_{RTD\ MIN}/(V_{IN\ MAX})$	15ppm • 20°C • 518.9µA • 100/40mV	390
Span	Drift • ΔT_A	30ppm • 20°C	600
Zero Output	Drift • ΔT_A	Note (1)	250
		Total Drift Error:	**1950**
NOISE (0.1Hz to 10Hz, Typ)			
Input Offset Voltage	$V_N/(V_{IN\ MAX}) \cdot 10^6$	6µV/40mV • 10^6	150
Current Reference	I_{REF} Noise • $R_{RTD\ MIN}/(V_{IN\ MAX}) \cdot 10^6$	0.015µA • 100Ω/40mV • 10^6	37.5
Zero Output	I_{ZERO} Noise/16mA • 10^6	1.1µA/16mA • 10^6	68.5
		Total Noise Error:	**256**
		TOTAL ERROR:	**2792 (1997)[3]** 0.28% (0.20%)[3]

NOTES: (1) Does not contribute to the output error due to calibration. (2) All errors are referred to input unless otherwise stated. (3) Calculated as root-sum–square.

TABLE XVII. Sample Error Budget Calculation.

APPLICATIONS

RTD CONNECTION METHODS

Two-Wire Connection

The simplest circuit that can be used to connect an RTD to the XTR108 is the two-wire connection shown in Figure 9. If the RTD is separated from the XTR108 by any distance the resistance of the lead wires can cause significant error in the reading. This wire resistance is noted as R_{LINE1} and R_{LINE2}. If the RF filter is not required, then the PGA inputs could be taken from the same pins as are used for the current sources.

Three-Wire Connection

It is possible to minimize the errors caused by the lead-wire resistance by connecting the RTD, see Figure 10. Operating under the assumption that the wire connecting pin 1 to the XTR108 is the same length as the wire at pin 2, and with the current through the RTD identical to the current through R_Z any error voltage caused by the lead-wire is the same on both sides. This appears as a common-mode voltage and is subtracted by the PGA.

The circuit in Figure 10 also shows a scheme where one board can be optimized for a wide range of temperatures. Consider a range of applications where there are up to five different minimum temperatures. Select R_{Z1} through R_{Z5} to be optimum for each of the minimum temperatures. The configuration codes in the EEPROM can be set to select that resistor for that unique situation.

Four-Wire Connection

For those applications where the resistance of the lead-wires is not equal, it may be an advantage to add a precision op amp to a four-wire connection, see Figure 11. The voltage offset and drift are error terms that degrade the operation of the system. This circuit does not suffer any loss of accuracy for the resistance of the RTD lead-wires.

BRIDGE SENSOR CONNECTIONS

Fixed Voltage Excitation

There exists a class of sensors that are best supplied with a voltage source excitation such as the bridge sensor shown in Figure 12. The excitation voltage here is given by:

$$V_{EX} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

Uni-Directional Linearity Control

The circuit in Figure 13 shows a bridge sensor with an excitation voltage that is adjusted to linearize the response using the same algorithm as the RTD linearization.

$$V_{EX} = 2 \bullet I_{REF}\ R_I$$

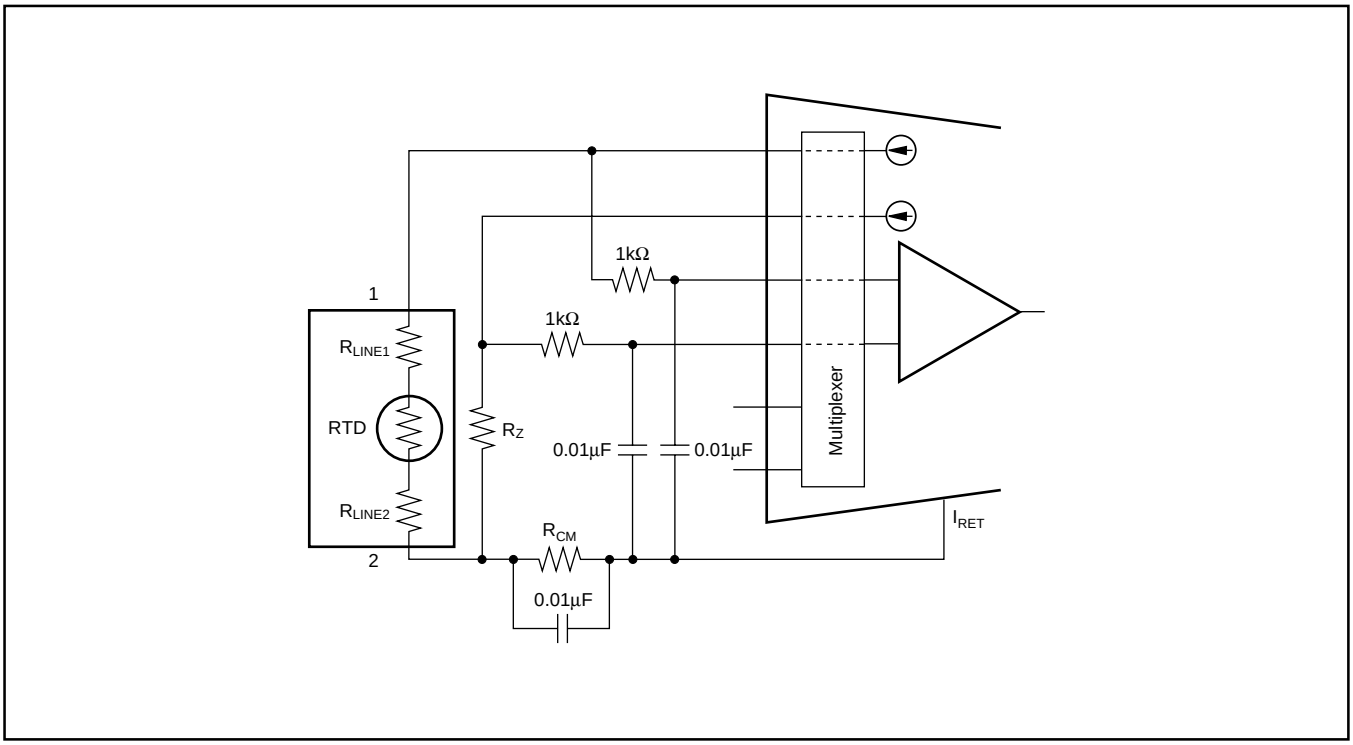


FIGURE 9. Two-Wire RTD Connection with RF Filter at Input Terminals.

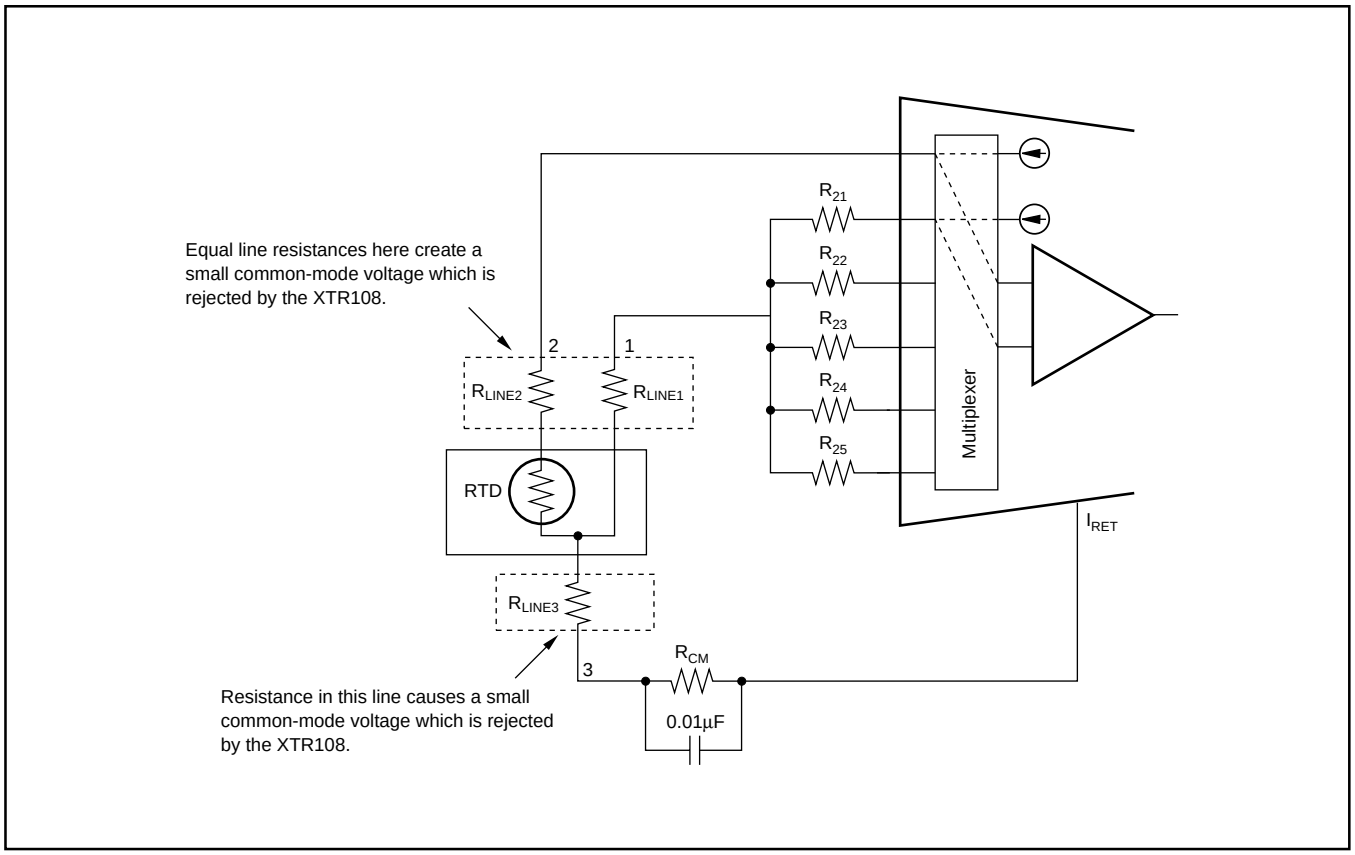


FIGURE 10. Three-Wire RTD Connection with Multiple Minimum Temperature Capabilities.

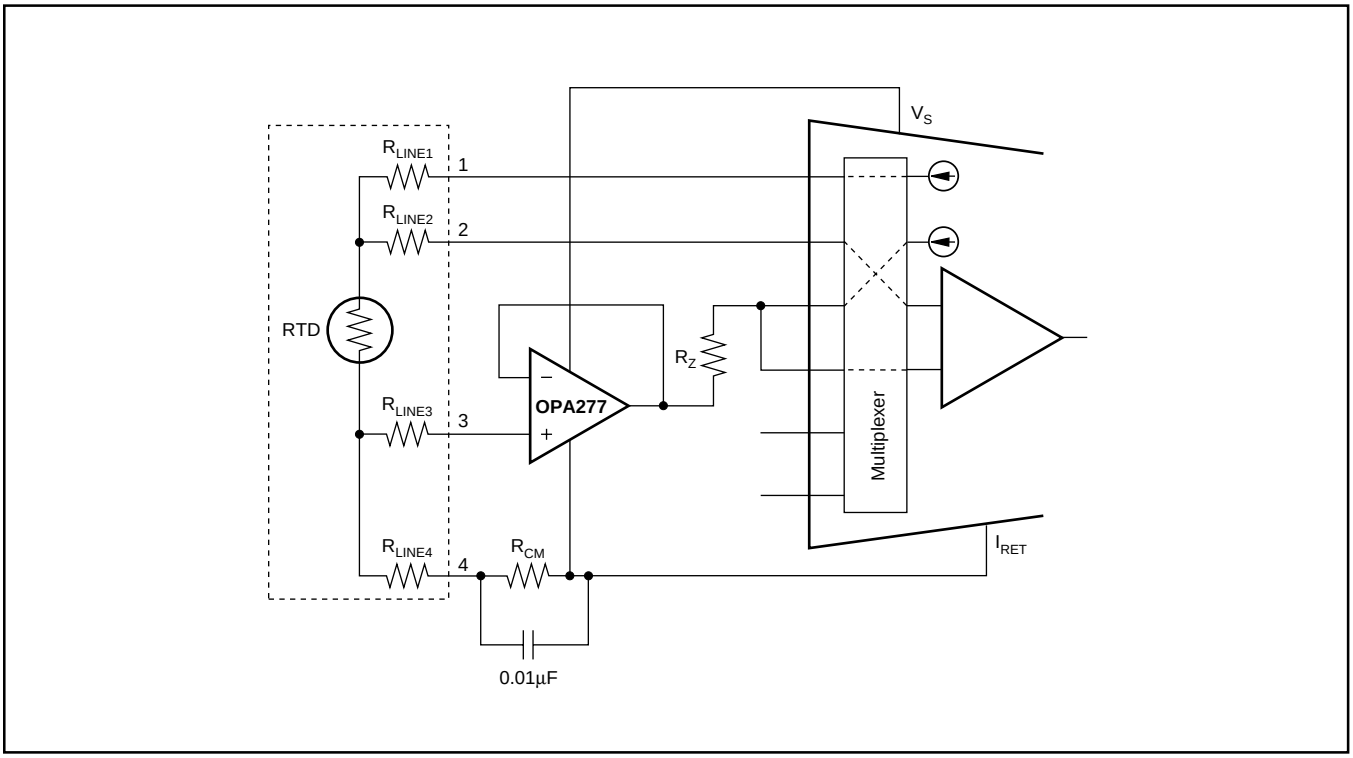


FIGURE 11. Four-Wire RTD Connection.

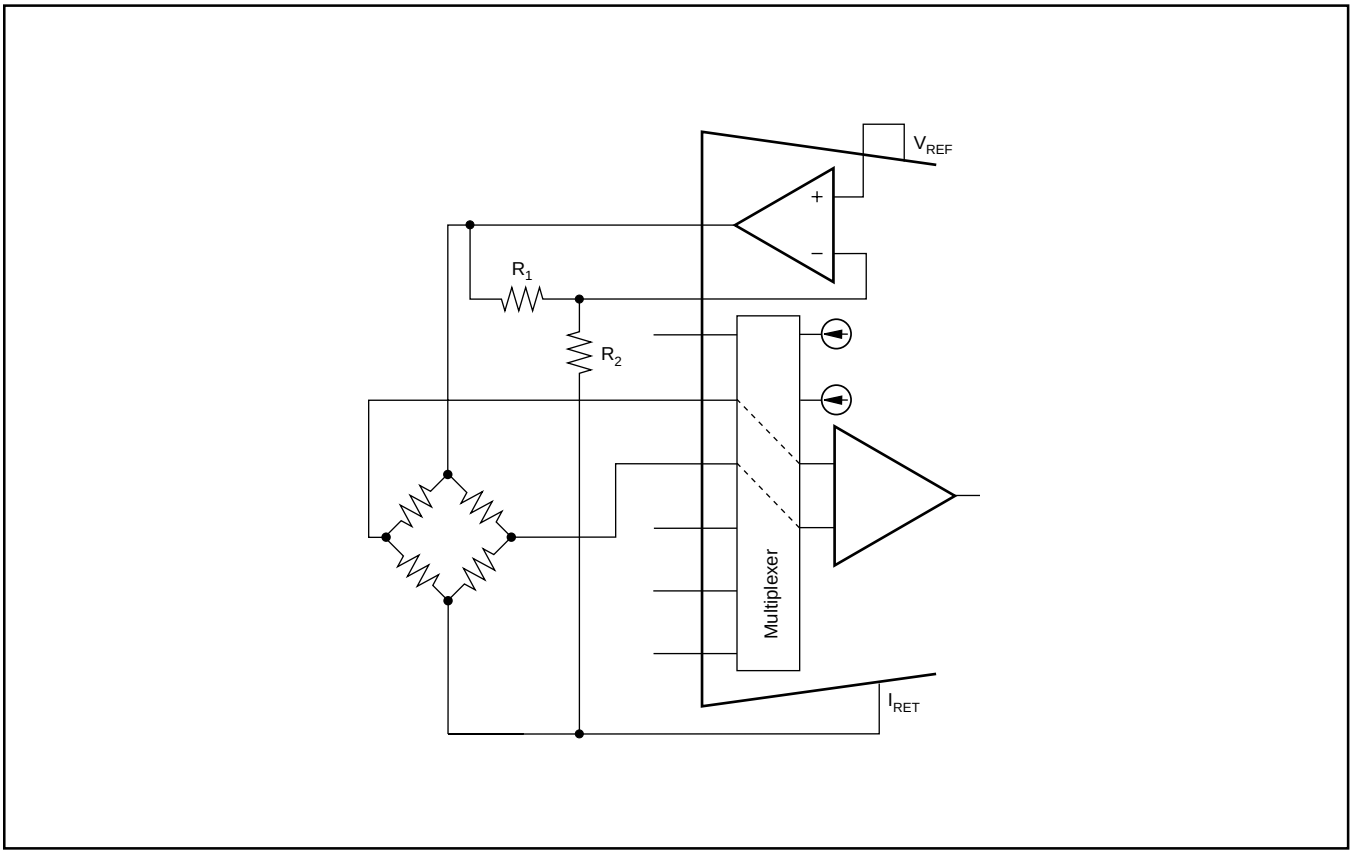


FIGURE 12. Voltage Excited Bridge with Excitation Derived from V_{REF}.

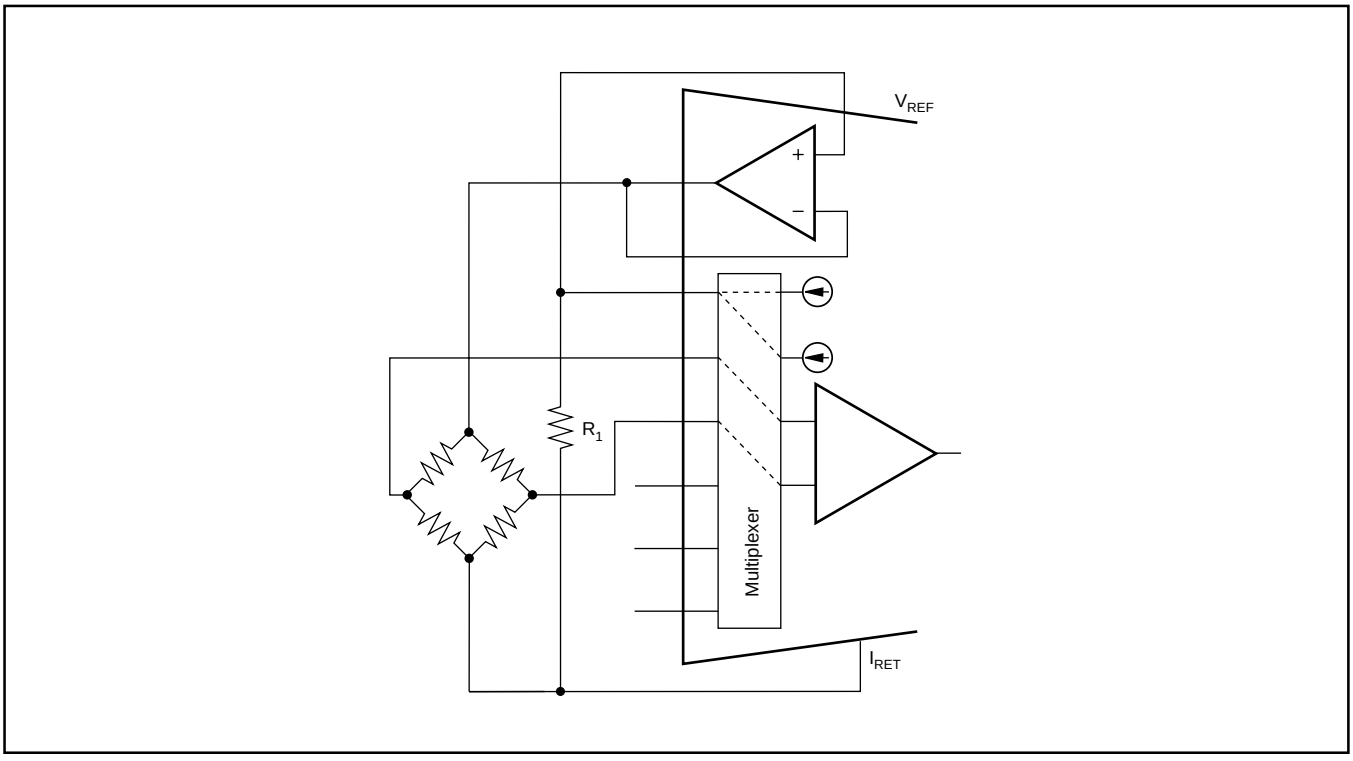


FIGURE 13. Voltage Excited Bridge with Uni-Directional Linearity by Control.

VOLTAGE OUTPUT MODE USING SIMPLE CURRENT PUMP

In order for the voltage output mode of the XTR108 to operate properly, a negative voltage needs to be applied to the I_{RET} pin ($-200mV < I_{RET} < -25mV$). For systems without a negative supply a charge pump is an easy way to generate this voltage. Figure 14 shows a simple and inexpensive way to build this charge pump using two resistors, two capacitors, and two diodes (in an SOT package). The charge pump uses the clock signal from the XTR108 SCLK pin to operate; consequently, the XTR108 must be in continuous EEPROM read mode (register 4, bit 0). Figure 15 shows the typical output of this circuit (–50mV dc).

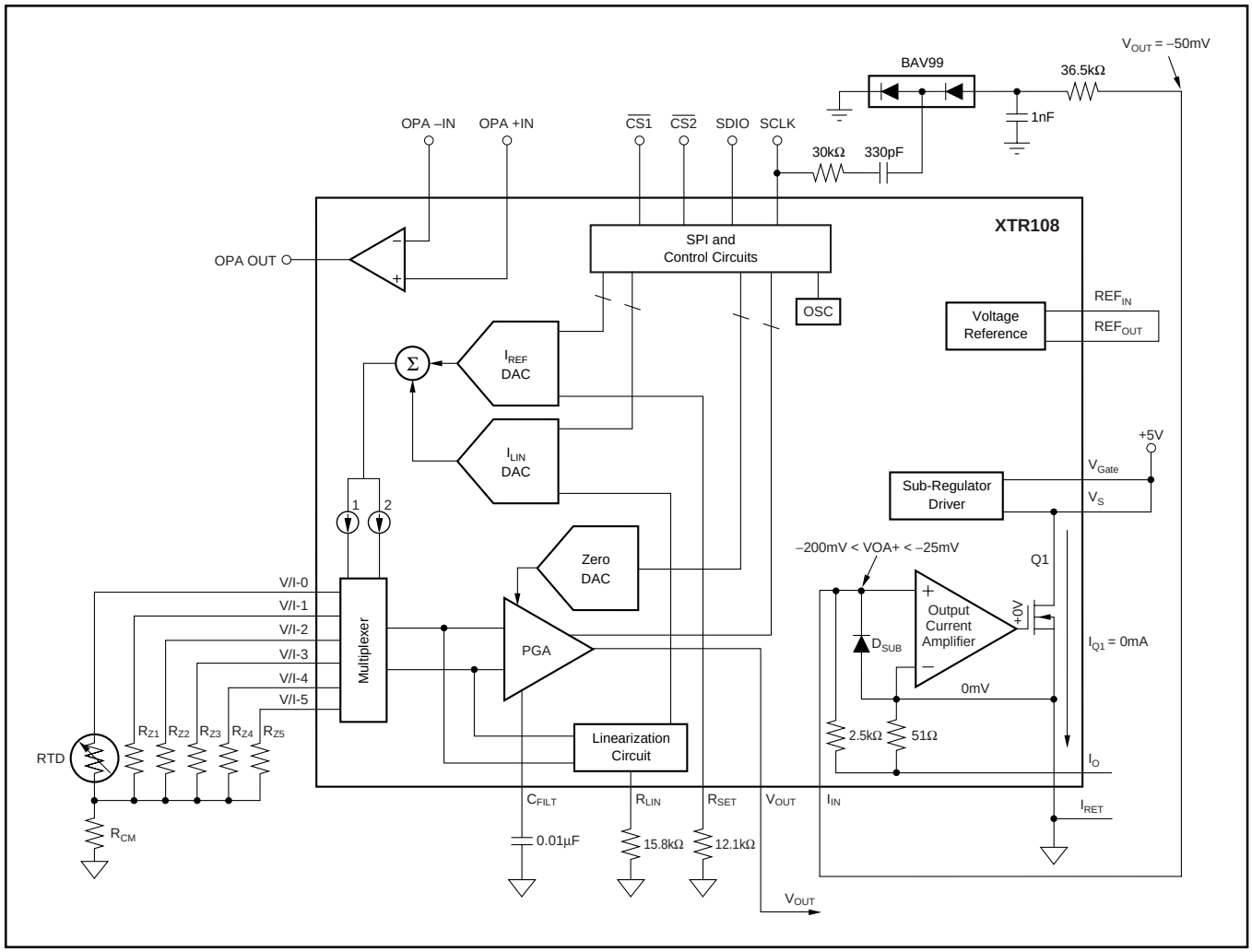


FIGURE 14. Voltage Output Mode Using Simple Current Pump.

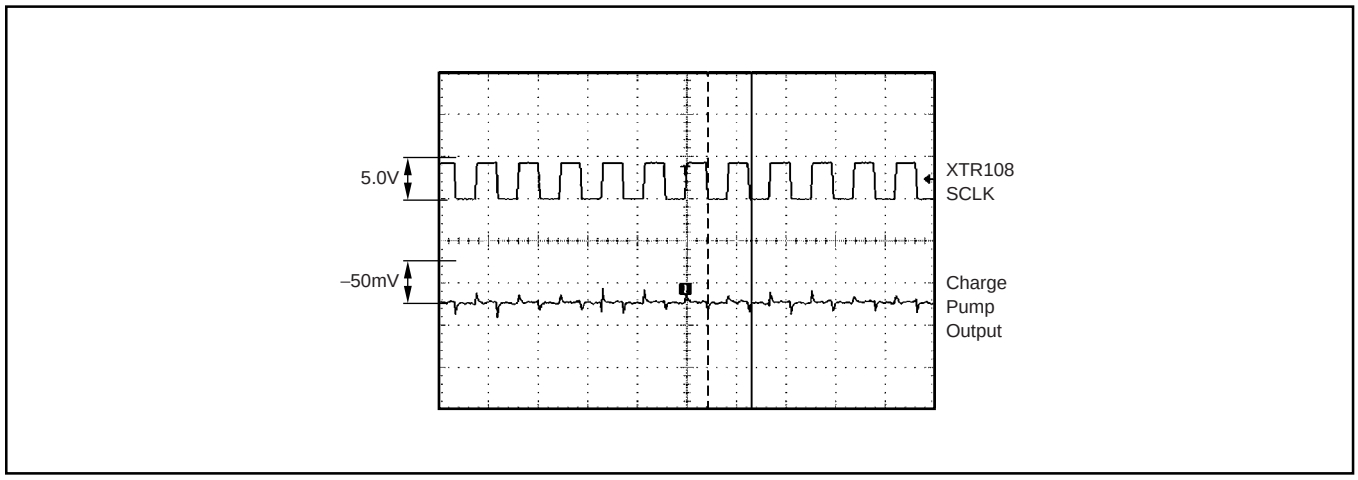


FIGURE 15. Output Waveform of Simple Current Pump.

COMMUNICATIONS WITH THE XTR108 USING A MICROCONTROLLER

When communicating with the XTR108, special care must be taken to avoid getting a false clock. When $\overline{CS1}$ is driven low, the false clock is generated because the microcontroller clock pin is in high-impedance state, which forces the clock pin to a logic high. Immediately after $\overline{CS1}$ is driven low, the microcontroller drives the clock pin low. This sequence creates a glitch that the XTR interprets as a clock; see Figure 16. This condition can be avoided by driving the SCLK pin low just prior to applying $\overline{CS1}$ low; see Figure 17. A series resistance should be placed between the microcontroller and the XTR108 because driving SCLK low before $\overline{CS1}$ can create a bus contention; see Figure 18.

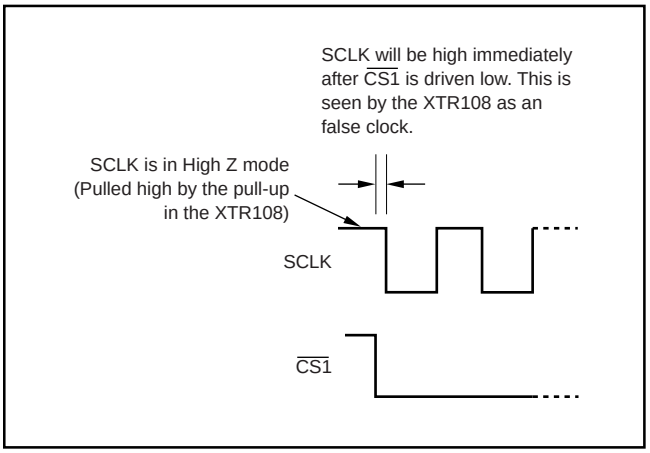


FIGURE 16. False Clock.

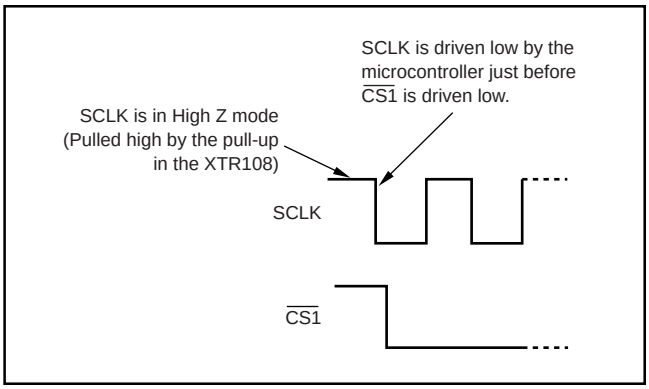


FIGURE 17. Proper Method to Drive the XTR108 to Avoid False Clock.

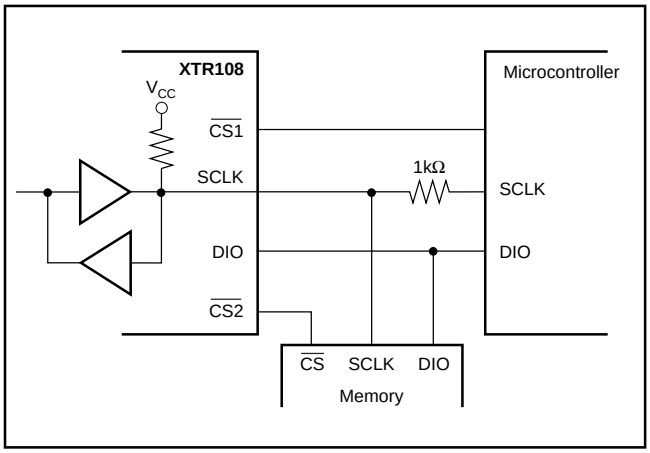


FIGURE 18. Resistor Protects XTR108 and Microcontroller During Bus Contention.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
XTR108EA	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
XTR108EA/2K5	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
XTR108EA/2K5G4	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
XTR108EAG4	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

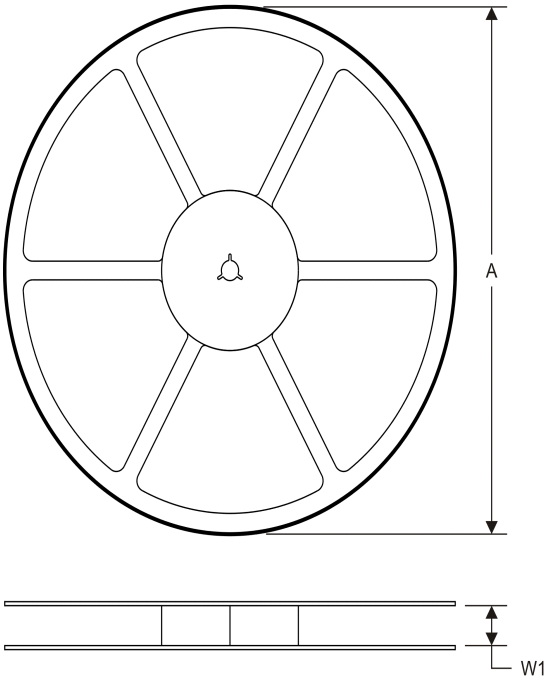
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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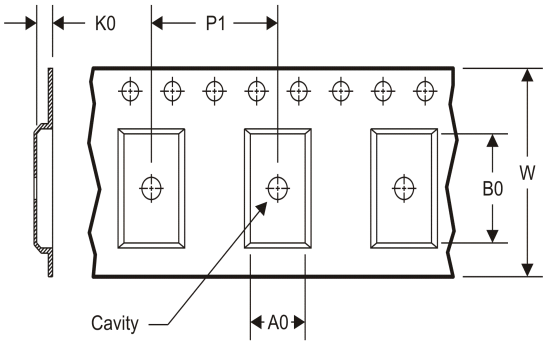
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



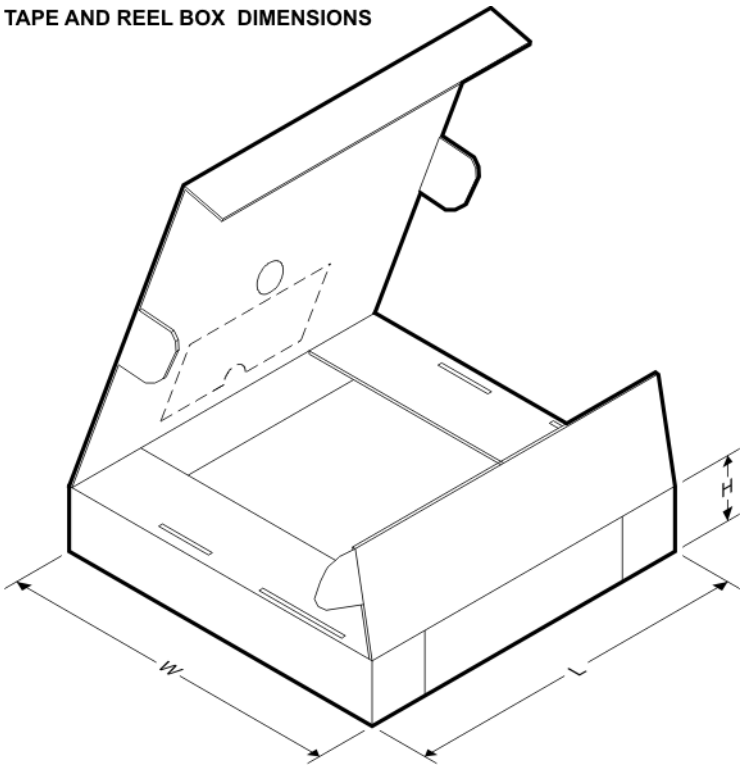
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR108EA/2K5	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

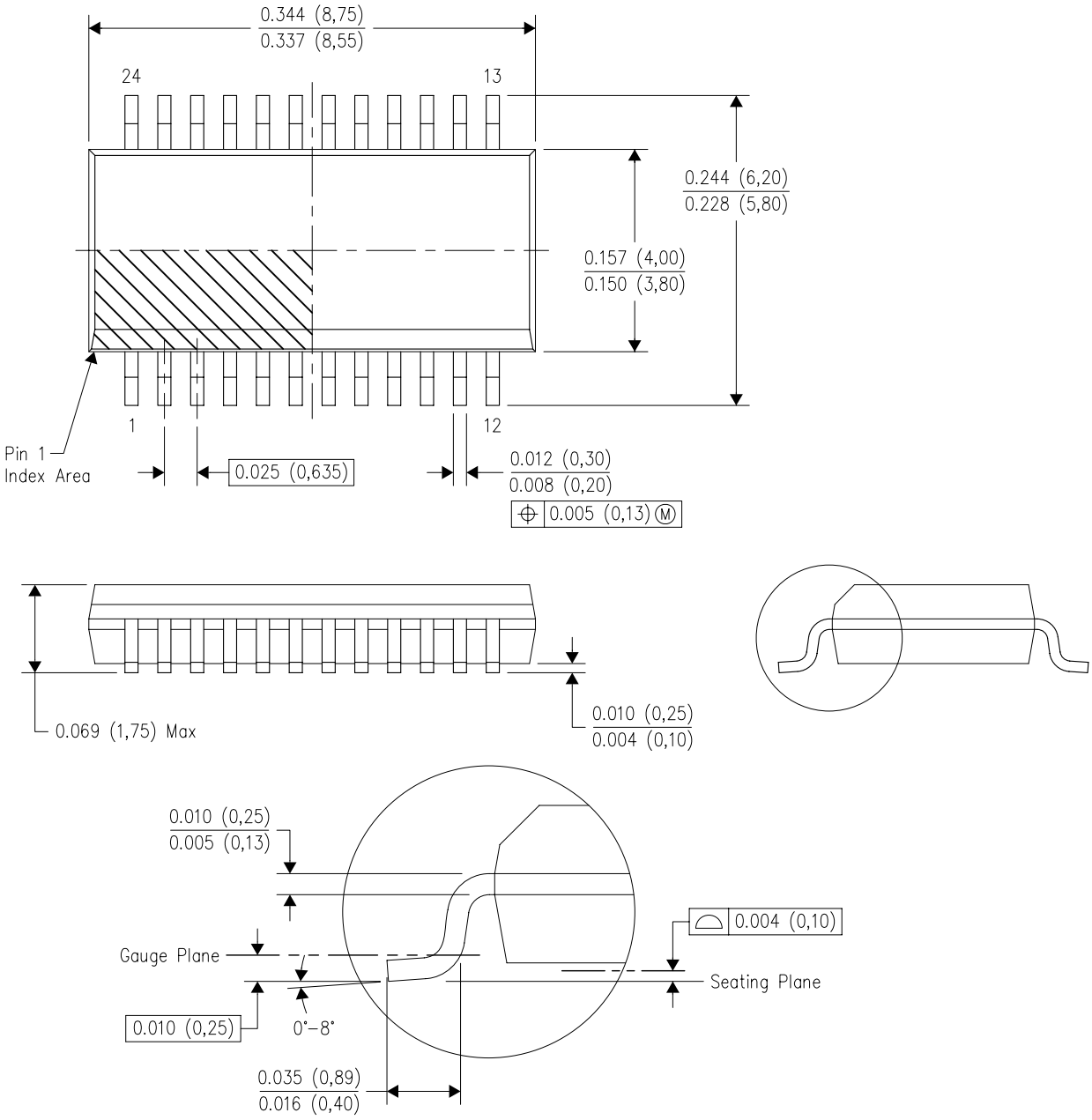
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

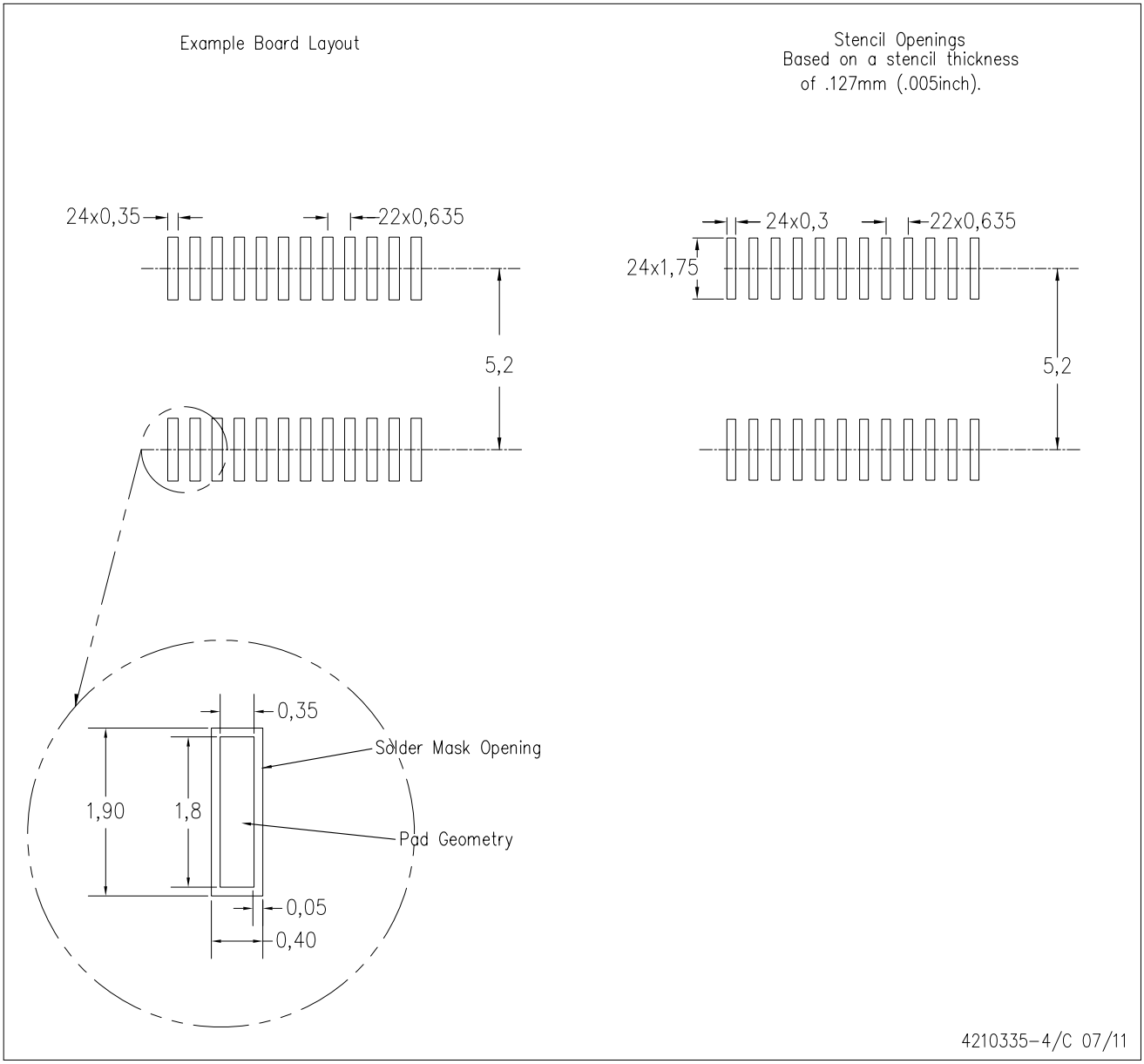
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR108EA/2K5	SSOP	DBQ	24	2500	367.0	367.0	38.0

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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