

# **NMC6551 1024-Bit (256 × 4) Static RAM**

## **General Description**

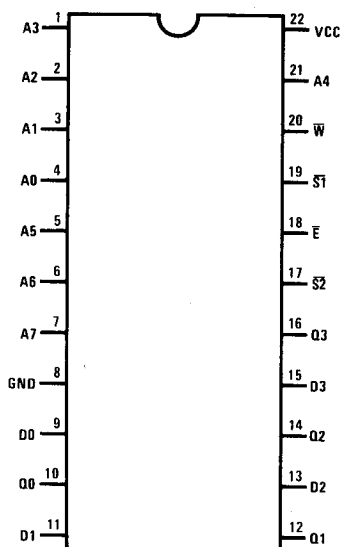
The NMC6551 is a static CMOS random access read/write memory organized as 256 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by on-chip address input and data output latches. The ENABLE input serves as the device strobe controlling the latching functions. The I/O terminals when not data output enabled, represent high impedance ports for easy memory expansion.

## **Features**

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 22 pin — high density packaging
- Output data latches
- Select latch for microprocessor interface

## **Connection Diagram**

**Dual-In-Line Package**



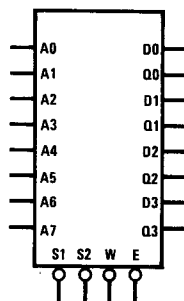
TOP VIEW

### **Pin Names**

A0-A7  
 $\bar{E}$   
 $\bar{W}$   
 D  
 Q  
 $\bar{S}1$ ,  $\bar{S}2$

Address Inputs  
 Chip Enable  
 Write Enable  
 Data Input  
 Data Output  
 Chip Selects

## **Logic Symbol**



Order Number NMC6551J-2, NMC6551J-9  
 or NMC6551J-5  
 See NS Package J22A

Order Number NMC6551N-5  
 See NS Package N22A

## Functional Description

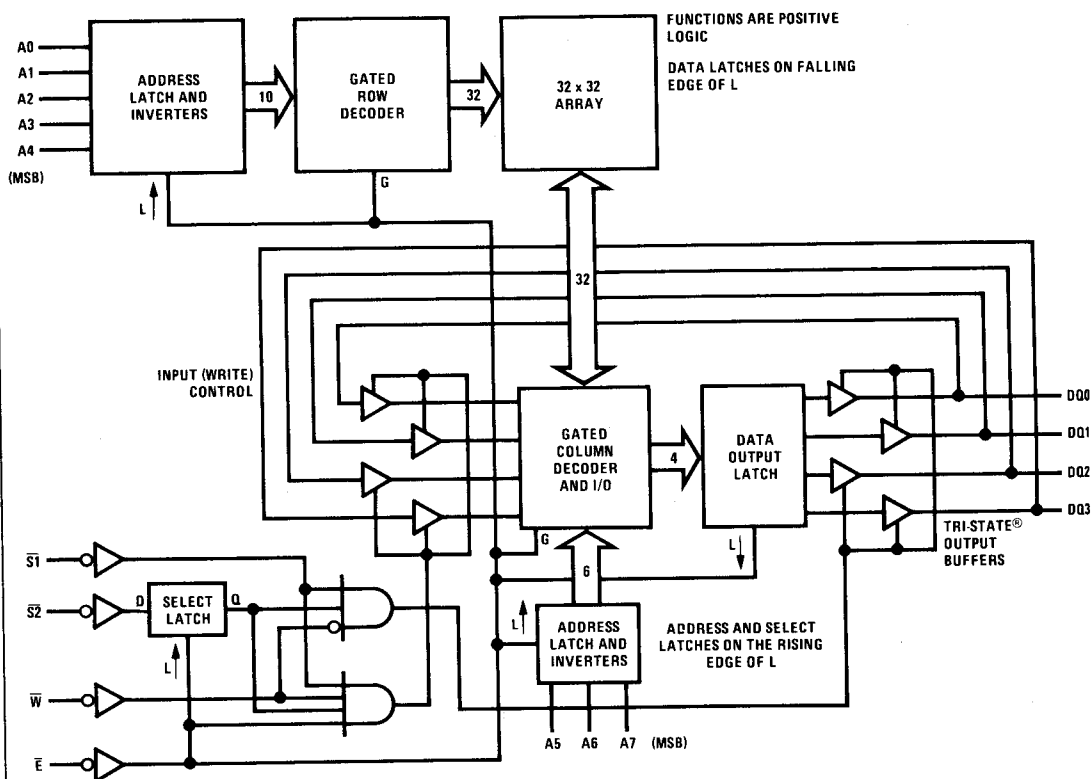
An NMC6551 memory cycle is initiated by the falling edge of the ENABLE ( $\bar{E}$ ) input, which latches the ADDRESS and SELECT 2 ( $\bar{S}_2$ ) information into the on-chip registers. Set-up and hold times must be met. Data output is enabled when the WRITE ( $\bar{W}$ ) input is HIGH and the ENABLE and SELECT 1 inputs are LOW.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the outputs. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to

return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next memory cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse timing is created by the coincident LOW of the WRITE, ENABLE and SELECT 1 inputs. The data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, or SELECT 1 input, whichever occurs first.

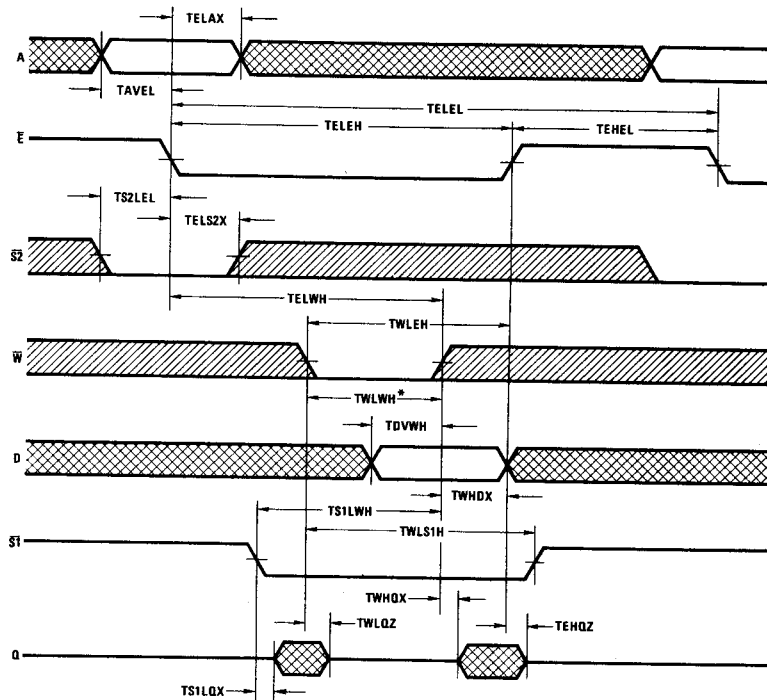
## Block Diagram



# Write Cycle AC Electrical Characteristics over the operating range

| Symbol | Parameter                                        | NMC6551B-9<br>NMC6551B-2 |     | NMC6551-9<br>NMC6551-2 |     | NMC6551-5 |     | Units |
|--------|--------------------------------------------------|--------------------------|-----|------------------------|-----|-----------|-----|-------|
|        |                                                  | Min                      | Max | Min                    | Max | Min       | Max |       |
| TAVEL  | Address Set-up Time                              | 0                        |     | 0                      |     | 10        |     | ns    |
| TELAX  | Address Hold Time                                | 40                       |     | 50                     |     | 70        |     | ns    |
| TWLWH  | Write Pulse Width ( $\bar{W}$ Low)               | 120                      |     | 180                    |     | 210       |     | ns    |
| TELEL  | Read or Write Cycle Time                         | 320                      |     | 400                    |     | 500       |     | ns    |
| TELEH  | Enable ( $\bar{E}$ ) Minimum Low Time            | 220                      |     | 300                    |     | 350       |     | ns    |
| TS2LEL | Chip Select 2 Set-up Time                        | 0                        |     | 0                      |     | 10        |     | ns    |
| TWHDX  | Data Hold Time                                   | 0                        |     | 0                      |     | 0         |     | ns    |
| TELS2X | Chip Select 2 Hold Time                          | 40                       |     | 50                     |     | 70        |     | ns    |
| TDVWH  | Data Set-up Time                                 | 100                      |     | 150                    |     | 170       |     | ns    |
| TELWH  | Write Pulse Width ( $\bar{E}$ and $\bar{W}$ Low) | 120                      |     | 180                    |     | 210       |     | ns    |
| TEHEL  | Enable ( $\bar{E}$ ) Minimum High Time           | 100                      |     | 100                    |     | 150       |     | ns    |
| TWLEH  | Write Pulse Width ( $\bar{E}$ and $\bar{W}$ Low) | 120                      |     | 180                    |     | 210       |     | ns    |
| TS1LWH | Chip Select 1 Write Pulse Hold Time              | 120                      |     | 180                    |     | 210       |     | ns    |
| TWLS1H | Chip Select 1 Write Pulse Set-up Time            | 120                      |     | 180                    |     | 210       |     | ns    |
| TS1LQX | Output Enable from $\bar{S}1$                    |                          | 130 |                        | 150 |           | 180 | ns    |
| TWLQZ  | Output Disable from $\bar{W}$                    |                          | 130 |                        | 150 |           | 180 | ns    |
| TWHQX  | Output Enable from $\bar{W}$                     |                          | 130 |                        | 150 |           | 180 | ns    |
| TEHQZ  | Output Disable from $\bar{E}$                    |                          | 130 |                        | 150 |           | 180 | ns    |

## Write Cycle Waveforms

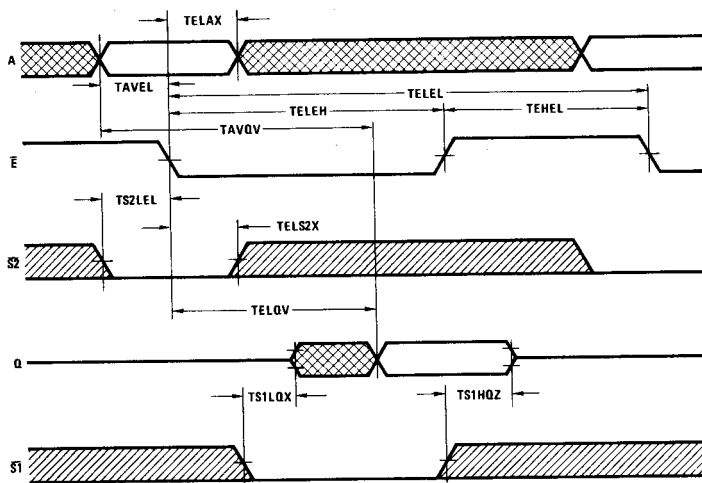


\* TWLWH, the write pulse, is the coincidence low of  $\bar{E}$ ,  $\bar{W}$ , and  $\bar{S}1$  inputs

# Read Cycle AC Electrical Characteristics over the operating range

| Symbol | Parameter                         | NMC6551B-9<br>NMC6551B-2 |     | NMC6551-9<br>NMC6551-2 |     | NMC6551-5 |     | Units |
|--------|-----------------------------------|--------------------------|-----|------------------------|-----|-----------|-----|-------|
|        |                                   | Min                      | Max | Min                    | Max | Min       | Max |       |
| TAVEL  | Address Set-up Time               | 0                        |     | 0                      |     | 10        |     | ns    |
| TELAX  | Address Hold Time                 | 40                       |     | 50                     |     | 70        |     | ns    |
| TELQV  | Enable Access Time                |                          | 220 |                        | 300 |           | 350 | ns    |
| TAVQV  | Address Access Time               |                          | 220 |                        | 300 |           | 360 | ns    |
| TELEH  | Enable (Ē) Minimum Low Time       | 220                      |     | 300                    |     | 350       |     | ns    |
| TELS2X | Chip Select 2 Hold Time           | 40                       |     | 50                     |     | 70        |     | ns    |
| TEHEL  | Enable (Ē) Minimum High Time      | 100                      |     | 100                    |     | 150       |     | ns    |
| TELEL  | Read or Write Cycle Time          | 320                      |     | 400                    |     | 500       |     | ns    |
| TS1LQX | Chip Select 1 Output Enable Time  |                          | 130 |                        | 150 |           | 180 | ns    |
| TS1HQZ | Chip Select 1 Output Disable Time |                          | 130 |                        | 150 |           | 180 | ns    |
| TS2LEL | Chip Select 2 Set-up Time         | 0                        |     | 0                      |     | 10        |     | ns    |

## Read Cycle Waveforms



## Absolute Maximum Ratings

|                                          |                     |
|------------------------------------------|---------------------|
| Supply Voltage VCC                       | 7V                  |
| Voltage at Any Pin                       | -0.3V to VCC + 0.3V |
| Storage Temperature Range                | -65°C to +150°C     |
| Package Dissipation                      | 500 mW              |
| Lead Temperature (Soldering, 10 seconds) | 300°C               |

## Operating Range

|                | Min   | Max   |
|----------------|-------|-------|
| Supply Voltage |       |       |
| NMC6551B-9     | 4.5V  | 5.5V  |
| NMC6551B-2     | 4.5V  | 5.5V  |
| NMC6551-9      | 4.5V  | 5.5V  |
| NMC6551-2      | 4.5V  | 5.5V  |
| NMC6551-5      | 4.75V | 5.25V |
| Temperature    |       |       |
| NMC6551B-9     | -40°C | 85°C  |
| NMC6551B-2     | -55°C | 125°C |
| NMC6551-9      | -40°C | 85°C  |
| NMC6551-2      | -55°C | 125°C |
| NMC6551-5      | 0°C   | 75°C  |

## DC Electrical Characteristics over the operating range, unless otherwise noted

| Symbol | Parameter                     | Conditions                             | NMC6551B-9, NMC6551B-2<br>NMC6551-9, NMC6551-2 |                | NMC6551-5 |           | Units |
|--------|-------------------------------|----------------------------------------|------------------------------------------------|----------------|-----------|-----------|-------|
|        |                               |                                        | Min                                            | Max            | Min       | Max       |       |
| VCCDR  | Data Retention Supply Voltage | VI = VCC, GND                          | 2.0                                            |                | 2.0       |           | V     |
| ICCSB  | Standby Supply Current        |                                        |                                                | 10<br>1(+25°C) |           | 100       | μA    |
| ICCOP* | Operating Supply Current      | f = 1 MHz, IO = 0,<br>VI = VCC or GND  |                                                | 4              |           | 4         | mA    |
| ICCDR  | Data Retention Supply Current | VCC = 3.0V, IO = 0,<br>VI = VCC or GND |                                                | 10             |           | 100       | μA    |
| II     | Input Leakage Current         | VI = VCC, GND                          | -1.0                                           | +1.0           | -1.0      | +1.0      | μA    |
| VIL    | Input Low Voltage             |                                        | -0.3                                           | 0.8            | -0.3      | 0.8       | V     |
| VIH    | Input High Voltage            |                                        | VCC - 2.0                                      | VCC + 0.3      | VCC - 2   | VCC + 0.3 | V     |
| IOZ    | Output Leakage Current        | VI = VCC, GND                          | -1.0                                           | +1.0           | -1.0      | +1.0      | μA    |
| VOL    | Output Low Voltage            | IOL = 3.2 mA                           |                                                | 0.4            |           | 0.4       | V     |
| VOH    | Output High Voltage           | IOH = -0.4 mA                          | 2.4                                            |                | 2.4       |           | V     |
| CI     | Input Capacitance             | f = 1 MHz                              |                                                | 6              |           | 6         | pF    |
| CO     | Output Capacitance            | f = 1 MHz                              |                                                | 10             |           | 10        | pF    |

\* ICCOP is proportional to operating frequency.

## AC Test Conditions

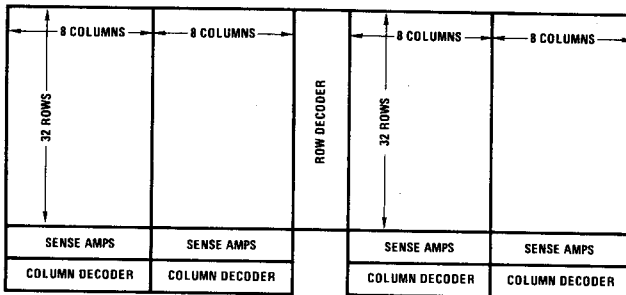
Input Rise and Fall Times: ≤ 20 ns

All Timing Reference Levels: 1/2 VCC

Output Load: 1 TTL Load, 50 pF

## NMC6551 Bit Map and Address Decoding

VCC

(MSB) ROWS (LSB)  
A4 A3 A2 A1 A0

|   |   |   |   |   |   |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

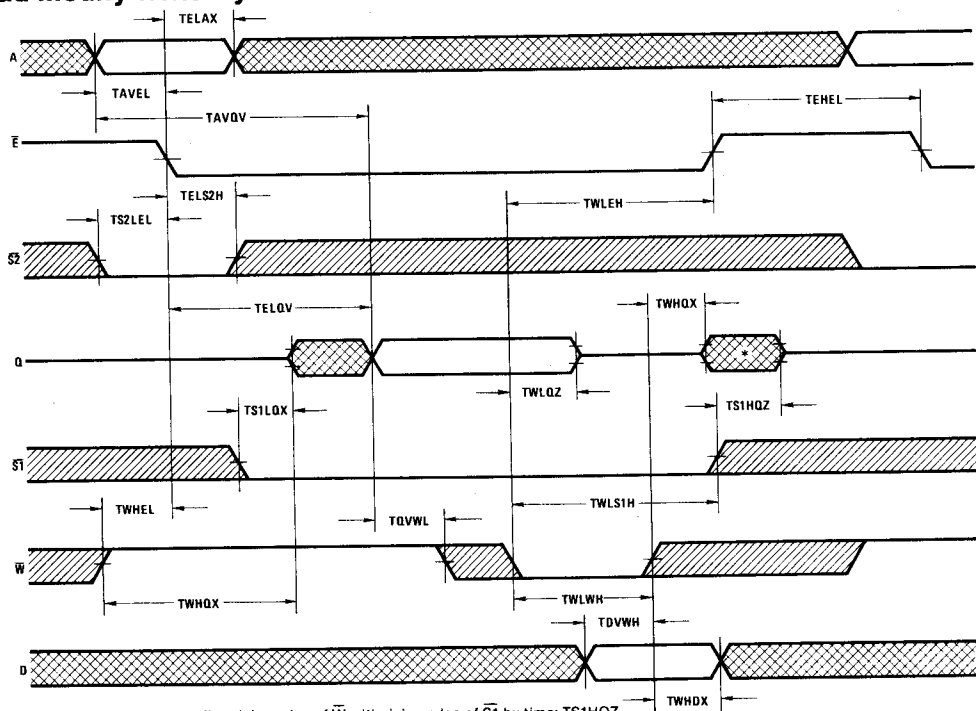
|           |   |   |   |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|---|---|---|
| (MSB) A7  | 1 | 1 | . | . | 0 | 1 | 1 | . | . | 0 |
| COLUMN A6 | 1 | 1 | . | . | 0 | 1 | 1 | . | . | 0 |
| (LSB) A5  | 1 | 0 | . | . | 0 | 1 | 0 | . | . | 0 |

|   |   |   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | . | . | 0 | 1 | 1 | . | . | 0 |
| 1 | 1 | . | . | 0 | 1 | 1 | . | . | 0 |
| 1 | 0 | . | . | 0 | 1 | 0 | . | . | 0 |

## Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

| Symbol | Parameter                                        | NMC6551B-9<br>NMC6551B-2 |     | NMC6551-9<br>NMC6551-2 |     | NMC6551-5 |     | Units |
|--------|--------------------------------------------------|--------------------------|-----|------------------------|-----|-----------|-----|-------|
|        |                                                  | Min                      | Max | Min                    | Max | Min       | Max |       |
| TAVEL  | Address Set-up Time                              | 0                        |     | 0                      |     | 10        |     | ns    |
| TELAX  | Address Hold Time                                | 40                       |     | 50                     |     | 70        |     | ns    |
| TELQV  | Enable Access Time                               |                          | 220 |                        | 300 |           | 350 | ns    |
| TAVQV  | Address Access Time                              |                          | 220 |                        | 300 |           | 360 | ns    |
| TWLEH  | Write Pulse Width ( $\bar{W}$ and $\bar{E}$ Low) | 120                      |     | 180                    |     | 210       |     | ns    |
| TEHEL  | Enable ( $\bar{E}$ ) Minimum High Time           | 100                      |     | 100                    |     | 150       |     | ns    |
| TWLWH  | Write Pulse Width ( $\bar{W}$ Low)               | 120                      |     | 180                    |     | 210       |     | ns    |
| TELEL  | Read or Write Cycle Time                         | 320                      |     | 400                    |     | 500       |     | ns    |
| TS1LQX | Chip Select 1 Output Enable Time                 |                          | 130 |                        | 150 |           | 180 | ns    |
| TS1HQZ | Chip Select 1 Output Disable Time                |                          | 130 |                        | 150 |           | 180 | ns    |
| TS2LEL | Chip Select 2 Set-up Time                        | 0                        |     | 0                      |     | 10        |     | ns    |
| TWHDX  | Data Hold Time                                   | 0                        |     | 0                      |     | 0         |     | ns    |
| TELS2H | Chip Select 2 Hold Time                          | 40                       |     | 50                     |     | 70        |     | ns    |
| TWLS1H | Chip Select 1 Write Pulse Set-up Time            | 120                      |     | 180                    |     | 210       |     | ns    |
| TWLQZ  | Output Disable from Write ( $\bar{W}$ )          |                          | 130 |                        | 150 |           | 180 | ns    |
| TDVWH  | Data Set-up Time                                 | 100                      |     | 150                    |     | 170       |     | ns    |
| TQVWL  | Data Valid to Write Time                         | 0                        |     | 0                      |     | 0         |     | ns    |
| TWHEL  | $\bar{W}$ Read Mode Set-up Time                  | 0                        |     | 0                      |     | 0         |     | ns    |
| TWHQX  | Output Enable from Write ( $\bar{W}$ )           |                          | 130 |                        | 150 |           | 180 | ns    |

## Read-Modify-Write Cycle Waveforms



\* Avoid unwanted output by preceding rising edge of  $\bar{W}$  with rising edge of  $S_1$  by time; TS1HQZ