Click here for production status of specific part numbers.

MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

General Description

The MAX15500/MAX15501 analog output conditioners provide a programmable current up to ±24mA, or a voltage up to ±12V proportional to a control voltage signal. The control voltage is typically supplied by an external DAC with an output voltage range of 0 to 4.096V for the MAX15500 and 0 to 2.5V for the MAX15501. The output current and voltage are selectable as either unipolar or bipolar. In the unipolar configuration, a control voltage of 5% full-scale (FS) produces a nominal output of 0A or 0V to achieve underrange capability. A control voltage of 100%FS produces one of two programmable levels (105%FS or 120%FS) to achieve overrange capability. The outputs of the MAX15500/MAX15501 are protected against overcurrent conditions and a short to ground or supply voltages up to ±35V. The devices also monitor for overtemperature and supply brownout conditions. The supply brownout threshold is programmable.

The MAX15500/MAX15501 are programmed through an SPI™ interface capable of daisy-chained operation. The MAX15500/MAX15501 provide extensive error reporting through the SPI interface and an additional open-drain interrupt output. The devices include an analog output to monitor load conditions.

The MAX15500/MAX15501 operate over the -40°C to +105°C temperature range. The devices are available in a 32-pin, 5mm x 5mm TQFN package.

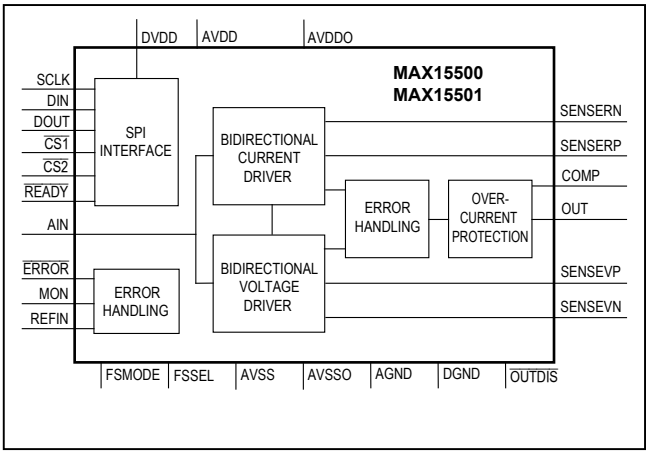
Applications

- Programmable Logic Controllers (PLCs)
- Distributed I/Os
- Embedded Systems
- Industrial Control and Automation

Benefits and Features

- Supply Voltage Up to ±32.5V
- Output Protected Up to ±35V
- Programmable Output (Plus Overrange)
  - ±10V
  - 0 to 10V
  - 0 to 5V
  - ±20mA
  - 0 to 20mA
  - 4 to 20mA
- Current Output Drives 0 to 1kΩ
- Voltage Output Drives Loads Down to 1kΩ
- HART Compliant
- 2ppm Gain Error Drift Over Temperature
- SPI Interface, with Daisy-Chain Capability
- Supports +4.096V (MAX15500) or +2.5V (MAX15501) Full-Scale Input Signals
- Extensive Error Reporting
  - Short-Circuit and Overcurrent Protection
  - Open-Circuit Detection
  - Brownout Detection
  - Overtemperature Protection
- Fast, 40µs Settling Time

Simplified Block Diagram



Absolute Maximum Ratings

AVDD to AGND .....-0.3V to +35V
AVSS to AGND.....-35V to +0.3V
AVDD to AVSS ..... 0 to +70V
AVDD to AVDDO ..... 0 to +4V
AVSS to AVSSO .....-4V to 0V
DGND to AGND.....-0.3V to +0.3V
AVDD to DVDD .....-6V to +35V
DVDD to DGND.....-0.3V to +6.0V
$\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, DOUT, $\overline{READY}$, $\overline{ERROR}$, FSMODE, MON, $\overline{OUTDIS}$, FSSEL to DGND .....-0.3V to +6.0V
AIN, REFIN to AGND .....-0.3V to +6.0V
SENSEVP, SENSEVN, SENSERP, SENSERN to AGND. the higher of -35V and (V_{AVSS} - 0.3V) to the lower of (V_{AVDD} + 0.3V) and +35V
OUT, COMP to AGND... the higher of -35V and (V_{AVSS} - 0.3V) to the lower of (V_{AVDD} + 0.3V) and +35V
Maximum Current on Pin .....±100mA
Continuous Power Dissipation (derate 34.5mW/°C above +70°C)
32-Pin TQFN (T_A = +70°C, multilayer board) 2758.6mW
Operating Temperature Range..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN-32

PACKAGE CODE	T3255+4
Outline Number	21-0140
Land Pattern Number	90-0012
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	47°C/W
Junction to Case (θ_{JC})	1.70°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.70°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{AVDD} = +24V, V_{AVSS} = -24V, V_{DVDD} = 5.0V, C_{LOAD} = 1nF, C_{COMP} = 0nF, V_{REFIN} = 4.096V for the MAX15500, V_{REFIN} = 2.5V for the MAX15501. All specifications for T_A = -40°C to +105°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (Note 1)						
Analog Positive Supply Voltage	V_{AVDD}	5% overrange (FSMODE = DVDD)	15	24	32.5	V
		20% overrange (FSMODE = DGND)	18.5	24	32.5	
Analog Negative Supply Voltage	V_{AVSS}	5% overrange (FSMODE = DVDD)	-32.5	-24	-15	V
		20% overrange (FSMODE = DGND)	-32.5	-24	-18.5	
AVDD to AVDDO Voltage Difference	V_{AVDDO}	(Note 1)		2.5		V
AVSS to AVSSO Voltage Difference	V_{AVSSO}	(Note 1)		2.5		V
Digital Supply Voltage	V_{DVDD}		2.7		5.25	V
Analog Positive Supply Current	I_{AP}	$I_{AP} = I_{AVDD} + I_{AVDDO}$, I_{LOAD} = 0A		5	7	mA
Analog Negative Supply Current	I_{AN}	$I_{AN} = I_{AVSS} + I_{AVSSO}$, I_{LOAD} = 0A	-7	-4.5		mA
Digital Supply Current	I_{DVDD}	V_{DVDD} = 5V		0.1	0.4	mA
Analog Positive Standby Current	I_{STBYP}	$I_{STBYP} = I_{AVDD} + I_{AVDDO}$, $\overline{OUTDIS}$ = DGND or software standby mode		1		mA
Analog Negative Standby Current	I_{STBYN}	$I_{STBYN} = I_{AVSS} + I_{AVSSO}$, $\overline{OUTDIS}$ = DGND or software standby mode		-0.5		mA
ANALOG INPUT (AIN, REFIN)						
Input Impedance	R_{IN}			10		kΩ
Input Capacitance	C_{IN}			10		pF
Analog Input Full Scale	V_{AIN}	FSSEL = DVDD, MAX15500	4.0	4.096	4.2	V
		FSSEL = DGND, MAX15501	2.4	2.5	2.6	
REFIN Full-Scale Input	V_{REFIN}	FSSEL = DVDD, MAX15500	4.0	4.096	4.2	V
		FSSEL = DGND, MAX15501	2.4	2.5	2.6	

Electrical Characteristics (continued)

(V_{AVDD} = +24V, V_{AVSS} = -24V, V_{DVDD} = 5.0V, C_{LOAD} = 1nF, C_{COMP} = 0nF, V_{REFIN} = 4.096V for the MAX15500, V_{REFIN} = 2.5V for the MAX15501. All specifications for T_A = -40°C to +105°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT OUTPUT (Note 2)							
Maximum Load Resistance	R_{LOAD}	V_{AVDD} = +24V, V_{AVSS} = -24V			750		Ω
		V_{AVDD} = +32.5V, V_{AVSS} = -32.5V			1000		
Maximum Load Inductance	L_{LOAD}	C_{COMP} = 100nF (Note 3)			15		mH
Maximum Load Capacitance	C_{LOAD}	C_{COMP} = 4.7nF			100		µF
Maximum Settling Time		Full-scale step from 0 to 20mA or -20mA to + 20mA, R_{LOAD} = 750Ω	To 0.1% accuracy, L_{LOAD} = 20µH, C_{COMP} = 0nF		40		µs
			To 0.1% accuracy, L_{LOAD} = 1mH, C_{COMP} = 0.15nF		500		
			To 0.1% accuracy, L_{LOAD} = 10mH, C_{COMP} = 0.15nF		500		
			To 0.01% accuracy, L_{LOAD} = 20µH, C_{COMP} = 0nF		60		
			To 0.01% accuracy, L_{LOAD} = 10mH, C_{COMP} = 0.15nF		600		
		1% full-scale step, R_{LOAD} = 750Ω	To 0.1% accuracy, L_{LOAD} = 20µH, C_{COMP} = 0nF		20		
			To 0.1% accuracy, L_{LOAD} = 1mH, C_{COMP} = 0.15nF		100		
			To 0.1% accuracy, L_{LOAD} = 10mH, C_{COMP} = 0.15nF		100		
			To 0.01% accuracy, L_{LOAD} = 20FH, C_{COMP} = 0nF		40		
			To 0.01% accuracy, L_{LOAD} = 10mH, C_{COMP} = 0.15nF		200		
Full-Scale Output Current	I_{OUT}	V_{FSMODE} = V_{DVDD}			±21		mA
		V_{FSMODE} = V_{DGND}			±24		

Electrical Characteristics (continued)

(V_{AVDD} = +24V, V_{AVSS} = -24V, V_{DVDD} = 5.0V, C_{LOAD} = 1nF, C_{COMP} = 0nF, V_{REFIN} = 4.096V for the MAX15500, V_{REFIN} = 2.5V for the MAX15501. All specifications for T_A = -40°C to +105°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Offset Error		V_{AIN} = 5% of V_{REFIN} (unipolar mode), V_{AIN} = 50% of V_{REFIN} (bipolar mode)			±0.1	±0.5	%FS
Offset-Error Drift					±5		ppm/°C
Gain Error	GE	0.01% precision R_{SENSE}, tested according to the ideal transfer functions shown in Table 8	MAX15500		±0.1	±0.51	%FS
			MAX15501		±0.1	±0.5	
Gain-Error Drift		No R_{SENSE} drift			±2		ppm/°C
Integral Nonlinearity Error	INL				0.05		%FS
Output Conductance		(dI_{OUT}/dV_{OUT}), I_{OUT} = 24mA, R_{LOAD} = 750Ω to 0Ω, FSMODE = DGND, unipolar mode			1.0		µA/V
Power-Supply Rejection Ratio	PSRR	At DC, V_{AVDD} = +24V to +32.5V, V_{AVSS} = -24V to -32.5V, V_{AIN} = V_{REFIN}, unipolar mode, FSMODE = DVDD			1.6		µA/V
Overcurrent Limit		R_{SENSE} shorted		25	30	40	mA
Output Current Noise		0.1Hz to 10Hz			20		nA_{RMS}
		At 1kHz			2.6		$nA/\sqrt{Hz}$
Output Slew Rate					1.5		mA/µs
Small-Signal Bandwidth					30		kHz
Maximum OUT Voltage to AVDDO		V_{AVDDO} - V_{OUT}			2.0		V
Minimum OUT Voltage to AVSSO		V_{OUT} - V_{AVSSO}			2.0		V
VOLTAGE OUTPUT (R_{LOAD} = 1kΩ)							
Minimum Resistive Load	R_{LOAD}				1		kΩ
Maximum Capacitive Load	C_{LOAD}	C_{COMP} = 4.7nF			100		µF
Maximum Settling Time (Full-Scale Step)		To 0.1% accuracy, load = 1kΩ in parallel with 1nF, C_{COMP} = 0nF			20		µs
		To 0.1% accuracy, load = 1kΩ in parallel with 1µF, C_{COMP} = 4.7nF			1000		
		To 0.01% accuracy, load = 1kΩ in parallel with 1nF, C_{COMP} = 0nF			30		
		To 0.01% accuracy, load = 1kΩ in parallel with 1µF, C_{COMP} = 4.7nF			1300		

Electrical Characteristics (continued)

(V_{AVDD} = +24V, V_{AVSS} = -24V, V_{DVDD} = 5.0V, C_{LOAD} = 1nF, C_{COMP} = 0nF, V_{REFIN} = 4.096V for the MAX15500, V_{REFIN} = 2.5V for the MAX15501. All specifications for T_A = -40°C to +105°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Settling Time (1% Full-Scale Step)		To 0.1% accuracy, load = 1kΩ in parallel with 1nF, C_{COMP} = 0nF			10		µs
		To 0.1% accuracy, load = 1kΩ in parallel with 1µF, C_{COMP} = 4.7nF			300		
		To 0.01% accuracy, load = 1kΩ in parallel with 1nF, C_{COMP} = 0nF			20		
		To 0.01% accuracy, load = 1kΩ in parallel with 1µF, C_{COMP} = 4.7nF			600		
Gain Error		Tested according to the ideal transfer functions shown in Table 9			±0.1	±0.5	%FS
Gain-Error Drift					±2		ppm/°C
Full-Scale Output Voltage	V_{OUT}	FSMODE = DVDD	5V range		5.25		V
			10V range		10.5		
		FSMODE = DGND	5V range		6		
			10V range		12		
Offset Error		V_{AIN} = 5% of V_{REFIN} (unipolar mode), V_{AIN} = 50% of V_{REFIN} (bipolar mode)			±0.1	±0.5	%FS
Offset-Error Drift					±2		ppm/°C
Integral Nonlinearity Error	INL				0.05		%FS
Power-Supply Rejection	PSRR	At DC, V_{AVDD} = +18.5V to +32.5V, V_{AVSS} = -18.5V to -32.5V, V_{AIN} = V_{REFIN}			30		µV/V
Output-Voltage Noise		0.1Hz to 10Hz			16.3		$µV_{RMS}$
		1kHz			250		nV/√Hz
Output-Voltage Slew Rate					1.5		V/µs
Short-Circuit Current				20	30	45	mA
Maximum OUT Voltage to AVDDO		V_{AVDDO} - V_{OUT}			2.0		V
Minimum OUT Voltage to AVSSO		V_{OUT} - V_{AVSSO}			2.0		V

Electrical Characteristics (continued)

(V_{AVDD} = +24V, V_{AVSS} = -24V, V_{DVDD} = 5.0V, C_{LOAD} = 1nF, C_{COMP} = 0nF, V_{REFIN} = 4.096V for the MAX15500, V_{REFIN} = 2.5V for the MAX15501. All specifications for T_A = -40°C to +105°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT MONITOR (MON)						
Maximum Output Voltage		Current mode, see the *Output Monitor* section for V_{MON} equations		3		V
		Voltage mode, see the *Output Monitor* section for V_{MON} equations		3		
Output Resistance				35		kΩ
OVERTEMPERATURE DETECTION						
Overtemperature Threshold				+150		°C
Overtemperature Threshold Hysteresis				10		°C
DIGITAL INPUTS ($\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, $\overline{OUTDIS}$, FSSEL, FSMODE)						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input Hysteresis	V_{IHYST}			300		mV
Input Leakage Current	I_{IN}	V_{INPUT} = 0V or V_{DVDD}		±0.1	±1.0	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUT (DOUT, $\overline{READY}$)						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA	V_{DVDD} - 0.5			V
Output Three-State Leakage	I_{OZ}	DOUT only		±0.1	±10	µA
Output Three-State Capacitance	C_{OZ}	DOUT only		15		pF
Output Short-Circuit Current	I_{OSS}	V_{DVDD} = 5.25V		±150		mA
DIGITAL INTERRUPT ($\overline{ERROR}$)						
Interrupt Active Voltage	V_{INT}	I_{SINK} = 5.0mA			0.4	V
Interrupt Inactive Leakage	I_{INTZ}			±0.1	±1.0	µA
Interrupt Inactive Capacitance	C_{INTZ}			15		pF
Interrupt Short-Circuit Current	I_{INTSS}	V_{DVDD} = 2.7V	5	30		mA

Electrical Characteristics (continued)

(V_{AVDD} = +24V, V_{AVSS} = -24V, V_{DVDD} = 5.0V, C_{LOAD} = 1nF, C_{COMP} = 0nF, V_{REFIN} = 4.096V for the MAX15500, V_{REFIN} = 2.5V for the MAX15501. All specifications for T_A = -40°C to +105°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
Serial-Clock Frequency	f_{SCLK}	(Note 4)	0		20	MHz
SCLK Pulse-Width High	t_{CH}	40% duty cycle	20			ns
SCLK Pulse-Width Low	t_{CL}	60% duty cycle	20			ns
$\overline{CS_}$ Fall to SCLK Fall Setup Time	t_{CSS}	To 1st SCLK falling edge	15			ns
SCLK Fall to $\overline{CS_}$ Fall Hold Time	t_{CSH}	(Note 5)	0			ns
DIN to SCLK Fall Setup Time	t_{DS}		15			ns
DIN to SCLK Fall Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Settle Time	t_{DOT}	C_{LOAD} = 20pF			30	ns
SCLK Fall to DOUT Hold Time	t_{DOH}	C_{LOAD} = 0pF	2			ns
SCLK Fall to DOUT Disable	t_{DOZ}	14th SCLK deassertion (Note 6)			30	ns
SCLK Fall to $\overline{READY}$ Fall	t_{CR}	16th SCLK assertion, C_{LOAD} = 0pF or 20pF	2		30	ns
$\overline{CS_}$ Fall to DOUT Enable	t_{DOE}	Asynchronous assertion	1		35	ns
$\overline{CS_}$ Rise to DOUT Disable	t_{CSDOZ}	Asynchronous deassertion			35	ns
$\overline{CS_}$ Rise to $\overline{READY}$ Rise	t_{CSR}	Asynchronous deassertion, C_{LOAD} = 20pF			35	ns
$\overline{CS_}$ Pulse-Width High	t_{CSW}		15			ns

Note 1: Use diodes as shown in the *Typical Operating Circuit/Functional Diagram* to ensure a voltage difference of 2V to 3.5V from AVDD to AVDDO and from AVSS to AVSSO.

Note 2: R_{LOAD} = 750Ω. For the MAX15500, R_{SENSE} = 48.7Ω for FSMODE = DVDD and R_{SENSE} = 42.2Ω for FSMODE = DGND. For the MAX15501, R_{SENSE} = 47.3Ω for FSMODE = DVDD and R_{SENSE} = 41.2Ω for FSMODE = DGND. See the *Typical Operating Circuit/Functional Diagram*.

Note 3: Condition at which part is stable.

Note 4: The maximum clock speed for daisy-chain applications is 10MHz.

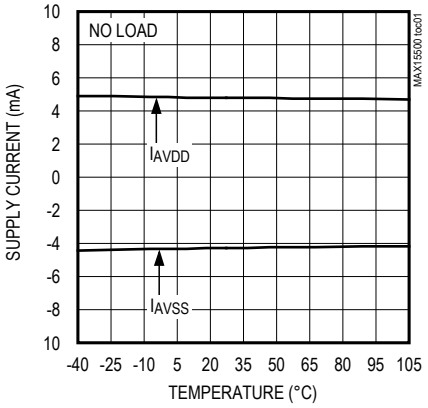
Note 5: t_{CSH} is applied to $\overline{CS_}$ falling to determine the 1st SCLK falling edge in a free-running SCLK application. It is also applied to $\overline{CS_}$ rising with respect to the 15th SCLK falling edge to determine the end of the frame.

Note 6: After the 14th SCLK falling edge, the MAX15500/MAX15501 outputs are high impedance and DOUT data is ignored.

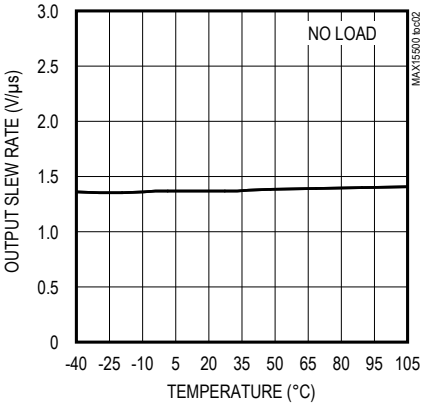
Typical Operating Characteristics

(V_{AVDD} = +24V, V_{DVDD} = +5V, V_{AVSS} = -24V, C_{LOAD} = 1nF, 5% overrange mode, unipolar current output or bipolar voltage-output mode, V_{REFIN} = +4.096V, T_A = +25°C, unless otherwise specified.)

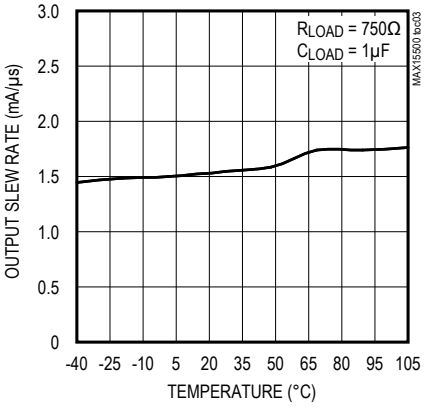
SUPPLY CURRENT vs. TEMPERATURE



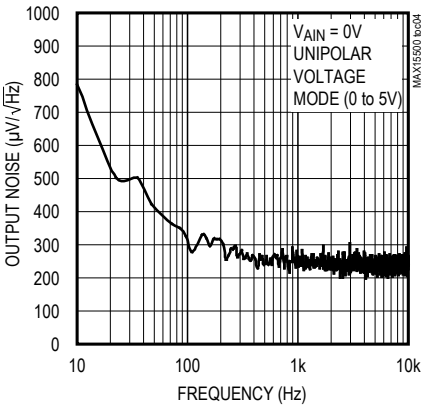
VOLTAGE-MODE OUTPUT SLEW RATE vs. TEMPERATURE



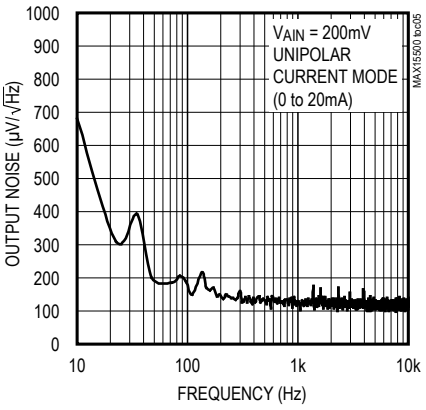
CURRENT-MODE OUTPUT SLEW RATE vs. TEMPERATURE



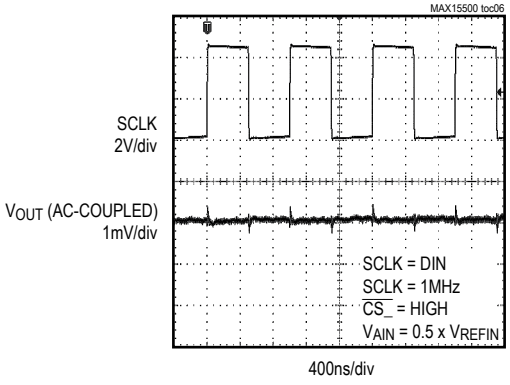
VOLTAGE-MODE OUTPUT NOISE vs. FREQUENCY



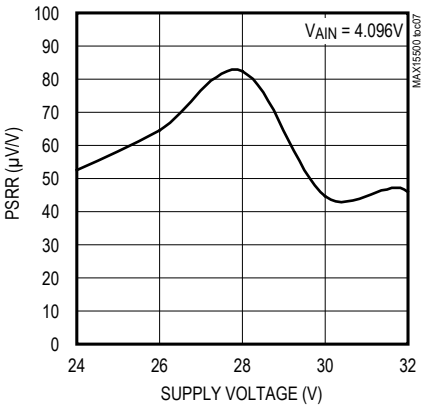
CURRENT-MODE OUTPUT NOISE vs. FREQUENCY



DIGITAL FEEDTHROUGH



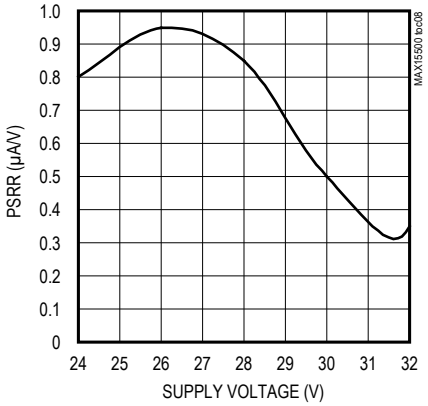
VOLTAGE-MODE PSRR vs. SUPPLY VOLTAGE



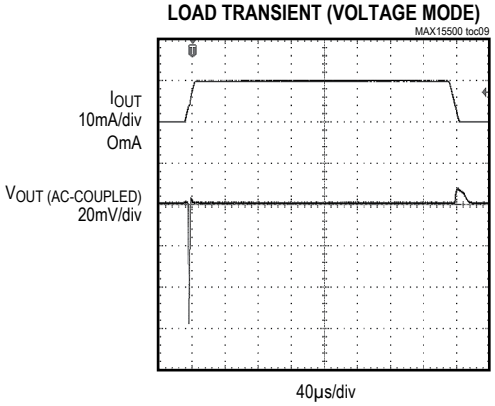
Typical Operating Characteristics (continued)

(V_{AVDD} = +24V, V_{DVDD} = +5V, V_{AVSS} = -24V, C_{LOAD} = 1nF, 5% overrange mode, unipolar current output or bipolar voltage-output mode, V_{REFIN} = +4.096V, T_A = +25°C, unless otherwise specified.)

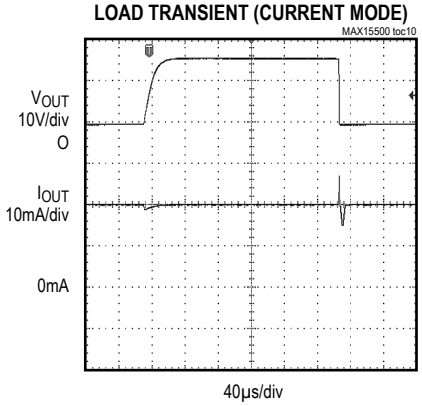
CURRENT-MODE PSRR vs. SUPPLY VOLTAGE



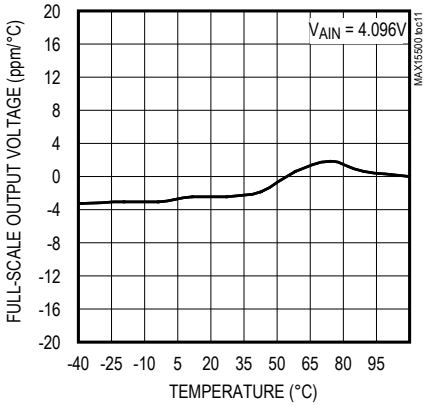
LOAD TRANSIENT (VOLTAGE MODE)



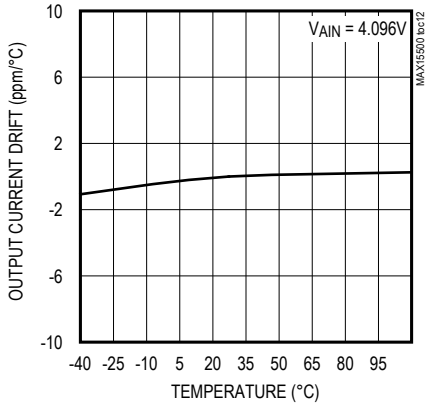
LOAD TRANSIENT (CURRENT MODE)



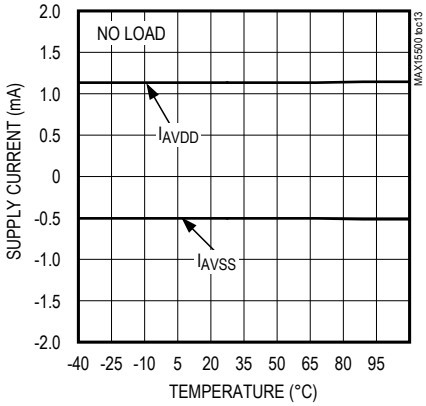
FULL-SCALE OUTPUT VOLTAGE vs. TEMPERATURE



OUTPUT CURRENT DRIFT vs. TEMPERATURE



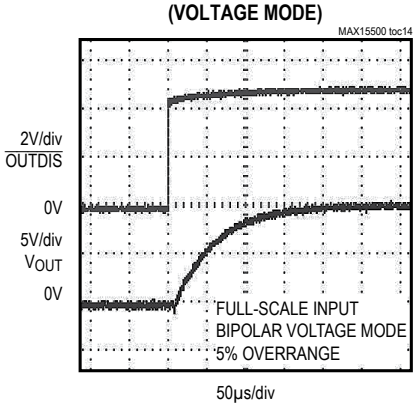
STANDBY SUPPLY CURRENT vs. TEMPERATURE



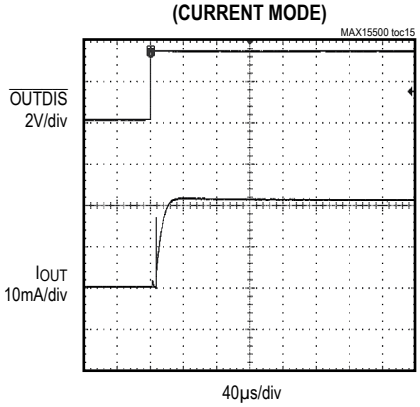
Typical Operating Characteristics (continued)

(V_{AVDD} = +24V, V_{DVDD} = +5V, V_{AVSS} = -24V, C_{LOAD} = 1nF, 5% overrange mode, unipolar current output or bipolar voltage-output mode, V_{REFIN} = +4.096V, T_A = +25°C, unless otherwise specified.)

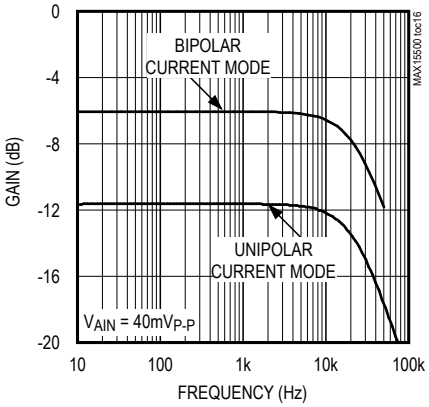
WAKEUP FROM STANDBY (VOLTAGE MODE)



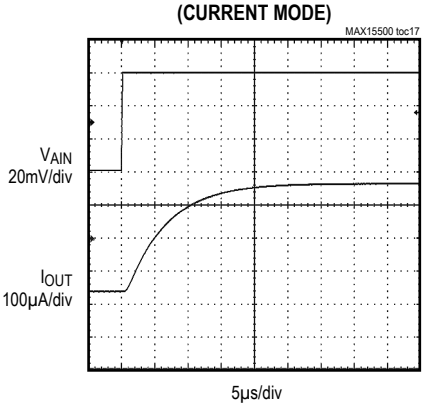
WAKEUP FROM STANDBY (CURRENT MODE)



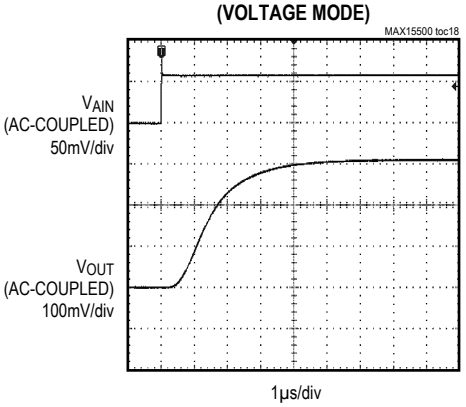
GAIN vs. FREQUENCY (HART COMPLIANT)



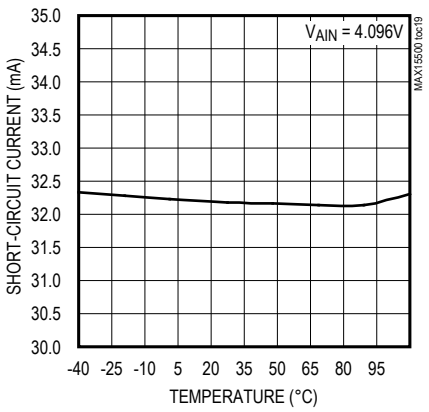
SMALL-SIGNAL STEP RESPONSE (CURRENT MODE)



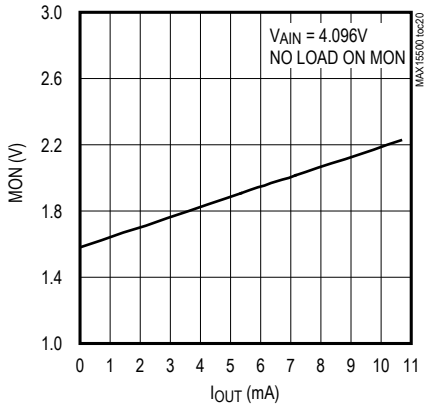
SMALL-SIGNAL STEP RESPONSE (VOLTAGE MODE)



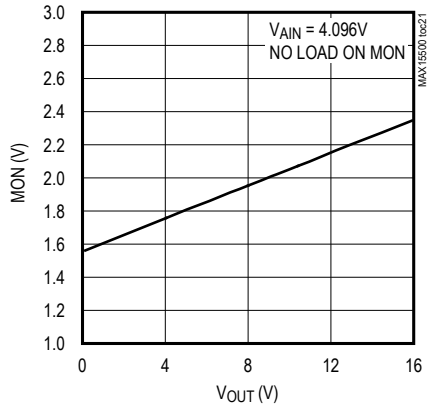
OUTPUT SHORT-CIRCUIT CURRENT vs. TEMPERATURE



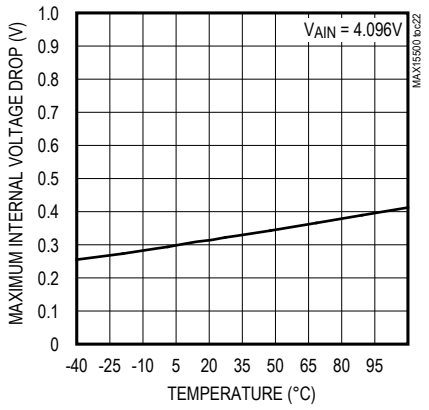
VOLTAGE-MODE MON TRANSFER CURVE vs. OUTPUT CURRENT



CURRENT-MODE MON TRANSFER CURVE vs. OUTPUT VOLTAGE



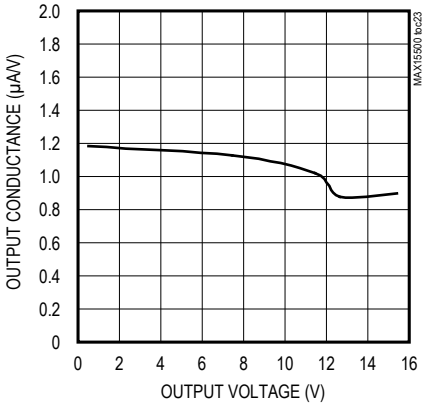
VOLTAGE-MODE MAXIMUM OUT TO AVDDO VOLTAGE vs. TEMPERATURE



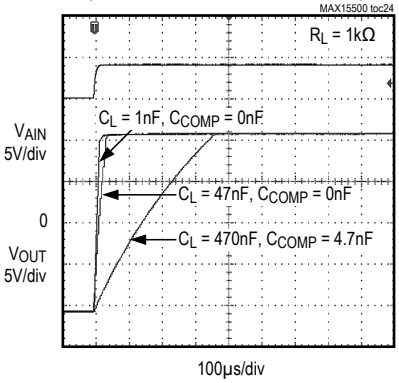
Typical Operating Characteristics (continued)

(V_{AVDD} = +24V, V_{DVDD} = +5V, V_{AVSS} = -24V, C_{LOAD} = 1nF, 5% overrange mode, unipolar current output or bipolar voltage-output mode, V_{REFIN} = +4.096V, T_A = +25°C, unless otherwise specified.)

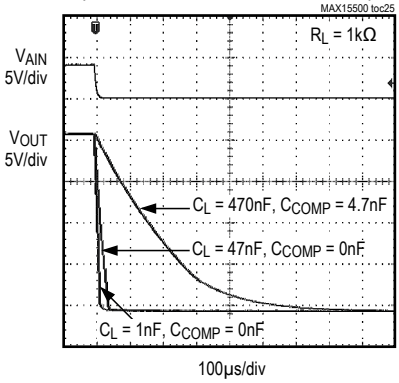
CURRENT-MODE OUTPUT CONDUCTANCE vs. OUTPUT VOLTAGE



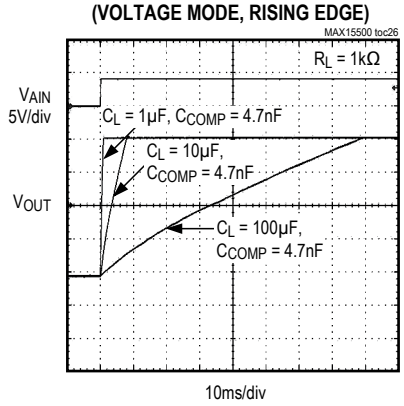
LARGE-SIGNAL SETTLING TIME (VOLTAGE MODE, RISING EDGE)



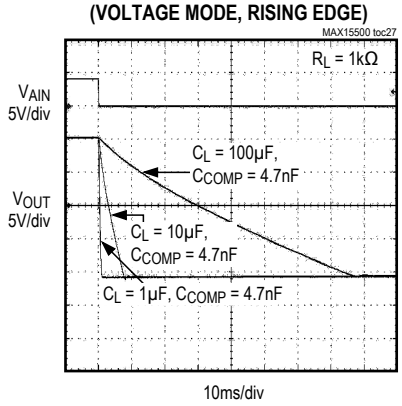
LARGE-SIGNAL SETTLING TIME (VOLTAGE MODE, FALLING EDGE)



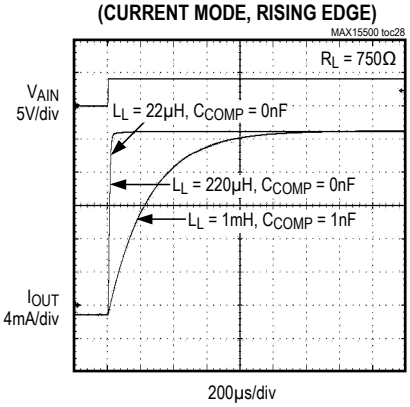
LARGE-SIGNAL SETTLING TIME (VOLTAGE MODE, RISING EDGE)



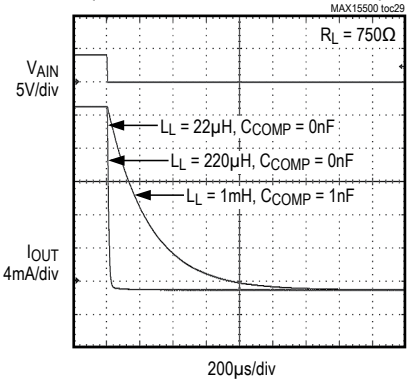
LARGE-SIGNAL SETTLING TIME (VOLTAGE MODE, RISING EDGE)



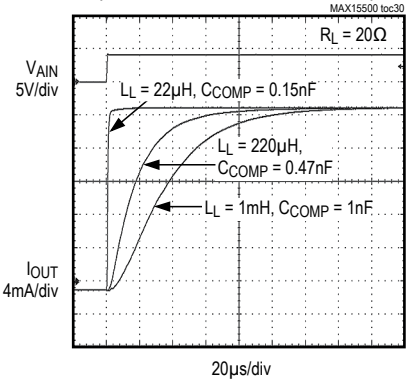
LARGE-SIGNAL SETTLING TIME (CURRENT MODE, RISING EDGE)



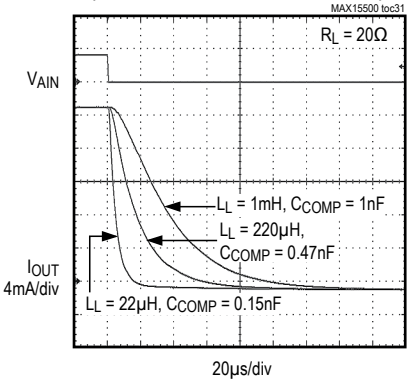
LARGE-SIGNAL SETTLING TIME (CURRENT MODE, FALLING EDGE)



LARGE-SIGNAL SETTLING TIME (CURRENT MODE, RISING EDGE)



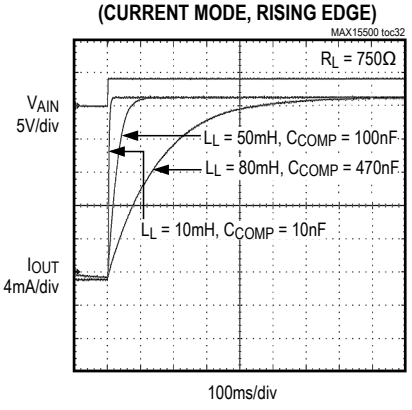
LARGE-SIGNAL SETTLING TIME (CURRENT MODE, FALLING EDGE)



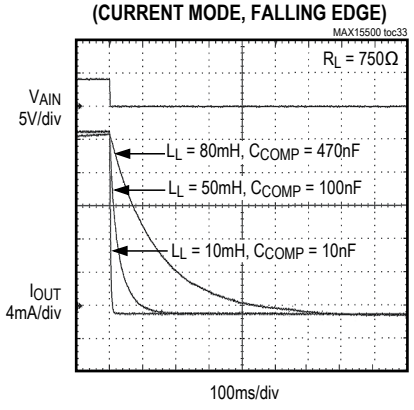
Typical Operating Characteristics (continued)

(V_{AVDD} = +24V, V_{DVDD} = +5V, V_{AVSS} = -24V, C_{LOAD} = 1nF, 5% overrange mode, unipolar current output or bipolar voltage-output mode, V_{REFIN} = +4.096V, T_A = +25°C, unless otherwise specified.)

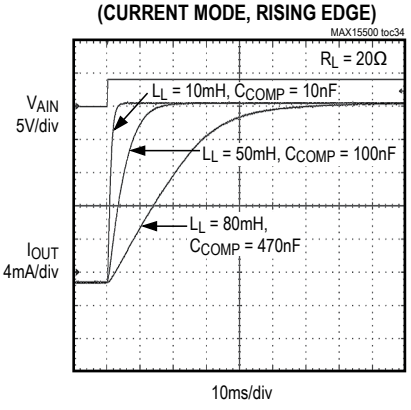
LARGE-SIGNAL SETTLING TIME (CURRENT MODE, RISING EDGE)



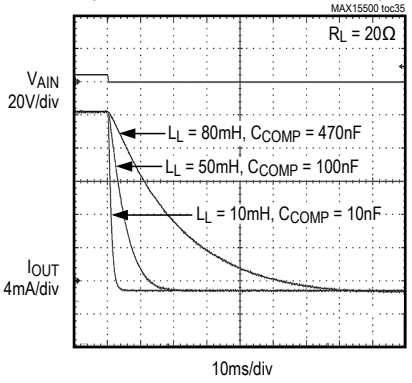
LARGE-SIGNAL SETTLING TIME (CURRENT MODE, FALLING EDGE)



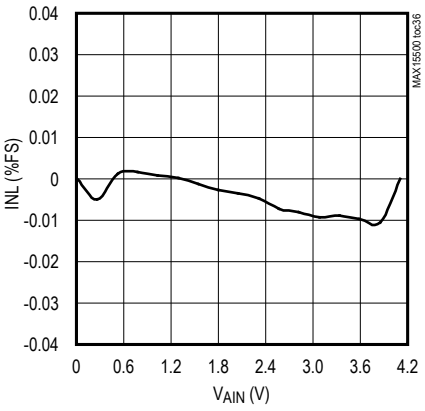
LARGE-SIGNAL SETTLING TIME (CURRENT MODE, RISING EDGE)



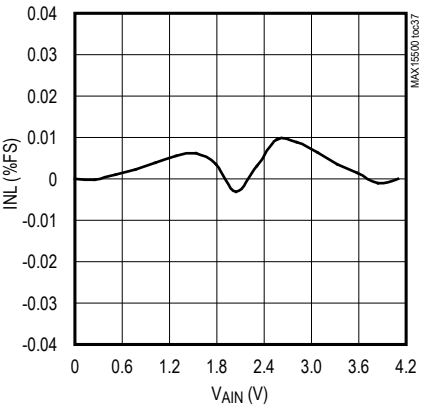
LARGE-SIGNAL SETTLING TIME (CURRENT MODE, FALLING EDGE)



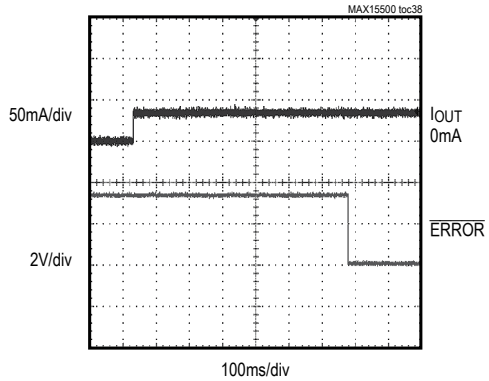
CURRENT-MODE INL



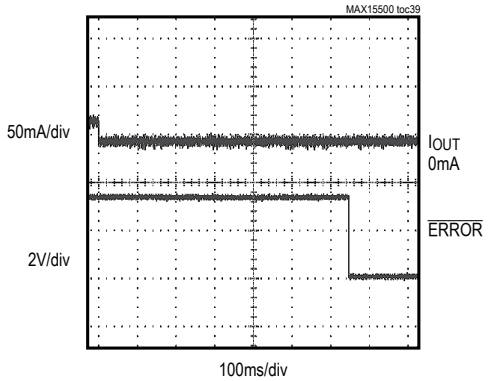
VOLTAGE-MODE INL



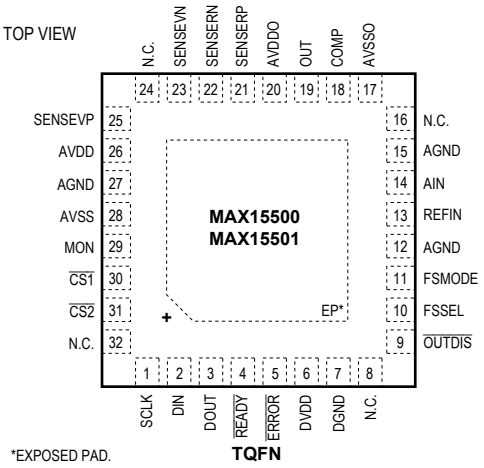
VOLTAGE-MODE SHORT-CIRCUIT DETECTION



CURRENT-MODE OPEN-CIRCUIT DETECTION



Pin Configuration



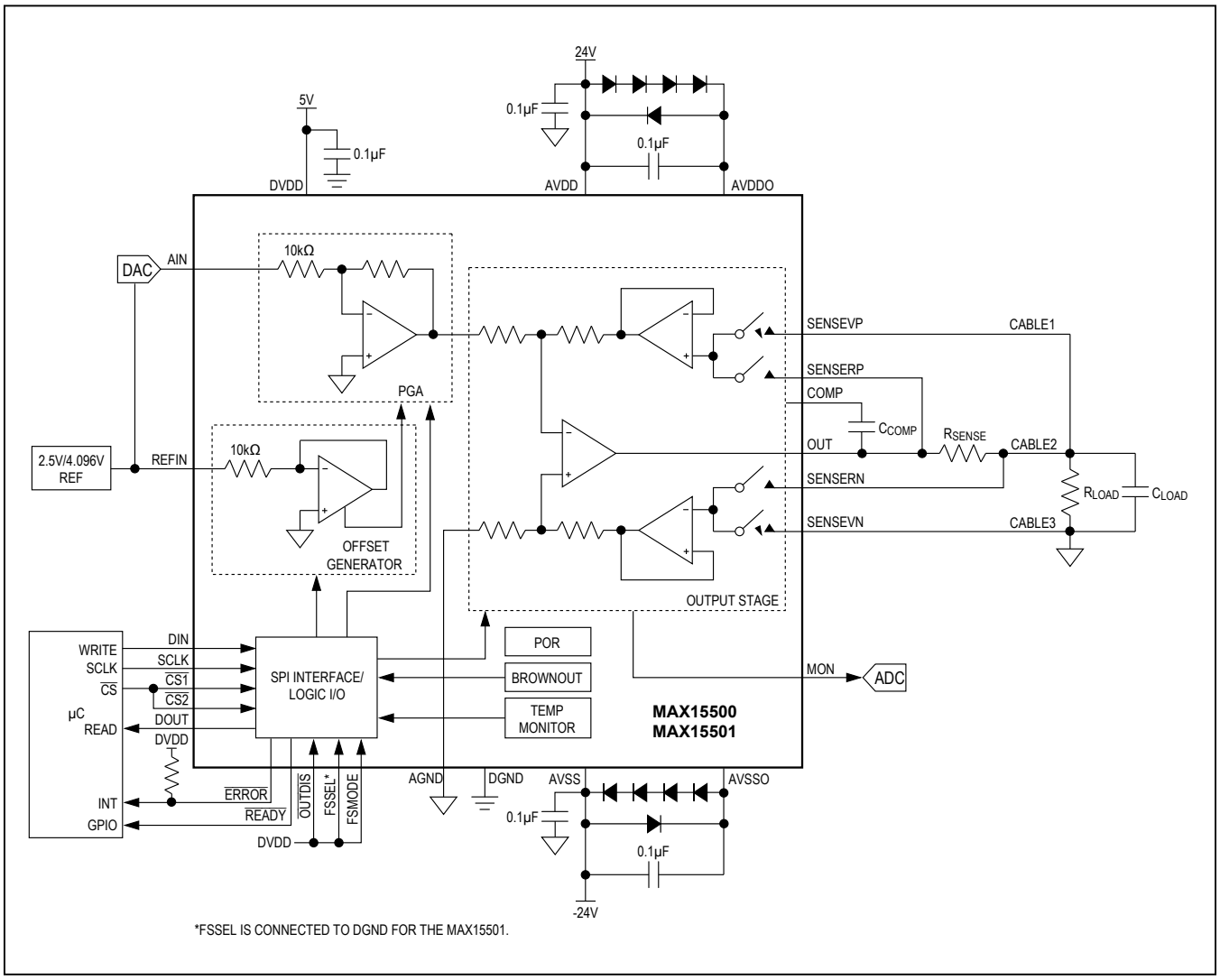
Pin Description

PIN	NAME	FUNCTION
1	SCLK	SPI Clock Input. Activate SCLK only when $\overline{CS_}$ is low to minimize noise coupling.
2	DIN	SPI Data Input. Data is clocked into the serial interface on the falling edge of SCLK.
3	DOUT	SPI Data Output. Data transitions at DOUT on the falling edge of SCLK. DOUT is high impedance when either $\overline{CS1}$ or $\overline{CS2}$ is high.
4	$\overline{READY}$	Active-Low Device Ready Output. $\overline{READY}$ is an active-low output that goes low when the device successfully completes processing an SPI data frame. $\overline{READY}$ returns high at the next rising edge of $\overline{CS_}$. In daisy-chain applications, the $\overline{READY}$ output typically drives the $\overline{CS_}$ input of the next device in the chain or a GPIO of a microcontroller.
5	$\overline{ERROR}$	Active-Low Flag Output. $\overline{ERROR}$ is an open-drain output that pulls low when output short circuit, output open circuit, overtemperature, or brownout conditions occur. $\overline{ERROR}$ typically drives an interrupt input of a microcontroller. The $\overline{ERROR}$ output is cleared after the internal error register is read through the SPI interface. Connect a 10kΩ pullup resistor from $\overline{ERROR}$ to DVDD. The MAX15500K/MAX15501K offer enhanced error mode logic. See the Error Handling section and Figures 11a and 11b for more details.
6	DVDD	Digital Power-Supply Voltage Input. Apply either a 3V or 5V nominal voltage supply to DVDD. DVDD powers the digital portion of the MAX15500/MAX15501. Bypass DVDD to DGND with a 0.1µF capacitor as close as possible to the device.
7	DGND	Digital Ground
8, 16, 24, 32	N.C.	No Connection. Not internally connected.
9	$\overline{OUTDIS}$	Active-Low Output Disable Input. $\overline{OUTDIS}$ is an active-low logic input that forces the analog output to 0A or 0V and puts the device in standby mode when connected to DGND. Connect $\overline{OUTDIS}$ to DVDD for normal operation.
10	FSSEL	Full-Scale Select Input. Connect FSSEL to DVDD for the MAX15500 when applying a +4.096V reference at REFIN. Connect FSSEL to DGND for the MAX15501 when applying a +2.50V reference at REFIN.

Pin Description (continued)

PIN	NAME	FUNCTION
11	FSMODE	Overrange Mode Select Input. Connect FSMODE to DVDD to set the output voltage to 105%FS when the input voltage is equal to the full-scale value. Connect FSMODE to DGND to set the output voltage to 120%FS when the input voltage is equal to the full-scale value. FSMODE has no effect in current mode.
12, 15, 27	AGND	Analog Ground
13	REFIN	Reference Voltage Input. Connect REFIN to an external +4.096V reference for the MAX15500 or +2.5V reference for the MAX15501. REFIN is used to set the offset for unipolar and bipolar modes.
14	AIN	Analog Signal Input. The analog input signal range at AIN is from 0V to the nominal full scale of +4.096V for the MAX15500 and +2.5V for the MAX15501.
17	AVSSO	Negative Output Driver Supply Voltage Input. AVSSO provides power to the driver output stage. Bypass AVSSO to AVSS with a 0.1µF capacitor. Use diodes as shown in the *Typical Operating Circuit/Functional Diagram* to ensure a voltage difference of 2V to 3.5V between AVSS and AVSSO.
18	COMP	Output Amplifier Compensation Feedback Node. Connect a compensation capacitor from COMP to OUT. See Table 10 for the recommended compensation capacitor values.
19	OUT	Analog Output. The analog voltage or current output range at OUT is programmable. See Tables 1 to 4 for possible output range settings.
20	AVDDO	Positive Output Driver Supply Voltage Input. AVDDO provides power to the driver output stage. Bypass AVDDO to AVDD with a 0.1µF capacitor. Use diodes as shown in the *Typical Operating Circuit/Functional Diagram* to ensure a voltage difference of 2V to 3.5V between AVDD and AVDDO.
21	SENSERP	Sense Resistor Positive Connection. See the *Typical Operating Circuit/Functional Diagram* for the typical connection.
22	SENSERN	Sense Resistor Negative Connection. See the *Typical Operating Circuit/Functional Diagram* for the typical connection.
23	SENSEVN	Kelvin Sense Voltage Negative Input. See the *Typical Operating Circuit/Functional Diagram* for the typical connection.
25	SENSEVP	Kelvin Sense Voltage Positive Input. See the *Typical Operating Circuit/Functional Diagram* for the typical connection.
26	AVDD	Positive Analog Supply Voltage Input. Bypass AVDD to AGND with a 0.1µF capacitor.
28	AVSS	Negative Analog Supply Voltage Input. Bypass AVSS to AGND with a 0.1µF capacitor.
29	MON	Load Monitoring Output. MON provides an analog 0 to 3V output. See the *Output Monitor* section.
30	$\overline{CS1}$	Active-Low SPI Chip-Select Input 1. See the *SPI Interface* section.
31	$\overline{CS2}$	Active-Low SPI Chip-Select Input 2. See the *SPI Interface* section.
—	EP	Exposed Pad. Internally connected to AVSS. Connect to AVSS. Connect to a large copper area to maximize thermal performance. Do not connect ground or signal lines through EP.

Typical Operating Circuit/Functional Diagram



Detailed Description

The MAX15500/MAX15501 output a programmable current up to ±24mA or a voltage up to ±12V proportional to a control signal at AIN. The devices operate from a dual 15V to 32.5V supply. The control voltage applied at AIN is typically supplied by an external DAC with an output voltage range of 0 to 4.096V for the MAX15500 and 0 to 2.5V for the MAX15501. The MAX15500/MAX15501 are capable of both unipolar and bipolar current and voltage outputs. In current mode, the devices produce currents of -1.2mA to +24mA or -24mA to +24mA. In voltage mode, the devices produce voltages of -0.3V to +6V, -0.6V to +12V, or ±12V. To allow for overrange and underrange capability in unipolar mode, the transfer function of the MAX15500/MAX15501 is offset such that when the voltage at AIN is 5% of full scale, I_{OUT} is 0mA and V_{OUT} is 0V. Once V_{AIN} attains full scale, V_{OUT} or I_{OUT} becomes full scale +5% or +20% depending on the state of FSMODE. The devices are protected against overcurrent and short-circuit conditions when OUT goes to ground or a voltage up to ±32.5V. The devices also monitor for overtemperature and supply brownout conditions. The supply brownout threshold is programmable between ±10V and ±24V in 2V increments.

The MAX15500/MAX15501 are programmed through an SPI interface with daisy-chain capability. A device ready logic output ($\overline{READY}$) and two device select inputs ($\overline{CS1}$ and $\overline{CS2}$) facilitate a daisy-chain arrangement for multiple device applications. The MAX15500/MAX15501 provide extensive error reporting of short-circuit, open-circuit, brownout, and overtemperature conditions through the SPI interface and an additional open-drain interrupt output ($\overline{ERROR}$). The MAX15500/MAX15501 include an analog 0 to 3V output (MON) to monitor the load condition at OUT.

Analog Section

The MAX15500/MAX15501 support two output modes: current and voltage. Each mode has different full-scale output values depending on the state of FSMODE as detailed in Table 1 through Table 4 and Figures 1 and 2. Use the device configuration register in Table 6 to select the desired voltage or current output range.

Startup

During startup, the MAX15500/MAX15501 output is set to zero and all register bits are set to zero. The devices remain in standby mode until they are configured through the SPI interface.

Input Voltage Range

The input voltage full-scale level is selectable between 2.5V and 4.096V using logic input FSSEL. The MAX15500 is specified for a 0 to 4.096V input voltage range, while the MAX15501 is specified for a 0 to 2.500V input voltage range. Connect FSSEL to DVDD to set the input range to 0 to 4.096V for the MAX15500. Connect FSSEL to DGND to set the input range to 0 to 2.500V for the MAX15501.

Table 1. Output Values for FSMODE = DVDD, Unipolar 5% Overrange

OUTPUT RANGE	OUTPUT VALUES	
	V_{AIN} = 5%FS	V_{AIN} = FS
0 to 20mA (4mA to 20mA)	0mA	21mA
0 to 5V	0V	5.25V
0 to 10V	0V	10.5V

Table 2. Output Values for FSMODE = DGND, Unipolar 20% Overrange

OUTPUT RANGE	OUTPUT VALUES	
	V_{AIN} = 5%FS	V_{AIN} = FS
0 to 20mA (4mA to 20mA)	0mA	24mA
0 to 5V	0V	6V
0 to 10V	0V	12V

Table 3. Output Values for FSMODE = DVDD, Bipolar 5% Overrange

OUTPUT RANGE	OUTPUT VALUES	
	V_{AIN} = 0V	V_{AIN} = FS
±20mA	-21mA	+21mA
±10V	-10.5V	+10.5V

Table 4. Output Values for FSMODE = DGND, Bipolar 20% Overrange

OUTPUT RANGE	OUTPUT VALUES	
	V_{AIN} = 0V	V_{AIN} = FS
±20mA	-24mA	+24mA
±10V	-12V	+12V

Output Monitor

The MON output provides an analog voltage signal proportional to the output voltage in current mode and proportional to the output current in voltage mode. Use this signal to measure the system load presented to the output. The full-scale signal on MON is 3V with a typical accuracy of 10%. The signal range is typically 1.5V to 3V in unipolar mode and 0 to 3V in bipolar mode.

In current mode, the MAX15500/MAX15501 program I_{OUT} and monitor the voltage at SENSERN.

$$V_{MON} = 1.425V + (V_{SENSERN}/20)$$

$$R_{LOAD} = ((V_{MON} - 1.425V) \times 20)/I_{OUT(PROGRAMMED)}$$

In voltage mode, the MAX15500/MAX15501 program V_{OUT} and monitor I_{OUT}.

$$V_{MON} = 1.521V + 62.4 \times I_{LOAD}$$

$$R_{LOAD} = V_{OUT(PROGRAMMED)}/((V_{MON} - 1.521V)/62.4)$$

Error Handling

Many industrial control systems require error detection and handling. The devices provide extensive error status reporting. An open-drain interrupt flag output, $\overline{ERROR}$, pulls low when an error condition is detected. An error register stores the error source. Reading the error register once resets the $\overline{ERROR}$ pin but not the error register itself, allowing the system to determine the source of the error and take steps to fix the error condition. After the error condition has been fixed, read the error register for the second time to allow the device to clear the error register. Read the error register for the third time to verify if the error register has been cleared. If another error occurs after the first read, $\overline{ERROR}$ goes low again. More information on reading and clearing the error register is described in the *SPI Interface* section.

When an output short-circuit or output open-load error occurs and disappears before the error register is read, the intermittent bit is set in the error register. The intermittent bit does not assert for brownout and overtemperature error conditions. The MAX15500/MAX15501 and MAX15500K/MAX15501K offer different error handling for open circuits and short circuits. See the individual sections, Figure 11a, and Figure 11b for more details.

Error Conditions

Output Short Circuit

The output short-circuit error bit asserts when the output current exceeds 30mA (typ) for longer than 260ms. In current mode, this error occurs when the sense resistor is shorted and the sense voltage is not equal to 0V. In voltage mode, this error occurs when the load is shorted to the supply or ground. The short-circuit error activates the intermittent bit in the error register if the error goes away before the error register is read.

The MAX15500/MAX15501 only asserts the short-circuit flag when a short is detected and an open circuit is not detected.

Output Short-Circuit: Voltage Mode Only

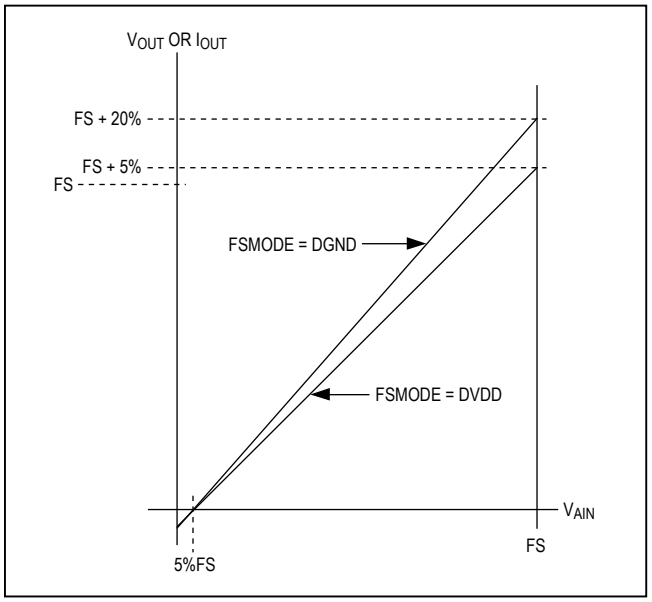


Figure 1. Unipolar Transfer Function

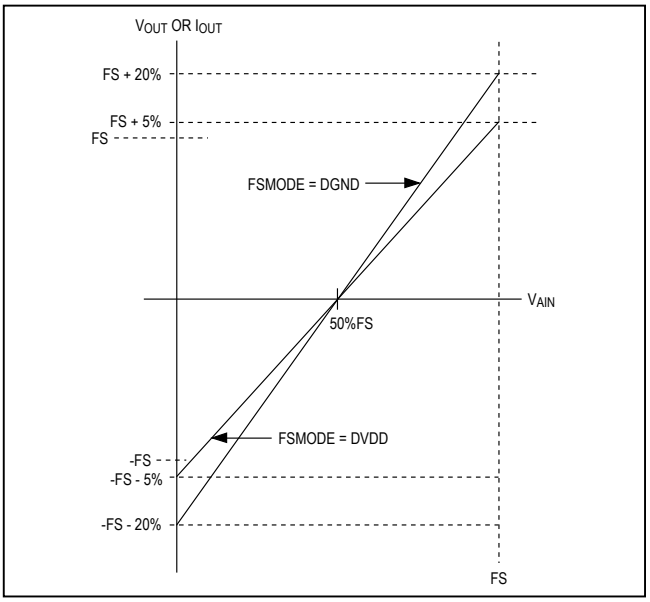


Figure 2. Bipolar Transfer Function

(MAX15500K/MAX15501K)

The output short-circuit error bit asserts when the output current exceeds 30mA (typ) for longer than 260ms in voltage mode only. This error occurs when the load is shorted to the supply or ground. The short-circuit error activates the intermittent bit in the error register if the error goes away before the error register is read.

Output Open Load (MAX15500/MAX15501)

The open-circuit error bit activates when VOUT is within 30mV of AVDDO or AVSSO and there is no short-circuit current in current mode for longer than 260ms. This error activates the intermittent bit in the error register if the error goes away before the error register is read.

The MAX15500/MAX15501 open-circuit flag is active when both a short circuit and open circuit are detected. The MAX15500/MAX15501 does not flag open circuit when the load current is between -3.5mA (typ) to +3.5mA (typ). Figure 11a shows the full range of the open circuit detection range and Figure 11b offers a zoomed in view. The MAX15500/MAX15501 are shown in the red lines.

Output Open Load (MAX15500K/MAX15501K)

The open-circuit error bit activates when VOUT is within 30mV of AVDDO or AVSSO for longer than 260ms. This error activates the intermittent bit in the error register if the error goes away before the error register is read.

The MAX15500K/MAX15501K does not flag open circuit when the load current is between -0.5mA (typ) to +0.5mA (typ). Figure 11a shows the full range of the open circuit detection range and Figure 11b offers a zoomed in view. The MAX15500K/MAX15501K are shown in the green lines.

Internal Overtemperature

The MAX15500/MAX15501 enter standby mode if the die temperature exceeds +150°C and the overtemperature protection is enabled as shown in Table 6. When the die temperature cools down below +140°C, the error register must be read back twice to resume normal operation. The devices provide a 10°C hysteresis. The MAX15500/MAX15501 and MAX15500K/MAX15501K all trigger the overtemperature ERROR flag in the same manner.

Brownout

The brownout-error bit activates when the supply voltage (V_{AVDD} or V_{AVSS}) falls below the brownout threshold. The threshold is programmable between ±10V to ±24V in 2V steps. See Table 6 for details. The MAX15500/MAX15501 provide a 2% hysteresis for the brownout threshold. The accuracy of the threshold is typically within 10%. During power-up, $\overline{ERROR}$ can go low and the brownout register is set. Users need to read out the error register twice to clear all the error register bits and reset $\overline{ERROR}$ to high. The MAX15500/MAX15501 and MAX15500K/MAX15501K all trigger the overtemperature ERROR flag in the same manner.

Output Protection

The MAX15500/MAX15501 supply inputs (AVDD, AVDDO, AVSS, and AVSSO) and sense inputs (SENSERN, SENSERP, SENSEVN, and SENSEVP) are protected against voltages up to ±35V with respect to AGND. See the *Typical Operating Circuit/Functional Diagram* for the recommended supply-voltage connection.

SPI Interface

Standard SPI Implementation

The MAX15500/MAX15501 SPI interface supports daisychaining. Multiple MAX15500/MAX15501 devices can be controlled from a single 4-wire SPI interface. The MAX15500/MAX15501 feature dual $\overline{CS_}$ inputs and an added digital output, $\overline{READY}$, that signals when the devices finish processing the SPI frame. $\overline{CS1}$ and $\overline{CS2}$ are internally OR-ed. Pull both $\overline{CS1}$ and $\overline{CS2}$ to logic-low to activate the MAX15500/MAX15501. For a daisy-chained application, connect the $\overline{CS1}$ input of all of the devices in the chain to the $\overline{CS}$ driver of the microcontroller. Connect the $\overline{CS2}$ input of the first device to ground or to the $\overline{CS}$ driver of the microcontroller. Connect $\overline{CS2}$ of the remaining devices to the $\overline{READY}$ output of the preceding device in the chain. The $\overline{READY}$ output of the last device in the chain indicates when all slave devices in the chain are configured. Connect the $\overline{READY}$ output of the last device in the chain to the microcontroller. Use the open-drain $\overline{ERROR}$ output as a wired-OR interrupt. See Figures 3 to 6.

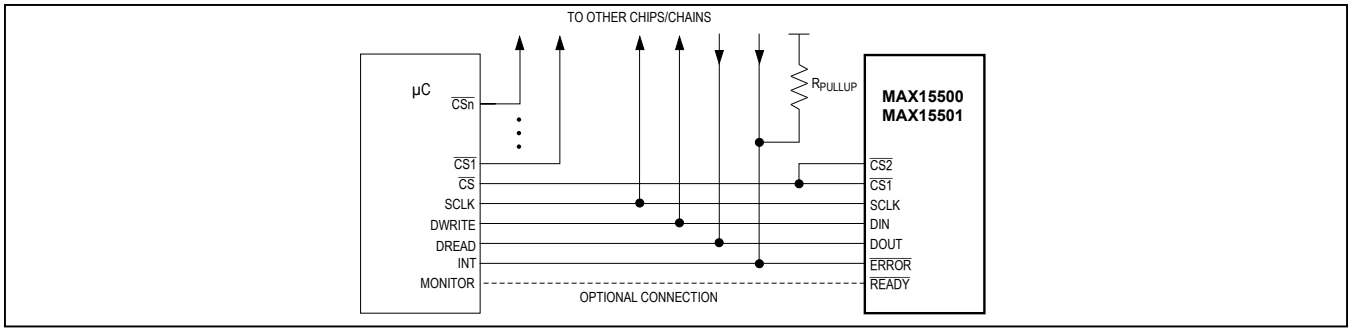


Figure 3. Single Connection (Compatible with Standard SPI)

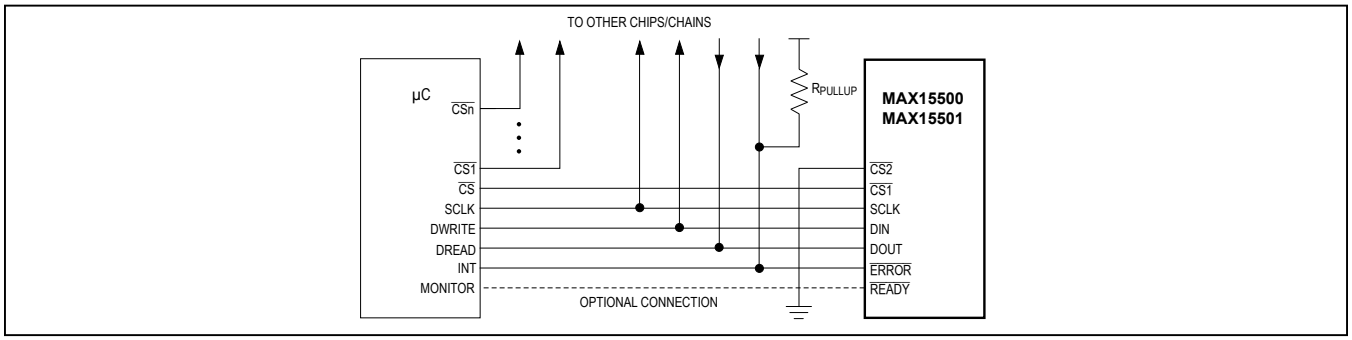


Figure 4. Alternate Single Connection (Compatible with Standard SPI)

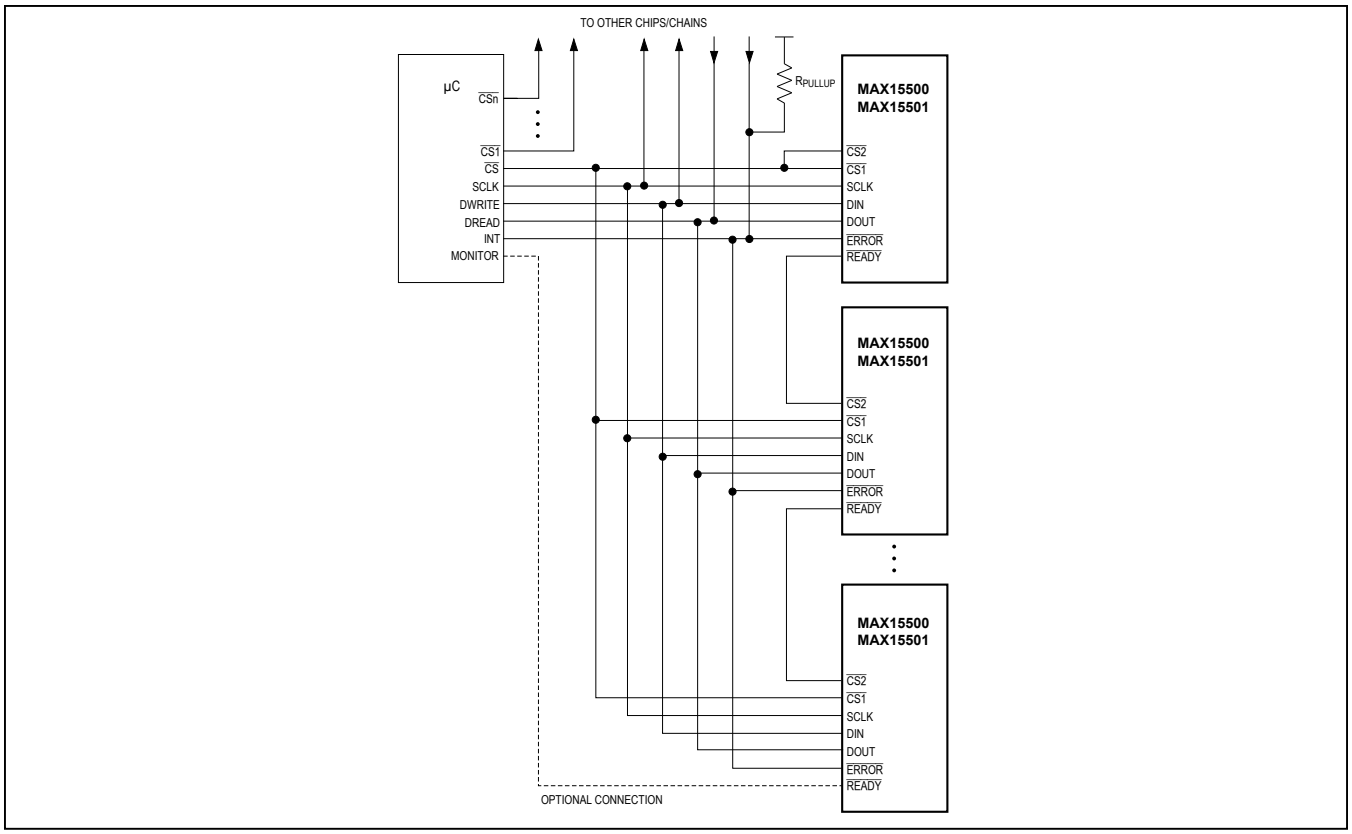


Figure 5. Daisy-Chain Connection (Compatible with Standard SPI)

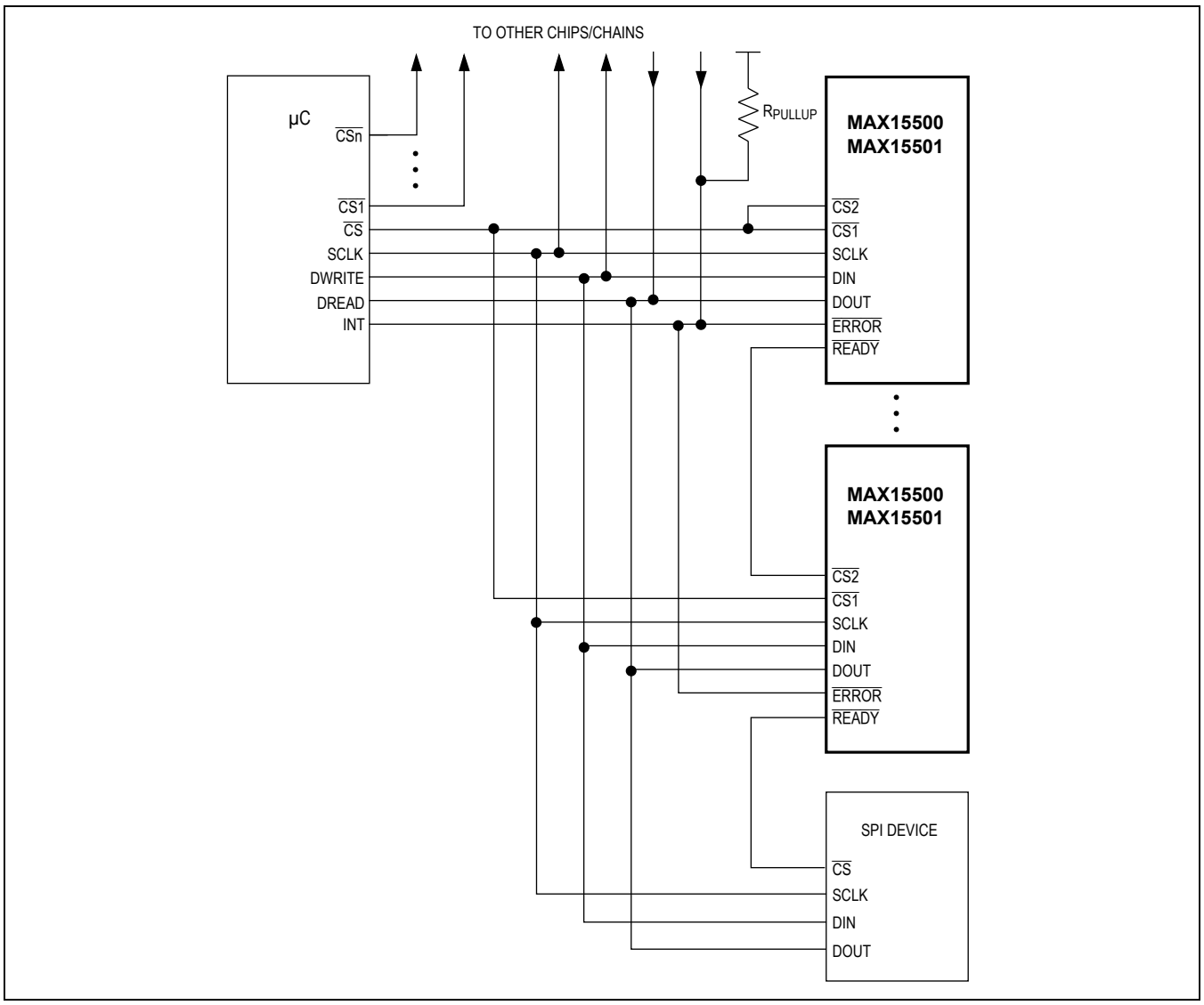


Figure 6. Daisy-Chain Terminating (Compatible with Standard SPI)

Modified SPI Interface Description

The SCLK, DIN, and DOUT of the MAX15500/MAX15501 assume standard SPI functionality. While the basic function of the MAX15500/MAX15501 $\overline{CS_}$ inputs is similar to the standard SPI interface protocol, the management of the $\overline{CS_}$ input within the chain is modified. When both $\overline{CS_}$ inputs are low, the MAX15500/MAX15501 assume control of the DOUT line and continue to control the line until the data frame is finished and $\overline{READY}$ goes low (Figure 9). Once a complete frame is processed and the $\overline{READY}$ signal is issued, the devices do not accept any data from DIN, until either $\overline{CS1}$ or $\overline{CS2}$ rises and returns low. A new communication cycle is initiated by a subsequent falling edge on $\overline{CS1}$ or $\overline{CS2}$. When either $\overline{CS1}$ or $\overline{CS2}$ is high, the MAX15500/MAX15501 SPI interface deactivates, DOUT returns to a high-impedance mode, $\overline{READY}$ (if active) clears, and any partial frames not yet processed are ignored.

$\overline{READY}$ asserts once a valid frame is processed allowing the next device in the chain to begin processing the subsequent frame. A valid frame consists of 16 SCLK cycles following the falling edge of $\overline{CS_}$. Once $\overline{READY}$ asserts, it remains asserted until either $\overline{CS_}$ rises, completing the programming of the chain.

The MAX15500/MAX15501 relinquish control of DOUT once the devices process the frame(s). DOUT remains high impedance when the SPI interface continues to hold $\overline{CS_}$ low beyond the required frame(s). Install a pullup/puldown resistor at the DOUT line to maintain the desired state when DOUT goes high impedance.

Single Device SPI Connection

For applications using a single MAX15500 or MAX15501, connect both $\overline{CS1}$ and $\overline{CS2}$ inputs to the device-select driver of the host microcontroller. Alternatively, connect one of the $\overline{CS_}$ inputs to the device-select driver of the host microcontroller and the other $\overline{CS_}$ to DGND. Both methods allow standard SPI interface operation. See Figures 3 and 4.

Daisy-Chain SPI Connection

The MAX15500/MAX15501-modified SPI interface allows a single SPI master to drive multiple devices in a daisy-chained configuration, saving additional SPI channels for other devices and saving cost in isolated applications.

Figure 5 shows multiple MAX15500/MAX15501 devices connected in a daisy chain. The chain behaves as a single device to the microcontroller in terms of timing with an expanded instruction frame requiring 16 SCLK cycles per device for complete programming. No timing parameters are affected by the $\overline{READY}$ propagation as all devices connect to the microcontroller chip-select through the $\overline{CS1}$ inputs.

A chain of MAX15500/MAX15501 devices can be terminated with any standard SPI-compatible single device without a $\overline{READY}$ output. The MAX15500/MAX15501 portion of the chain continues to display timing parameters comparable to a single device. See Figure 6.

When using the MAX15500/MAX15501 with mixed chains, the connections could require some modification to accommodate the interfaces of the additional devices in the chain. Construct the daisy chain as shown in Figure 7 when using devices with similar $\overline{READY}$ outputs but without dual $\overline{CS_}$ inputs such as the MAX5134 quad 16-bit DAC. The chain is subject to timing relaxation for parameters given with respect to $\overline{CS_}$ rising edges to accommodate $\overline{READY}$ propagation to and through consecutive MAX5134 devices.

The chain can begin and terminate with either device type. Each MAX5134 or MAX15500/MAX15501 device in the chain could be replaced by a subchain of similar devices. If the chain is terminated with a standard SPI device, omit the optional connection from $\overline{READY}$ to the monitor input on the microcontroller. The MAX15500/MAX15501 portion of the chain continues to display timing parameters comparable to a single device.

SPI Digital Specifications and Waveforms

Figures 8, 9, and 10 show the operation of the modified SPI interface. The minimum programming operation typically used in single device applications is 16 SCLK periods, the minimum for a valid frame. This cycle can also represent the operation of the final device in a chain.

The extended programming operation is typically used for devices in daisy-chained applications. In this case, $\overline{READY}$ drives the chip-select input of the subsequent device in the chain. The next device in the chain begins its active frame on the 16th SCLK falling edge in response to $\overline{READY}$ falling (latching DIN[13] on the 17th SCLK falling edge, if present).

Aborted SPI Operations

Driving a $\overline{CS_}$ input high before a valid SPI frame is transmitted to the device can cause an erroneous command. Avoid driving $\overline{CS_}$ high before a valid SPI frame is transmitted to the device. See Figures 9 and 10 for valid SPI operation timing.

SPI Operation Definitions

Input data bits DIN[13:11] represent the SPI command address while DIN[9:0] represent the data written to or read from the command address. The command address directs subsequent input data to the proper internal register for setting up the behavior of the device and selects the correct status data for readback through DOUT. Command address 0h points to a no-op command and does not impact the operation of the device. DOUT is active during this operation and reads back 00h. Command address 1h points to the configuration register used to program the MAX15500/MAX15501. Device configuration takes effect following the 14th SCLK falling edge. DOUT activates and remains low during this operation. Command addresses 4h and 5h point to readback commands of the MAX15500/MAX15501. Readback commands provide configuration and error register status through DOUT[9:0] and do not affect the internal operation of the device. Command addresses 2h, 3h, 6h, and 7h are reserved for future use. Table 5 shows the list of commands.

Device Configuration Operation

Table 6 shows the function of each bit written to the configuration register 1h. Table 7 shows the data readback registers.

Readback Operations

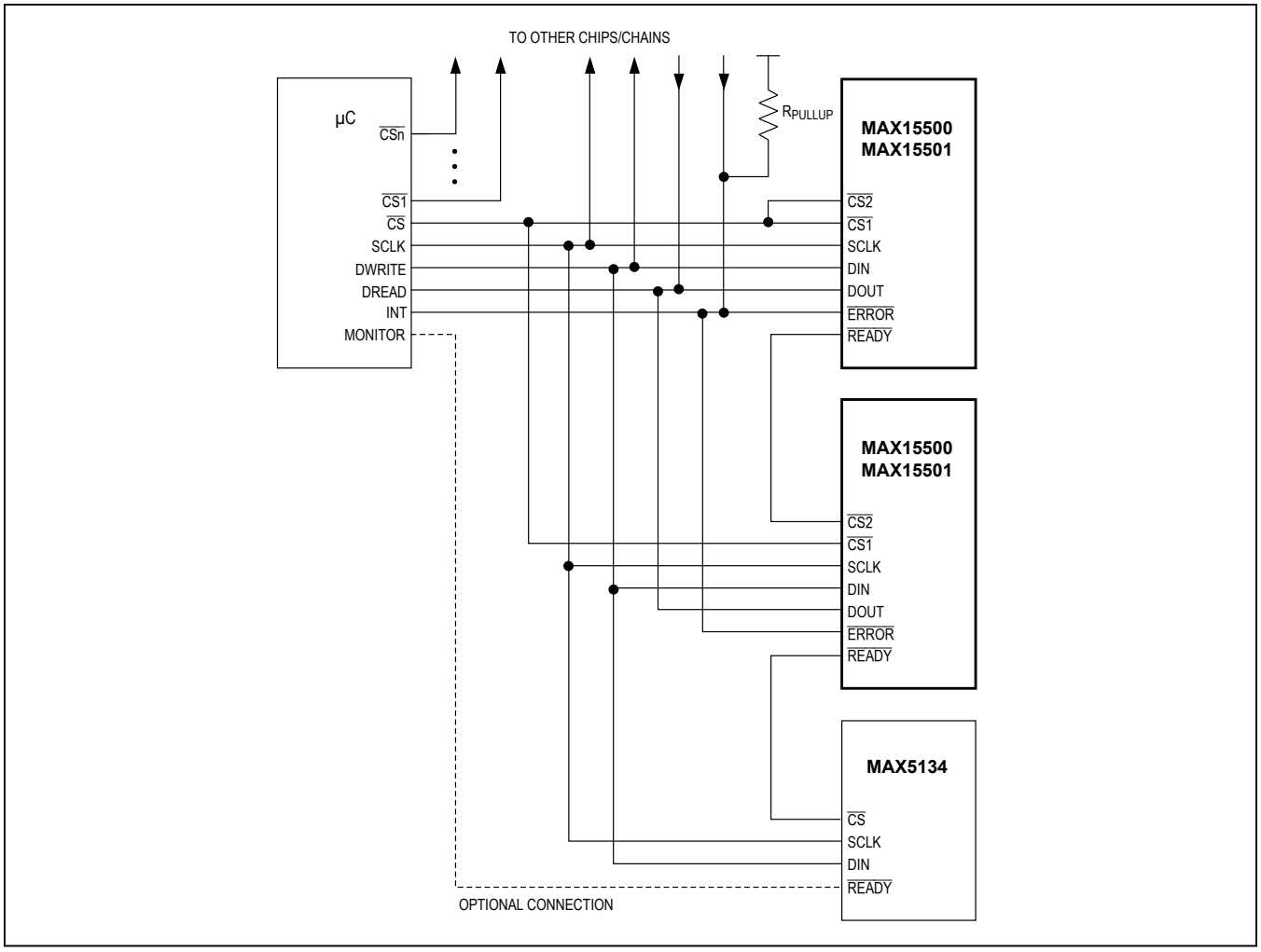


Figure 7. Mixed MAX15500/MAX15501 and MAX5134 Daisy-Chain Connections

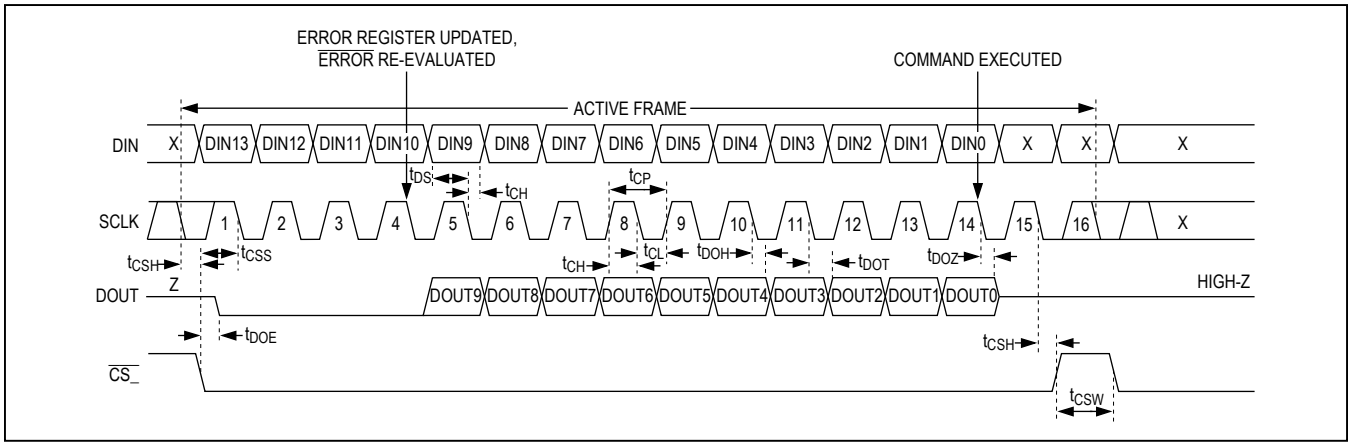


Figure 8. Minimum SPI Programming Operation (Typically for Single Device Applications)

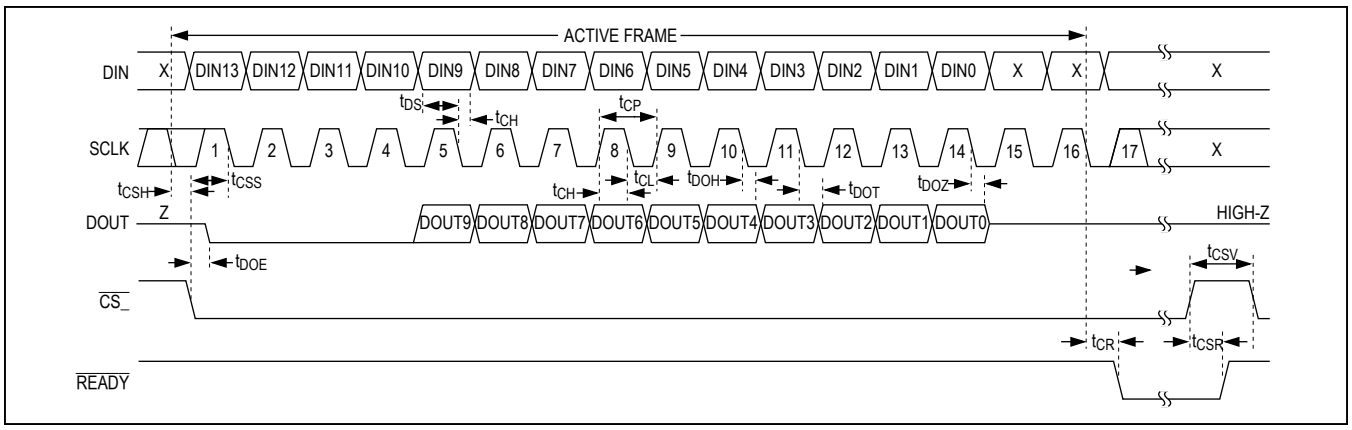


Figure 9. Extended SPI Programming Operation (Daisy-Chained Applications)

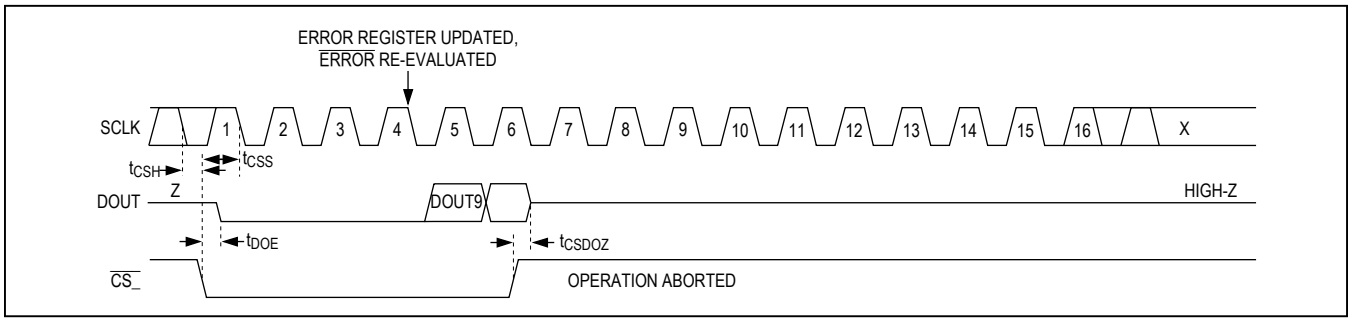


Figure 10. Aborted SPI Programming Operation (Invalid, Showing t_{CSDOZ} and Internal Activity)

Write to the command addresses 4h or 5h to read back the configuration register data or the internal error information through DOUT[9:0]. For error readback operations, each bit corresponds to a specific error condition, with multiple bits indicating multiple error conditions present.

Intermittent Errors

An intermittent error is defined as an error that is detected and is resolved before the error register is read back. When the error is resolved without intervention, the intermittent bit (bit 9) is set. The output short-circuit and output open-load errors trigger the intermittent bit. Internal over-temperature and supply voltage brownout do not trigger the intermittent bit.

Error Reporting Applications

The $\overline{ERROR}$ output is typically connected to an interrupt input of the system microcontroller. The MAX15500/MAX15501 only issue an interrupt when a new error condition is detected. The devices do not issue interrupts when errors (either individual or multiple) are resolved or when already reported errors persist. The system microcontroller resets $\overline{ERROR}$ when the system microcontroller reads back the error register. $\overline{ERROR}$ does not assert again unless a different error occurs.

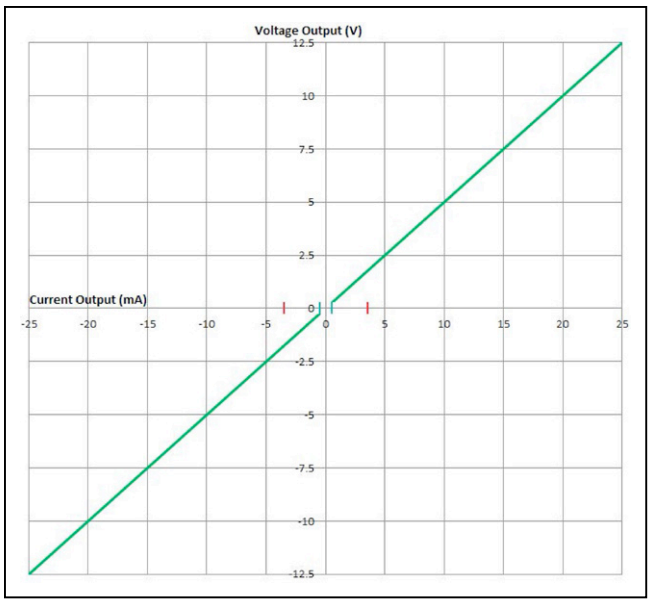


Figure 11a. Diagram Showing the MAX15500/MAX15501 "Plain" (Red) and the MAX15500K/MAX15501K (Teal) Open-Circuit Detection Windows

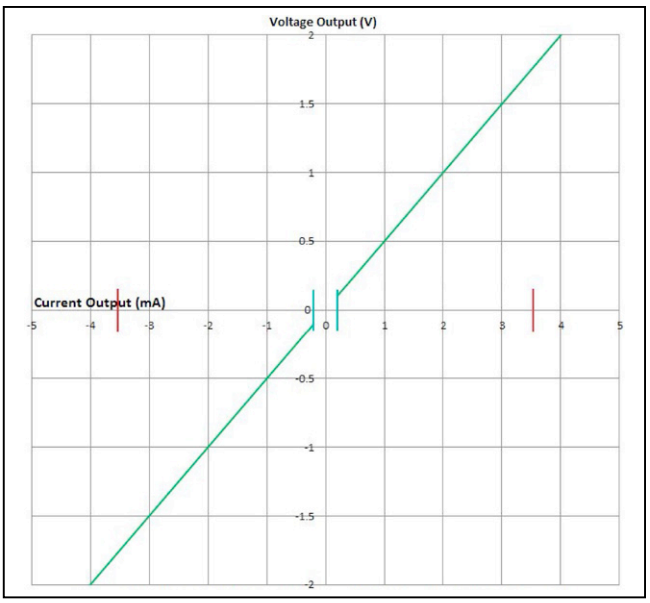


Figure 11b. Zoomed In Diagram Showing the MAX15500/MAX15501 "Plain" (Red) and the MAX15500K/MAX15501K (Teal) Open-Circuit Detection Windows

Table 5. SPI Commands

COMMAND ADDRESS DIN[13:11]	NAME	DESCRIPTION
000	No-op	No operation.
001	Write configuration	Write device configuration register. See Table 6 for details.
010	Reserved	Reserved, no operation.
011	Reserved	Reserved, no operation.
100	Read error	Read error register status. See Table 7 for details.
101	Read configuration	Read device configuration register. See Table 6 for details.
110	Reserved	Reserved, no operation.
111	Reserved	Reserved, no operation.

Table 6. Configuration Register

LOCATION	FUNCTION	DESCRIPTION
DIN[9:7]	Mode[2:0]	Sets device operating mode. 000 Mode[0]: Standby 001 Mode[1]: Bipolar current: ±20mA 010 Mode[2]: Unipolar current: 0 to 20mA 011 Mode[3]: Unipolar current: 4mA to 20mA 100 Mode[4]: Standby 101 Mode[5]: Bipolar voltage: ±10V 110 Mode[6]: Unipolar voltage: 0 to 10V 111 Mode[7]: Unipolar voltage: 0 to 5V
DIN[6:4]	VBOTH[2:0]	Sets supply voltage brownout threshold for error reporting. 000: ±10V 001: ±12V 010: ±14V 011: ±16V 100: ±18V 101: ±20V 110: ±22V 111: ±24V
DIN[3]	Thermal shutdown	0 = thermal protection off. 1 = thermal protection on.
DIN[10], DIN[2:0]	—	Reserved

Note: *Modes 2h and 3h are functionally identical.*

Table 7. Readback Operations and Formatting

DOUT BITS	DESCRIPTION
COMMAND ADDRESS DIN[13:11] = 101. READBACK DEVICE CONFIGURATION REGISTER	
DOUT[9:0]	See configuration register details in Table 6.
COMMAND ADDRESS DIN[13:11] = 100. READBACK ERROR REGISTER	
DOUT[9]	Output Intermittent Fault. For details, see the *Error Handling* section.
DOUT[8]	Output Short Circuit. Output short circuit. In the MAX15500/MAX15501, this bit asserts when IOUT > 30mA in voltage and current modes for longer than 260ms. In the MAX15500K/MAX15501K, this bit asserts when Iout > 30mA for longer than 260ms (in voltage mode only).
DOUT[7]	Output Open Load. In the MAX15500/MAX15501, this bit asserts when VOUT is within 30mV of AVDDO or AVSSO and there is no short-circuit condition for longer than 260ms. In the MAX15500K/MAX15501K, the output open load bit asserts when V_{OUT} is within 30mV of AV_{DDO} or AV_{SSO} for longer than 260ms.
DOUT[6]	Internal Overtemperature. This bit asserts when the die temperature exceeds +150°C.
DOUT[5]	Supply Brownout. This bit asserts when either supply has entered the brownout limits. See Table 6 for details.
DOUT[4:0]	Reserved

Since the MAX15500/MAX15501 do not use a continuous clock signal, the SPI read cycles are used to cycle the error detection and reporting logic. Continue to poll the device until the error readback reports an all clear status when resolving single or multiple errors. See below for examples of typical error handling situations and the effects of the SPI read operations.

1) Error resolved by the system.
   a) The MAX15500/MAX15501 detect an error condition and $\overline{\text{ERROR}}$ asserts.
   b) The host controller reads the error register for the first time. This has the effect of resetting $\overline{\text{ERROR}}$. The data indicates to the host processor which error is active.
   c) The host processor resolves the error successfully.
   d) The host processor reads the error register for the second time. The data still shows that the error is present as the error persisted for some time after step b and before step c. If the error is either an open load or short circuit, the intermittent bit is set. An overtemperature or a brownout does not set the intermittent bit. Reading the register a second time resets the register.
   e) The host reads the error register for a third time. The data now shows the error is resolved and future occurrences of this error will trigger $\overline{\text{ERROR}}$ assertion.
2) Error resolved before the host processor reads error register.
   a) The MAX15500/MAX15501 detect an error condition and $\overline{\text{ERROR}}$ asserts, but the error resolves itself.
   b) The host controller reads the error register for the first time resetting $\overline{\text{ERROR}}$. The data indicates to the host processor which error is active. The data also indicates to the host that the error has been resolved since the intermittent bit is set.
   c) The host processor reads the error register for the second time. The data still shows that the error is active. If the error is for an output fault, the data also indicates to the host that the error has been resolved since the intermittent bit is set. Reading the register a second time resets the register.
3) An error that cannot be resolved.
   a) The MAX15500/MAX15501 detect an error condition and $\overline{\text{ERROR}}$ asserts.
   b) The host controller reads the error register for the first time and resets $\overline{\text{ERROR}}$. The data indicates to the host processor which error is active.
   c) The host processor takes action to resolve the error unsuccessfully.
   d) The host processor reads the error register for the second time. The data still shows that the error is present.
   e) The host processor reads the error for the third time. The data show the error to be unresolved. $\overline{\text{ERROR}}$ does not respond to the same error until the error is resolved and reported. $\overline{\text{ERROR}}$ asserts if different errors occur.

Applications Information

Setting the Output Gain in Current Mode

In current mode, there is approximately 1.0V across the current-sensing resistors at full scale. The current sensing resistor sets the gain and is calculated as follows:

$$R_{SENSE} = VS_{ENSE_FS}/I_{MAX}$$

where V_{SENSE_FS} is the full-scale voltage across the sense resistor.

See Table 8 for values of V_{SENSE_FS}.

Output Gain in Voltage Mode

The output gain in voltage mode is fixed as shown in Table 9.

Selection of the Compensation Capacitor (CCOMP)

Use Table 10 to select the compensation capacitor.

Layout Considerations

In the current-mode application, use Kelvin and a short connection from SENSERN and SENSERP to the R_{SENSE} terminals to minimize gain-error drift. Balance and minimize all analog input traces for optimum performance.

Table 8. Recommended Current Setting Components

V_{REFIN} (V)	OVERRANGE (%)	BIPOLAR/ UNIPOLAR	MODE	V_{SENSE_FS} (V)	R_{SENSE} (Ω)	I_{OUT} (mA)	IDEAL GAIN	IDEAL TRANSFER FUNCTION
4.096	+20	Unipolar	2	1.02144	42.2	24.205	0.2625/42.2	$I_{OUT} = 0.2625 \times (V_{AIN} - 0.05 \times V_{REFIN})/42.2$
		Bipolar	1	±1.024	42.2	±24.27	0.5/42.2	$I_{OUT} = 0.5 \times (V_{AIN} - 0.5 \times V_{REFIN})/42.2$
	+5	Unipolar	2	1.02144	48.7	20.97	0.2625/48.7	$I_{OUT} = 0.2625 \times (V_{AIN} - 0.05 \times V_{REFIN})/48.7$
		Bipolar	1	±1.024	48.7	±21.03	0.5/48.7	$I_{OUT} = 0.5 \times (V_{AIN} - 0.5 \times V_{REFIN})/48.7$
2.500	+20	Unipolar	2	1.009375	41.2	24.5	0.425/41.2	$I_{OUT} = 0.425 \times (V_{AIN} - 0.05 \times V_{REFIN})/41.2$
		Bipolar	1	±1	41.2	±24.27	0.8/41.2	$I_{OUT} = 0.8 \times (V_{AIN} - 0.5 \times V_{REFIN})/41.2$
	+5	Unipolar	2	1.009375	47.5	21.25	0.425/47.5	$I_{OUT} = 0.425 \times (V_{AIN} - 0.05 \times V_{REFIN})/47.5$
		Bipolar	1	±1	47.5	±21.05	0.8/47.5	$I_{OUT} = 0.8 \times (V_{AIN} - 0.5 \times V_{REFIN})/47.5$

Table 9. Full-Scale Output Voltages

V_{REFIN} (V)	OVERRANGE (%)	BIPOLAR/ UNIPOLAR	MODE	IDEAL GAIN	IDEAL TRANSFER FUNCTION	IDEAL V_{OUT} (V)
4.096	+20	Unipolar	7	1.5625	$V_{OUT} = 1.5625 \times (V_{AIN} - 0.05 \times V_{REFIN})$	6.08
			6	3.125	$V_{OUT} = 3.125 \times (V_{AIN} - 0.05 \times V_{REFIN})$	12.16
		Bipolar	5	6.0	$V_{OUT} = 6.0 \times (V_{AIN} - 0.5 \times V_{REFIN})$	±12.288
	+5	Unipolar	7	1.375	$V_{OUT} = 1.375 \times (V_{AIN} - 0.05 \times V_{REFIN})$	5.3504
			6	2.75	$V_{OUT} = 2.75 \times (V_{AIN} - 0.05 \times V_{REFIN})$	10.7008
		Bipolar	5	5.25	$V_{OUT} = 5.25 \times (V_{AIN} - 0.5 \times V_{REFIN})$	±10.752
2.500	+20	Unipolar	7	2.5125	$V_{OUT} = 2.5125 \times (V_{AIN} - 0.05 \times V_{REFIN})$	5.96719
			6	5.0625	$V_{OUT} = 5.0625 \times (V_{AIN} - 0.05 \times V_{REFIN})$	12.0234
		Bipolar	5	9.6	$V_{OUT} = 9.6 \times (V_{AIN} - 0.5 \times V_{REFIN})$	±12
	+5	Unipolar	7	2.175	$V_{OUT} = 2.175 \times (V_{AIN} - 0.05 \times V_{REFIN})$	5.16563
			6	4.425	$V_{OUT} = 4.425 \times (V_{AIN} - 0.05 \times V_{REFIN})$	10.5094
		Bipolar	5	8.4	$V_{OUT} = 8.4 \times (V_{AIN} - 0.5 \times V_{REFIN})$	±10.5

Table 10. Recommended Compensation Capacitor for Various Load Conditions

MODE	C_L (F)	R_L (Ω)	L_L (H)	C_{COMP} (F)
Voltage	0 to 1n	1	0	0
Voltage	1n to 100n	1	0	1n
Voltage	100n to 1µ	1	0	2.2n
Voltage	1µ to 100µ	1	0	4.7n
Current	0 to 1n	20 to 750	0 to 20µ	0
Current	0 to 1n	20 to 750	20µ to 1m	2.2n
Current	0 to 1n	20 to 750	1m to 50m	100n
Current	1n to 100n	20 to 750	0 to 20µ	1n
Current	1n to 100n	20 to 750	20µ to 1m	2.2n
Current	1n to 100n	20 to 750	1m to 50m	100n
Current	100n to 1µ	20 to 750	0 to 20µ	2.2n
Current	100n to 1µ	20 to 750	20µ to 1m	2.2n
Current	100n to 1µ	20 to 750	1m to 50m	100n
Current	1µ to 100µ	20 to 750	0 to 20µ	2.2n
Current	1µ to 100µ	20 to 750	20µ to 1m	2.2n
Current	1µ to 100µ	20 to 750	1m to 50m	100n

C_L = Load capacitance.
R_L = Load resistance.
L_L = Load inductance.
C_{COMP} = Compensation capacitance.

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	PIN-PACKAGE	REFERENCE
MAX15500GTJ+	32 TQFN-EP*	+4.096V
MAX15500KGTJ+	32 TQFN-EP*	+4.096V
MAX15501GTJ+	32 TQFN-EP*	+2.5V
MAX15501KGTJ+	32 TQFN-EP*	+2.5V

Note: *All devices are specified over the -40°C to +105°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
SPI is a trademark of Motorola, Inc.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	2/11	Corrected description of DOUT pin in *Pin Description* section	13
2	10/15	Added new figures and text to Applications section and added “K” versions for added ERROR pin functionality.	1, 13, 17, 18, 23, 24
3	7/19	Added *Package Information*, removed old package section, and updated Table 10	2, 29

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