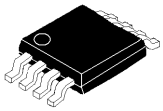
TS922, TS922A

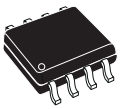
Rail-to-rail, high output current dual operational amplifier

Datasheet - production data

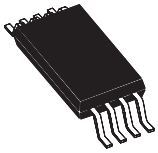
J
Flip-chip with backcoating



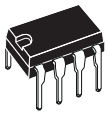
MiniSO8
(plastic micropackage)



D
SO8
(plastic micropackage)



P
TSSOP8
(thin shrink small outline package)



N
DIP8
(plastic package)

Features

- Rail-to-rail input and output
- Low noise: 9 nV/$\sqrt{Hz}$
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1 V/µs
- Operating from 2.7 to 12 V
- Low input offset voltage: 900 µV max. (TS922A)
- ESD internal protection: 2 kV
- Latch-up immunity
- Macromodel included in this specification
- Dual version available in Flip-chip package

Applications

- Headphone and servo amplifiers
- Sound cards, multimedia systems
- Line drivers, actuator drivers
- Mobile phones and portable equipment
- Instrumentation with low noise as key factor
- Piezoelectric speaker drivers

Description

TS922 and TS922A devices are rail-to-rail dual BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operation. These devices have high output currents which allow low-load impedances to be driven.

Very low noise, low distortion, low offset, and a high output current capability make these devices an excellent choice for high quality, low voltage, or battery operated audio systems.

The devices are stable for capacitive loads up to 500 pF.

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1 Pin diagrams

Figure 1. Pinout for Flip-chip package (top view)

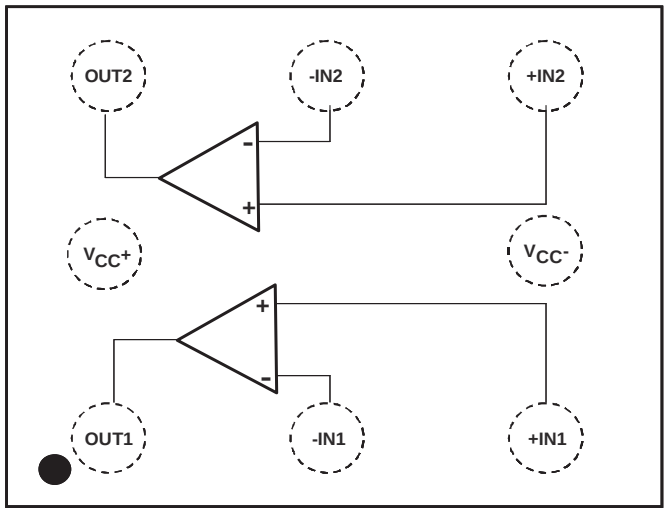
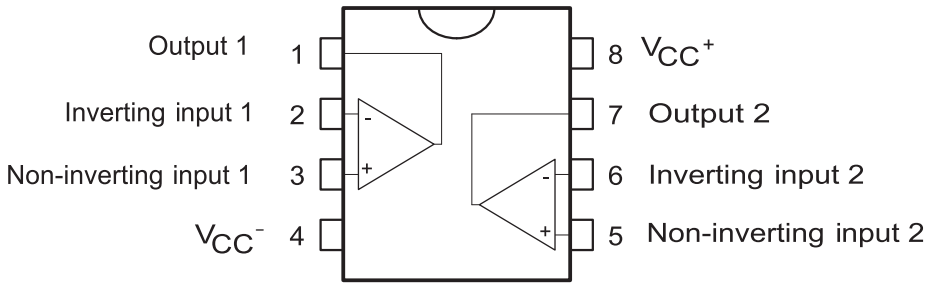


Figure 2. Pin connections for MiniSO8, SO8, TSSOP8, and DIP8 (top view)



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	14	V
V_{id}	Differential input voltage(2)	±1	
V_{in}	Input voltage(3)	V_{CC-} -0.3 to V_{CC+}+0.3	
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(4) Flip-chip SO8 TSSOP8	 90 125 120	°C/W
R_{thjc}	Thermal resistance junction to case(4) SO8 TSSOP8	 40 37	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(5) MM: machine model(6) CDM: charged device model(7)	2000 120 1500	V
	Output short-circuit duration	See note(8)	
	Latch-up immunity	200	mA
	Soldering temperature (10 s), leaded version Soldering temperature (10 s), unleaded version	250 260	°C

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal. If V_{id} > ±1 V, the maximum input current must not exceed ±1 mA. In this case (V_{id} > ±1 V), an input series resistor must be added to limit the input current.
3. Do not exceed 14 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These values are typical.
5. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of pin combinations with other pins floating.
7. Charged device model: all pins and plus package are charged together to the specified voltage and then discharged directly to ground.
8. There is no short-circuit protection inside the device: short-circuits from the output to V_{CC} can cause excessive heating. The maximum output current is approximately 80 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 12	V
V_{icm}	Common mode input voltage range	V_{CC-} -0.2 to V_{CC+} +0.2	
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. Electrical characteristics measured at V_{CC} = +3 V, V_{CC}- = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	TS922 TS922A TS922IJ (Flip-chip)			3 0.9 1.5	mV
		$T_{min} \le T_{amb} \le T_{max}$ TS922 TS922A TS922IJ (Flip-chip)			 5 1.8 2.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	$V_{out} = V_{CC}/2$ $T_{min} \le T_{amb} \le T_{max}$		1	30 30	nA
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$ $T_{min} \le T_{amb} \le T_{max}$		15	100 100	
V_{OH}	High level output voltage	R_L= 10 kΩ $T_{min} \le T_{amb} \le T_{max}$	2.90 2.90			V
		R_L = 600 Ω $T_{min} \le T_{amb} \le T_{max}$	2.87 2.87			
		R_L = 32 Ω		2.63		
V_{OL}	Low level output voltage	R_L= 10 kΩ $T_{min} \le T_{amb} \le T_{max}$			50 50	mV
		R_L = 600 Ω $T_{min} \le T_{amb} \le T_{max}$			100 100	
		R_L = 32 Ω		180		
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 2 V_{p-p} $T_{min} \le T_{amb} \le T_{max}$	70	200		V/mV
		R_L = 600 Ω, V_{out} = 2 V_{p-p} $T_{min} \le T_{amb} \le T_{max}$	15	35		
		R_L = 32 Ω, V_{out} = 2 V_{p-p}		16		
I_{CC}	Total supply current	No load, $V_{out} = V_{CC}/2$ $T_{min} \le T_{amb} \le T_{max}$		2	3 3.2	mA
GBP	Gain bandwidth product	R_L = 600 Ω		4		MHz
CMR	Common mode rejection ratio	V_{icm} = 0 to 3 V $T_{min} \le T_{amb} \le T_{max}$	60 56	80		dB
SVR	Supply voltage rejection ratio	V_{CC} = 2.7 to 3.3 V $T_{min} \le T_{amb} \le T_{max}$	60 60	85		
I_o	Output short-circuit current		50	80		mA
SR	Slew rate		0.7	1.3		V/µs

Table 3. Electrical characteristics measured at V_{CC} = +3 V, V_{CC}- = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ϕm	Phase margin at unit gain	R_L = 600 Ω, C_L = 100 pF		68		Degrees
G_m	Gain margin			12		dB
e_n	Equivalent input noise voltage	f = 1 kHz		9		$\frac{nV}{\sqrt{Hz}}$
THD	Total harmonic distortion	V_{out} = 2 V_{p-p}, f = 1 kHz, A_V = 1, R_L = 600 Ω		0.005		%
C_s	Channel separation			120		dB

Table 4. Electrical characteristics measured at V_{CC} = 5 V, V_{CC}- = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	TS922 TS922A TS922IJ (Flip-chip)			3 0.9 1.5	mV
		$T_{min} \le T_{amb} \le T_{max}$ TS922 TS922A TS922IJ (Flip-chip)			 5 1.8 2.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	$V_{out} = V_{CC}/2$ $T_{min} \le T_{amb} \le T_{max}$		1	30 30	nA
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$ $T_{min} \le T_{amb} \le T_{max}$		15	100 100	
V_{OH}	High level output voltage	R_L= 10 kΩ $T_{min} \le T_{amb} \le T_{max}$	4.9 4.9			V
		R_L = 600 Ω $T_{min} \le T_{amb} \le T_{max}$	4.85 4.85			
		R_L = 32 Ω		4.4		
V_{OL}	Low level output voltage	R_L= 10 kΩ $T_{min} \le T_{amb} \le T_{max}$			50 50	mV
		R_L = 600 Ω $T_{min} \le T_{amb} \le T_{max}$			120 120	
		R_L = 32 Ω		300		
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 2 V_{p-p} $T_{min} \le T_{amb} \le T_{max}$	70	200		V/mV
		R_L = 600 Ω, V_{out} = 2 V_{p-p} $T_{min} \le T_{amb} \le T_{max}$	20	35		
		R_L = 32 Ω, V_{out} = 2 V_{p-p}		16		
I_{cc}	Total supply current	No load, $V_{out} = V_{CC}/2$ $T_{min} \le T_{amb} \le T_{max}$		2	3 3.2	mA
GBP	Gain bandwidth product	R_L = 600 Ω		4		MHz
CMR	Common mode rejection ratio	V_{icm} = 0 to 5 V $T_{min} \le T_{amb} \le T_{max}$	60 56	80		dB
SVR	Supply voltage rejection ratio	V_{CC} = 4.5 to 5.5 V $T_{min} \le T_{amb} \le T_{max}$	60 60	85		
I_o	Output short-circuit current		50	80		mA
SR	Slew rate		0.7	1.3		V/µs
ϕm	Phase margin at unit gain	R_L = 600 Ω, C_L =100 pF		68		Degrees
G_m	Gain margin			12		dB
e_n	Equivalent input noise voltage	f = 1 kHz		9		$\frac{nV}{\sqrt{Hz}}$

Table 4. Electrical characteristics measured at V_{CC} = 5 V, V_{CC}- = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
THD	Total harmonic distortion	V_{out} = 2 V_{p-p}, f = 1 kHz, A_v = 1, R_L = 600 Ω		0.005		%
C_s	Channel separation			120		dB

Figure 3. Output short-circuit current vs. output voltage

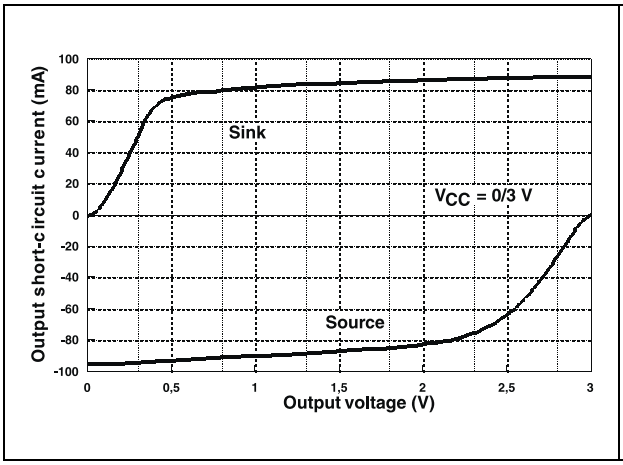


Figure 4. Total supply current vs. supply voltage

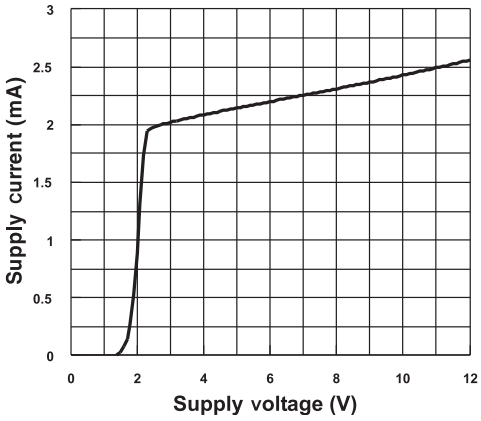


Figure 5. Voltage gain and phase vs. frequency

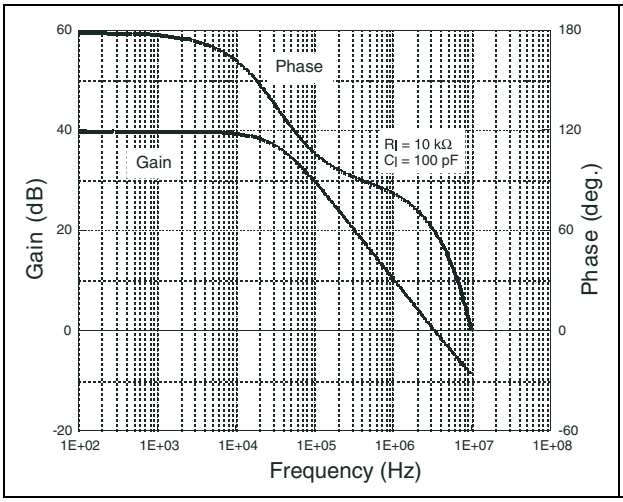


Figure 6. Equivalent input noise voltage vs. frequency

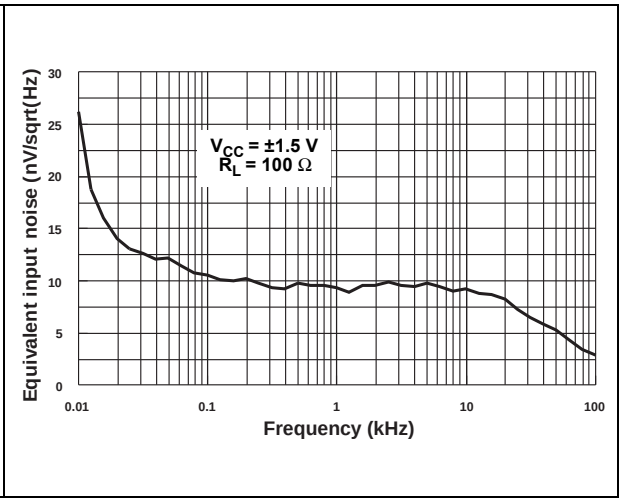


Figure 7. THD + noise vs. frequency (R_L = 2 kΩ, V_o = 10 Vpp, V_{CC} = ± 6 V)

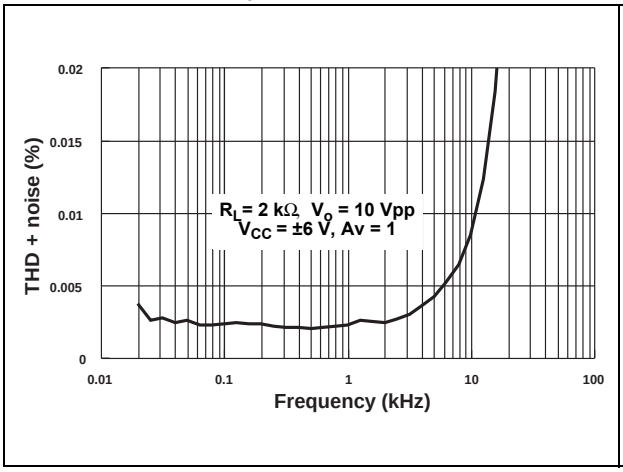


Figure 8. THD + noise vs. frequency (R_L = 32 Ω, V_o = 4 Vpp, V_{CC} = ± 2.5 V)

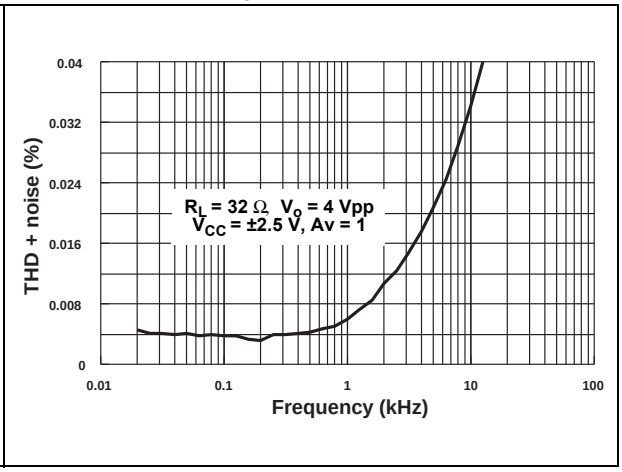


Figure 9. THD + noise vs. frequency (R_L = 32 Ω, V_o = 2 Vpp, V_{CC} = ± 1.5 V)

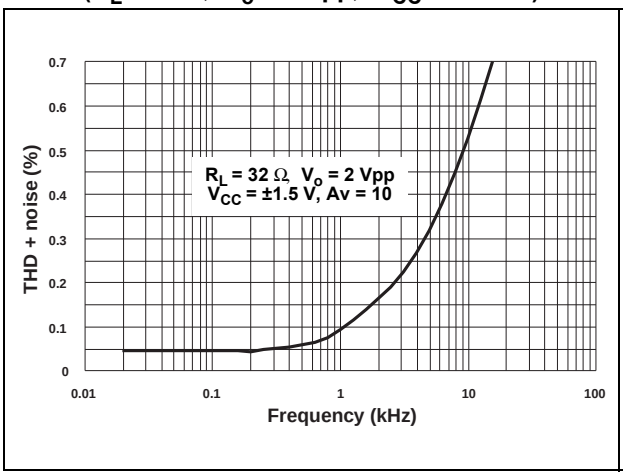


Figure 10. THD + noise vs. output voltage (R_L = 600 Ω, f = 1 kHz, V_{CC} = 0/3 V)

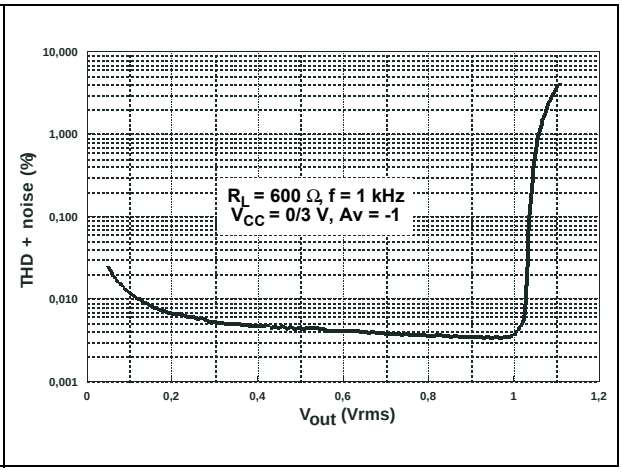


Figure 11. THD + noise vs. output voltage (R_L = 32 Ω, f = 1 kHz, V_{CC} = ± 1.5 V)

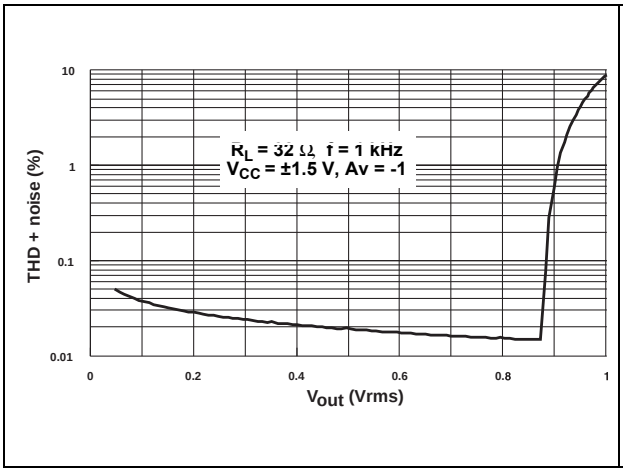


Figure 12. THD + noise vs. output voltage (R_L = 2 kΩ, f = 1 kHz, V_{CC} = ± 1.5 V)

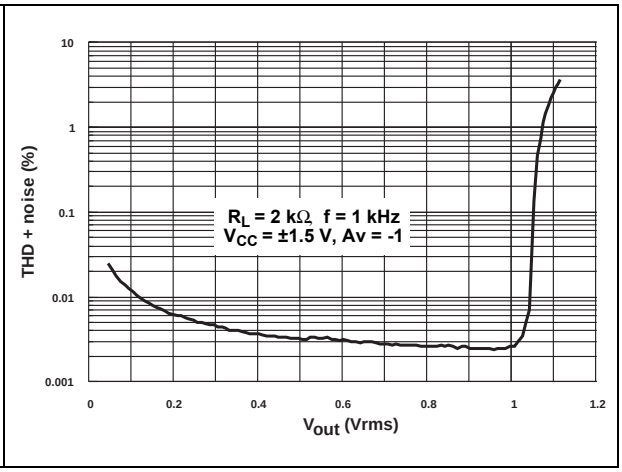
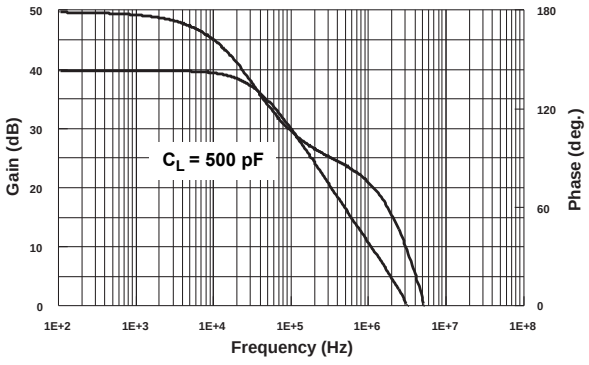


Figure 13. Open loop gain and phase vs. frequency



4 TS922, TS922A macromodel

4.1 Important note concerning this macromodel

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (for example, temperature and supply voltage). Thus the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.

Data derived from macromodels used outside of the specified conditions (for example, V_{CC}, temperature) or worse, outside of the device operating conditions (for example, V_{CC}, V_{icm}), are not reliable in any way.

Section 4.2 provides the electrical characteristics resulting from the use of the TS922, TS922A macromodel.

4.2 Electrical characteristics from macromodelization

Table 5. Electrical characteristics resulting from macromodel simulation at V_{CC} = 3 V, V_{CC}- = 0 V, R_L, C_L connected to V_{CC}/2, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 10 kΩ	200	V/mV
I_{CC}	No load, per operator	1.2	mA
V_{icm}		-0.2 to 3.2	V
V_{OH}	R_L = 10 kΩ	2.95	
V_{OL}		25	mV
I_{sink}	V_O = 3 V	80	mA
I_{source}	V_O = 0 V		
GBP	R_L = 600 kΩ	4	MHz
SR	R_L = 10 kΩ, C_L = 100 pF	1.3	V/µs
ϕm	R_L = 600 kΩ	68	Degrees

4.3 Macromodel code

```
** Standard Linear Ics Macromodels, 1996.
** CONNECTIONS:
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
*
.SUBCKT TS92X 1 2 3 4 5
*
.MODEL MDTH D IS=1E-8 KF=2.664234E-16 CJO=10F
*
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 8.125000E+00
RIN 15 16 8.125000E+00
RIS 11 15 2.238465E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 153.5u
VOFN 13 14 DC 0
IPOL 13 5 3.200000E-05
CPS 11 15 1e-9
DINN 17 13 MDTH 400E-12
VIN 17 5 -0.100000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.400000E+00
FCP 4 5 VOFP 1.865000E+02
FCN 5 4 VOFN 1.865000E+02
FIBP 2 5 VOFP 6.250000E-03
FIBN 5 1 VOFN 6.250000E-03
* GM1 STAGE ***************
FGM1P 119 5 VOFP 1.1
FGM1N 119 5 VOFN 1.1
RAP 119 4 2.6E+06
RAN 119 5 2.6E+06
* GM2 STAGE ***************
G2P 19 5 119 5 1.92E-02
G2N 19 5 119 4 1.92E-02
R2P 19 4 1E+07
```

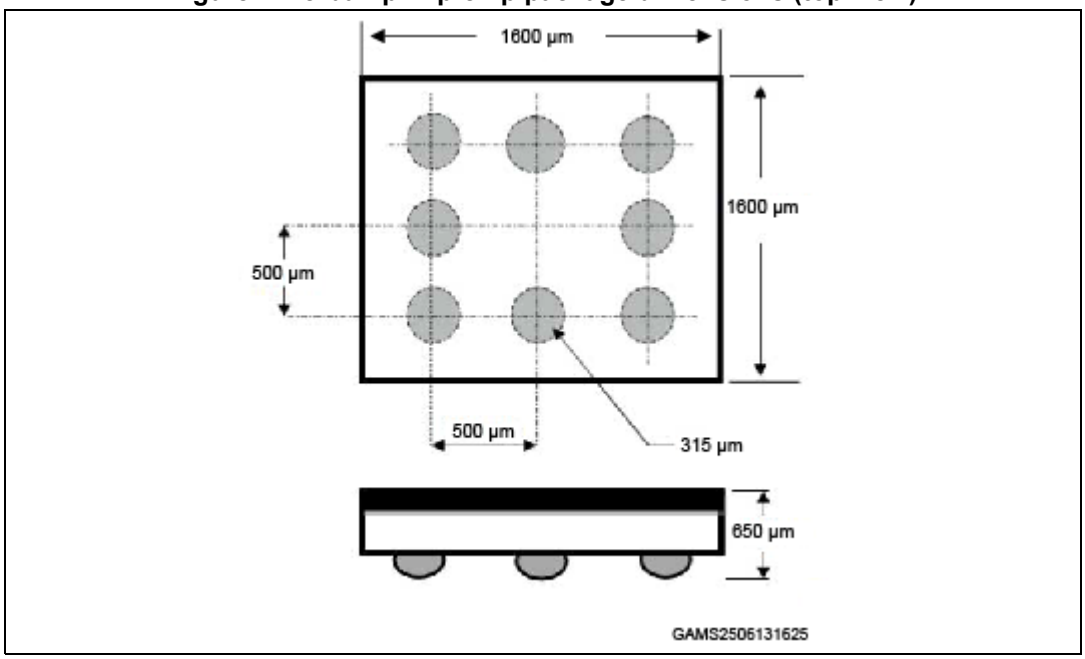
```
R2N 19 5 1E+07
*************************
VINT1 500 0 5
GCONVP 500 501 119 4 19.38
VP 501 0 0
GCONVN 500 502 119 5 19.38
VN 502 0 0
********* orientation isink isource *******
VINT2 503 0 5
FCOPY 503 504 VOUT 1
DCOPYP 504 505 MDTH 400E-9
VCOPYP 505 0 0
DCOPYN 506 504 MDTH 400E-9
VCOPYN 0 506 0
*************************
F2PP 19 5 poly(2) VCOPYP VP 0 0 0 0 0.5
F2PN 19 5 poly(2) VCOPYP VN 0 0 0 0 0.5
F2NP 19 5 poly(2) VCOPYN VP 0 0 0 0 1.75
F2NN 19 5 poly(2) VCOPYN VN 0 0 0 0 1.75
* COMPENSATION ************
CC 19 119 25p
* OUTPUT ***********
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 6.250000E+02
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 6.250000E+02
VINM 5 27 5.000000E+01
VOUT 3 23 0
ROUT 23 19 6
COUT 3 5 1.300000E-10
DOP 19 25 MDTH 400E-12
VOP 4 25 1.052
DON 24 19 MDTH 400E-12
VON 24 5 1.052
.ENDS;TS92X
```

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 8-bump Flip-chip package information

Figure 14. 8-bump Flip-chip package dimensions (top view)



1. Die size: 1600 µm x 1600 µm ±30 µm
   Die height: 350 µm ±20 µm
   Die height (including bumps): 650 µm
   Bump diameter: 315 µm ±50 µm
   Bump height: 250 µm ±40 µm
   Pitch: 500 µm ±10 µm
   Backcoating

Figure 15. 8-bump Flip-chip footprint recommendation

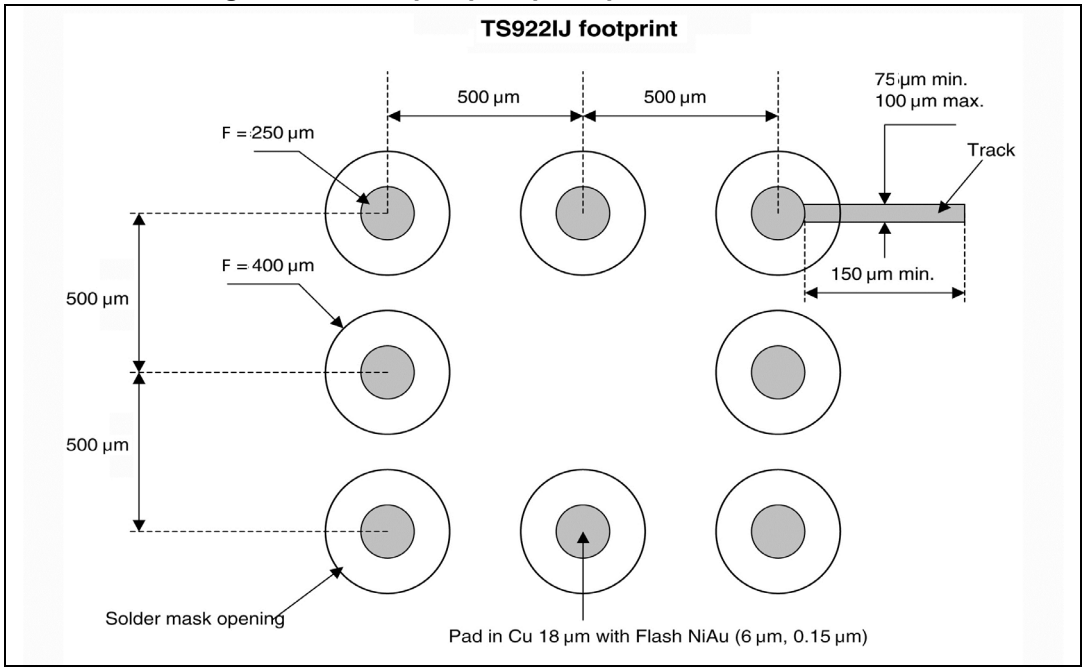
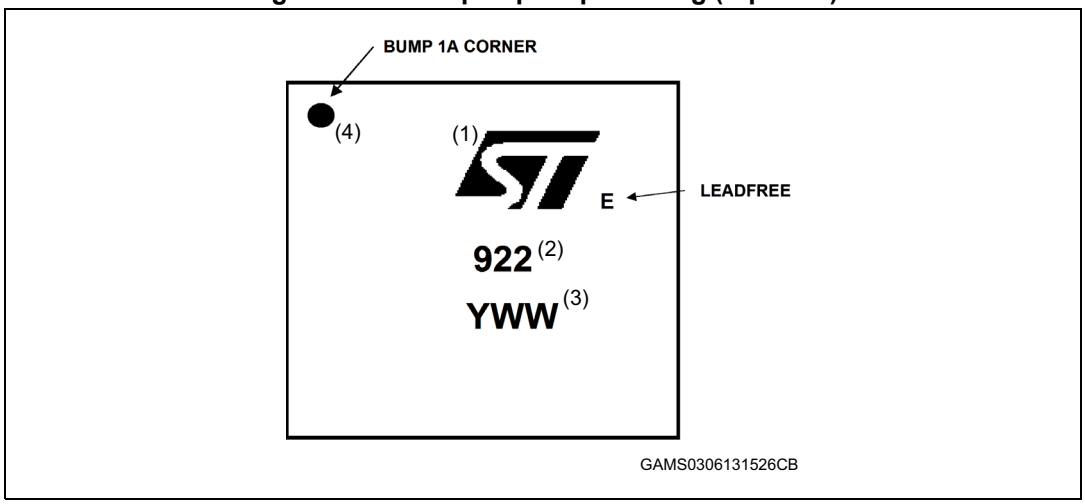
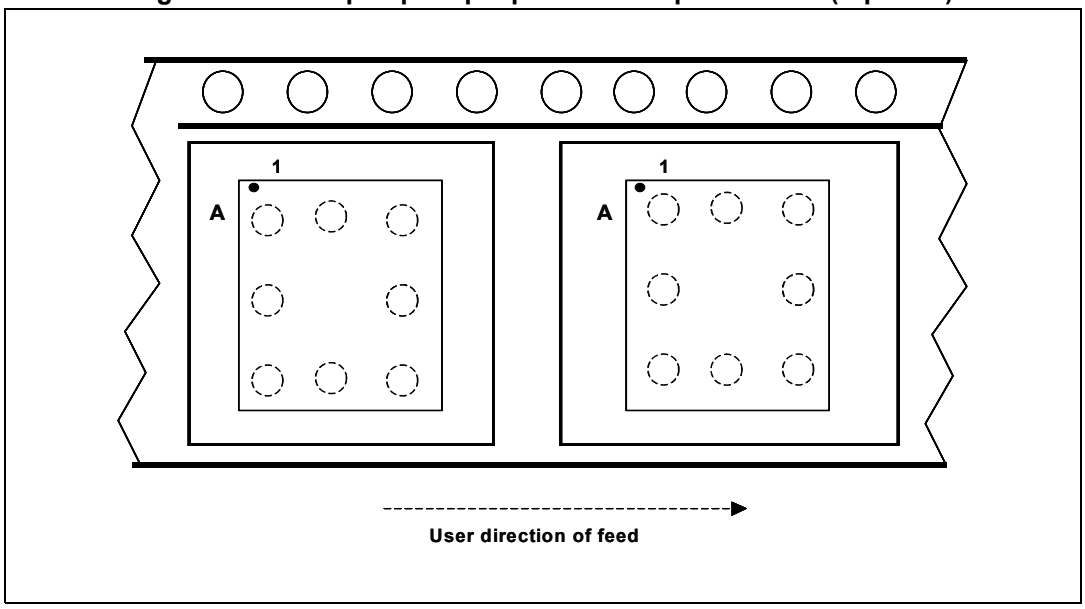


Figure 16. 8-bump Flip-chip marking (top view)



1. ST logo
2. Part number
3. Date code: Y = year, WW = week
4. This dot indicates the bump corner 1A

Figure 17. 8-bump Flip-chip tape and reel specification (top view)



1. Device orientation: the devices are oriented in the carrier pocket with bump number A1 adjacent to the sprocket holes.

5.2 MiniSO8 package information

Figure 18. MiniSO8 package mechanical drawing

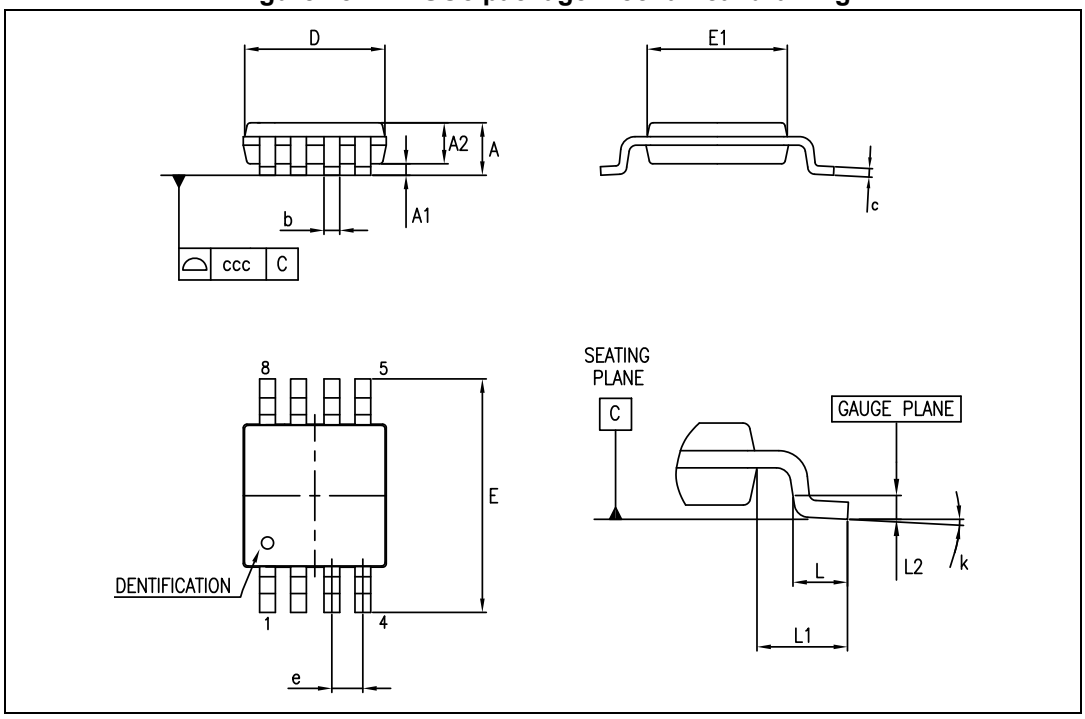


Table 6. MiniSO8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

5.3 SO8 package information

Figure 19. SO8 package mechanical drawing

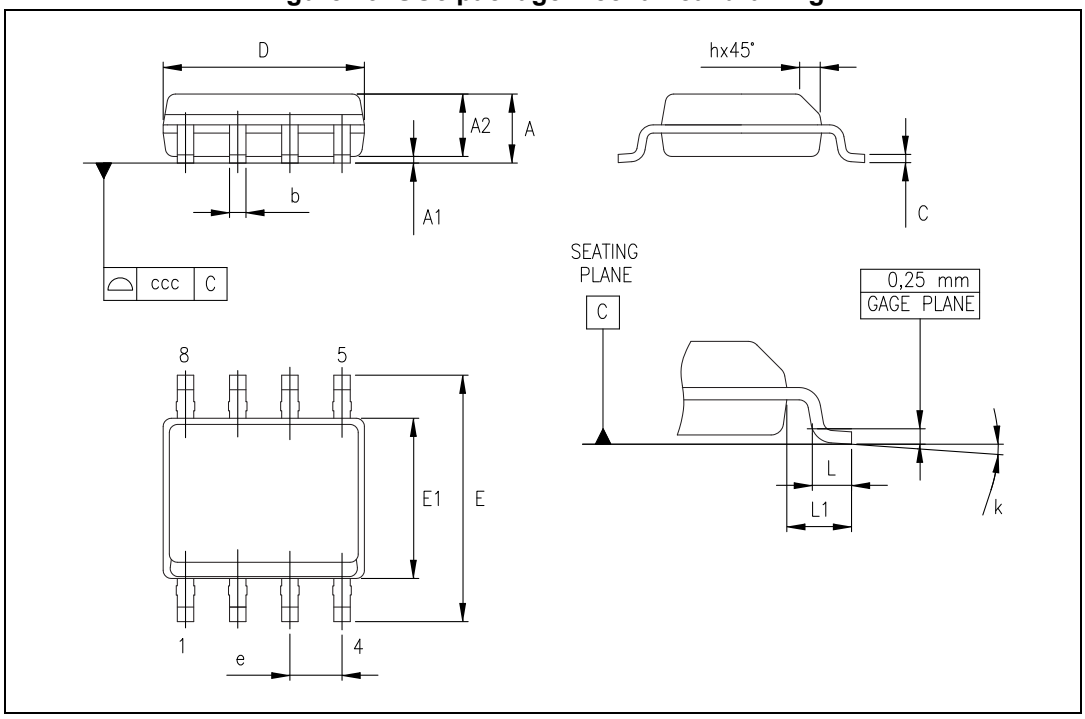


Table 7. SO8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

5.4 TSSOP8 package information

Figure 20. TSSOP8 package mechanical drawing

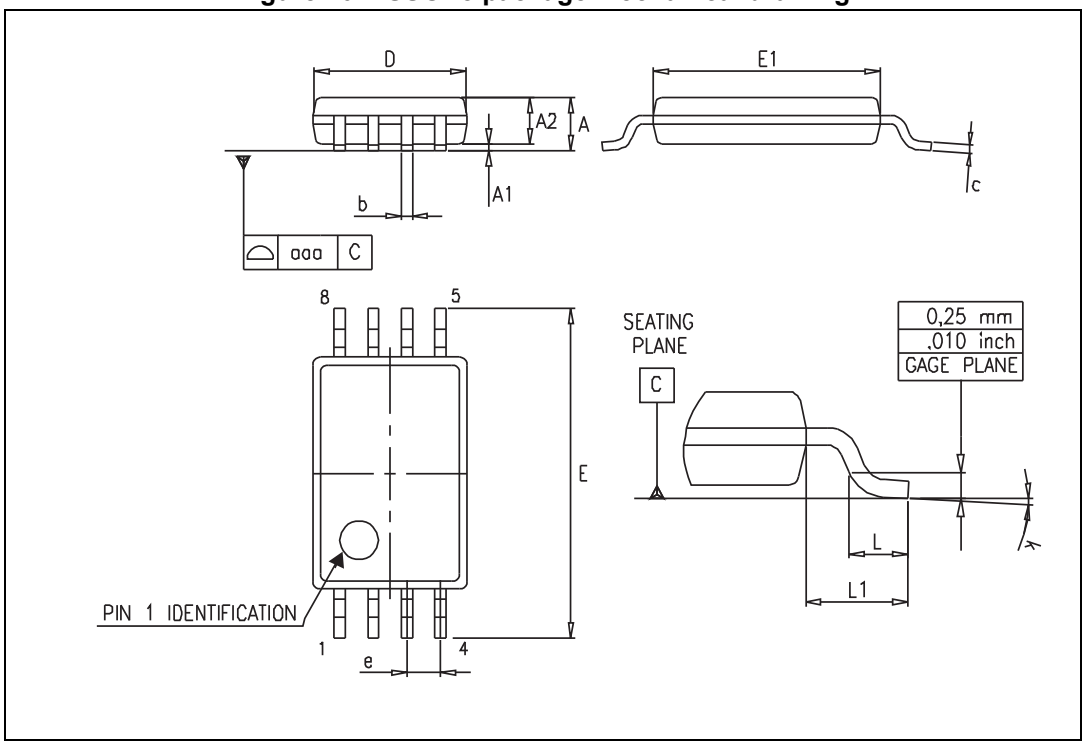


Table 8. TSSOP8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa			0.10			0.004

5.5 DIP8 package information

Figure 21. DIP8 package mechanical drawing

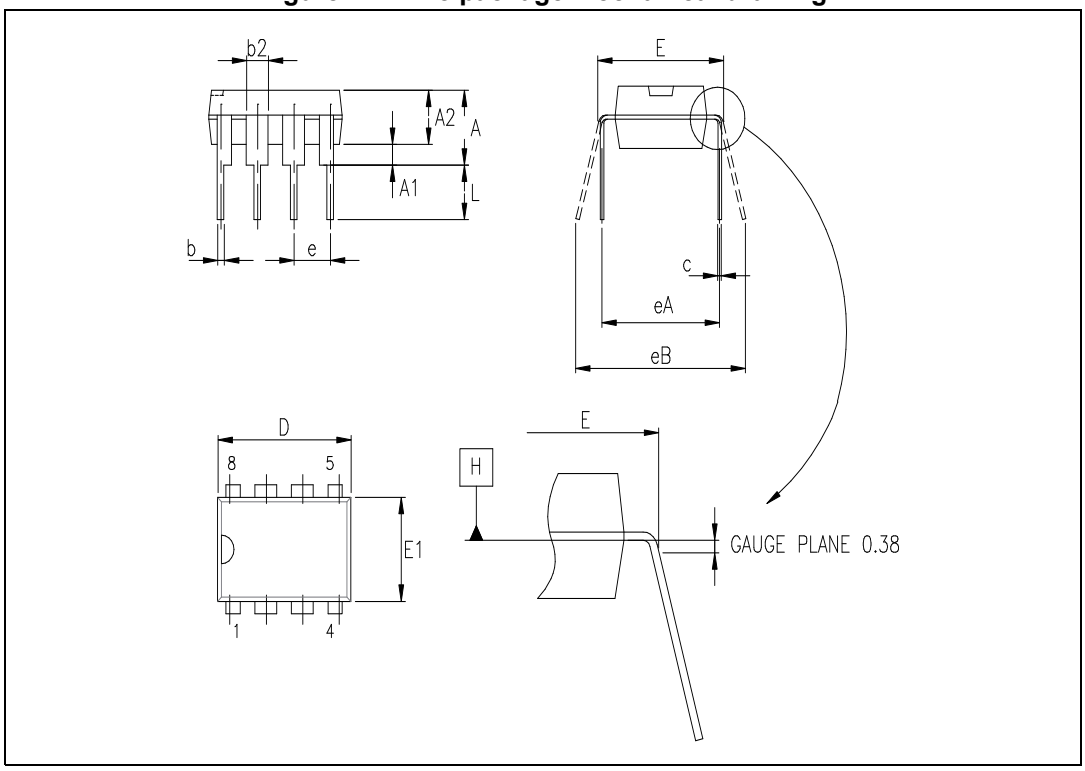


Table 9. DIP8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

6 Ordering information

Table 10. Order codes

Order codes	Temperature range	Package	Packaging	Marking
TS922ID TS922IDT	-40 °C to +125 °C	SO-8	Tube or tape and reel	922I
TS922AID TS922AIDT				922AI
TS922IYDT(1)		SO-8 (automotive grade)		922IY
TS922AIYDT(1)			Tape and reel	922AIY
TS922IPT		TSSOP8		922I
TS922AIPT				922AI
TS922IST		MiniSO8		K158
TS922AIST				K159
TS922IN		DIP8	Tube	TS922IN
TS922IYPT(2)		TSSOP8 (automotive grade)	Tape and reel	922IY
TS922AIYPT(2)				922AY
TS922IYST(2)		MiniSO8 (automotive grade)		K10A
TS922AIYST(2)				K10B
TS922IJT/EIJT		Flip-chip with backcoating		922

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.
2. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent are ongoing.

7 Revision history

Table 11. Document revision history

Date	Revision	Changes
01-Feb-2001	1	First release.
01-Jul-2004	2	Flip-chip package inserted in the document.
02-May-2005	3	Modifications in AMR *Table 1 on page 4* (explanation of V_{id} and V_i limits, ESD MM and CDM values added, R_{thja} added).
01-Aug-2005	4	PPAP references inserted in the datasheet, see *Table 6 on page 22*.
01-Mar-2006	5	TS922EIJT part number inserted in the datasheet, see *Table 6 on page 22*.
26-Jan-2007	6	Modifications in AMR *Table 1 on page 4* (R_{thjc} added), parameter limits on full temperature range added in *Table 3 on page 6* and *Table 4 on page 8*.
12-Nov-2007	7	Added notes on ESD in AMR table. Re-formatted package information. Added notes for automotive grade in order codes table.
02-Feb-2010	8	Document reformatted. Added root part number TS922A on cover page. Removed TS922AIYD order code from *Table 10*.
15-Jan-2013	9	Added MiniSO8 package. Modified test conditions for CMR in *Table 3* and *Table 4*. Replaced V_{DD} by V_{CC-} in title of *Table 3*, *Table 4*, and *Table 5*. Updated titles of *Figure 7* to *Figure 12* (added conditions to differentiate them). Removed TS922IYD device from *Table 10*. Minor corrections throughout document.
04-Jun-2013	10	*Features*: updated package information for Flip-chip *Figure 2*: Updated title *Table 1*: updated footnotes *5*, *6*, and *7* *Table 3* and *Table 4*: replaced DV_{io} with $\Delta V_{io}/\Delta T$ *Figure 14*: added backcoating to package information *Figure 16*: updated footnote *3* *Table 10*: updated package information for Flip-chip
27-Jun-2013	11	*Figure 14*: updated to include new height for backcoating