

PH16030L

N-channel TrenchMOS™ logic level FET

Rev. 01 — 24 February 2005 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- SO8 equivalent area footprint
- Low thermal resistance
- Low gate charge.

1.3 Applications

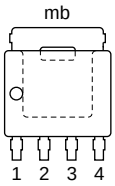
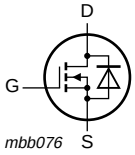
- DC-to-DC converters
- Portable appliances.

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $R_{DSon} \leq 16.9$ mΩ
- $I_D \leq 38$ A
- $Q_{gd} = 2.9$ nC (typ).

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source		
4	gate		
mb	mounting base; connected to drain		

SOT669 (LFPAK)

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PH16030L	LFPAK	plastic single-ended surface mounted package; 4 leads	SOT669

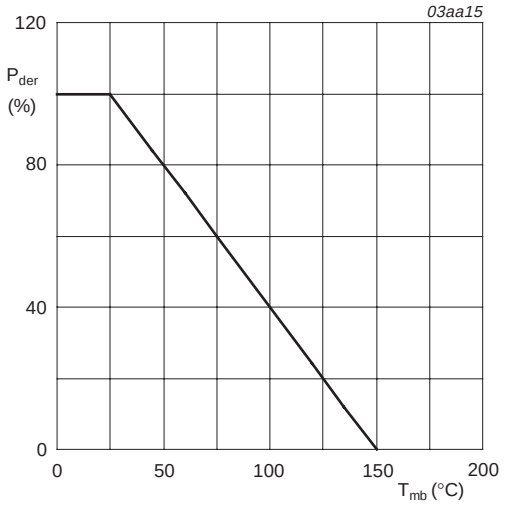
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

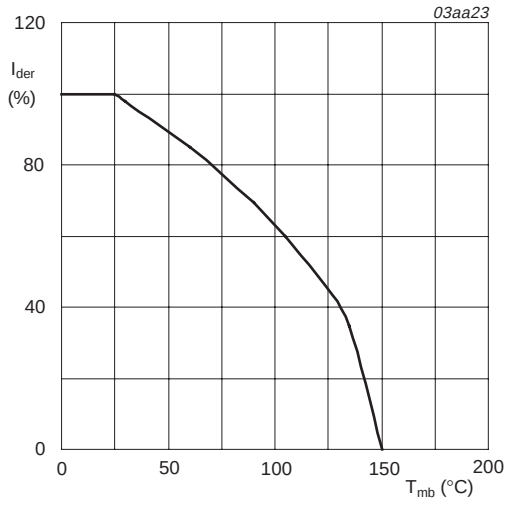
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C	-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage (DC)		-	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	-	38	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2	-	24	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	41.6	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	38	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	100	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 21 A; t_p = 0.1 ms; V_{DD} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C	-	44	mJ

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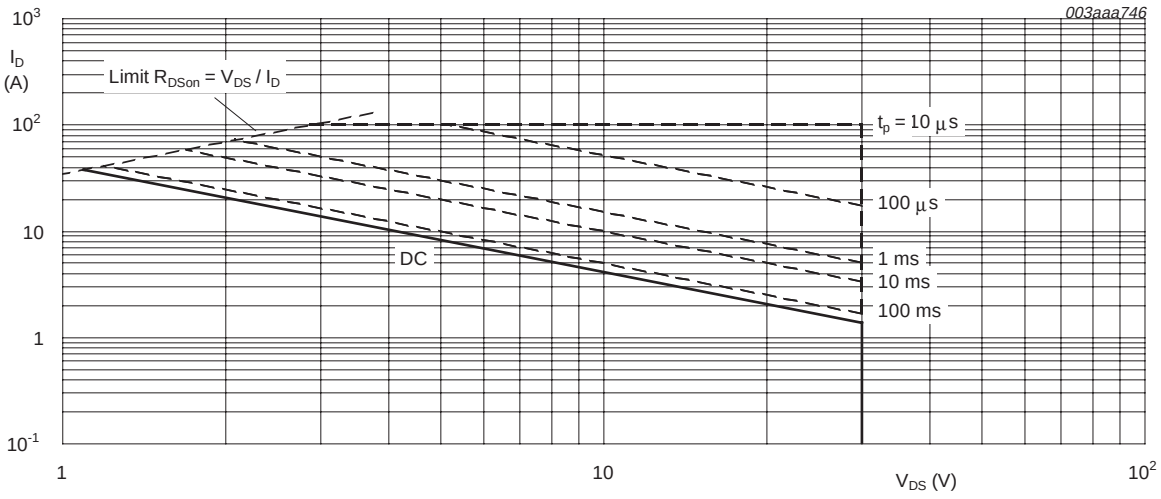
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	3	K/W

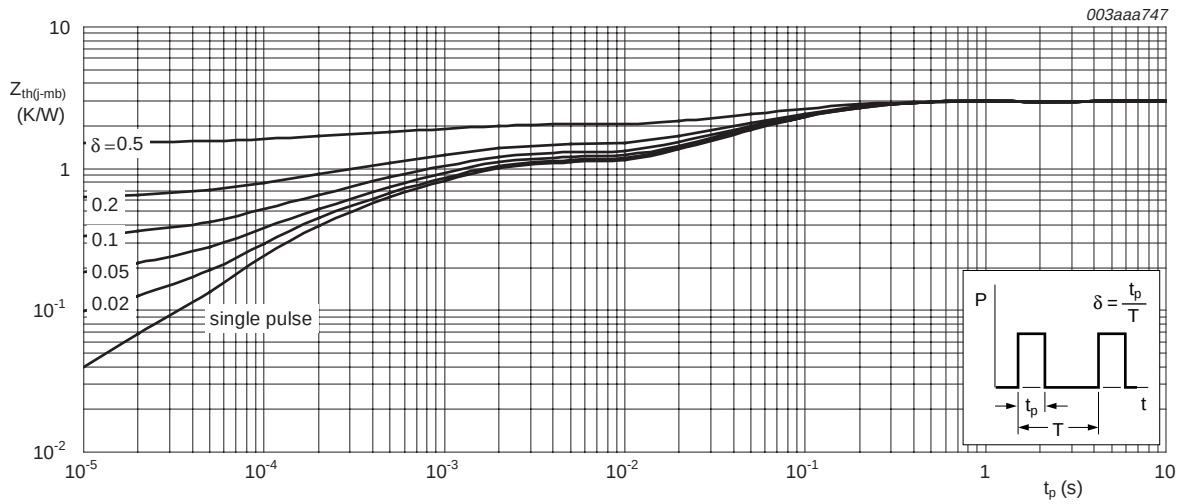


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

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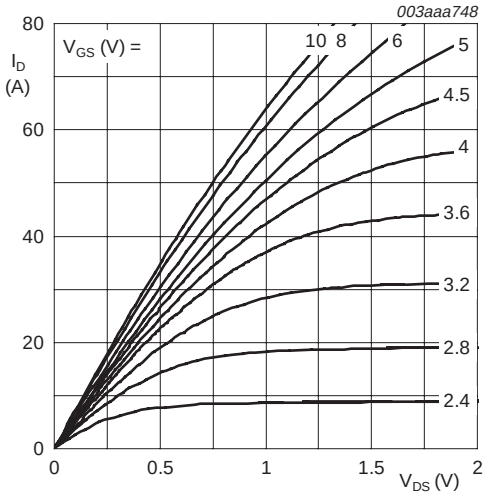
6. Characteristics

Table 5: Characteristics

T_j = 25 °C unless otherwise specified.

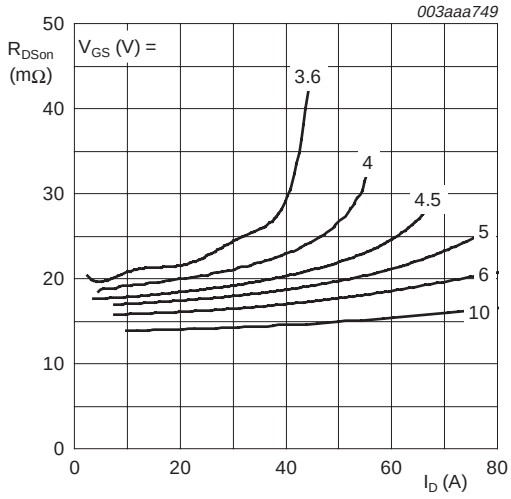
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9 and 10				
		T_j = 25 °C	1	1.5	2	V
		T_j = 150 °C	0.6	-	-	V
		T_j = –55 °C	-	-	2.2	V
I_{DSS}	drain-source leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; Figure 6 and 8				
		T_j = 25 °C	-	14.1	16.9	mΩ
		T_j = 150 °C	-	24	28.7	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; Figure 6 and 8	-	18.8	23.5	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Figure 11 and 12	-	8.2	-	nC
Q_{gs}	gate-source charge		-	2.3	-	nC
Q_{gs1}	pre-$V_{GS(th)}$ gate-source charge		-	0.9	-	nC
Q_{gs2}	post-$V_{GS(th)}$ gate-source charge		-	1.4	-	nC
Q_{gd}	gate-drain (Miller) charge		-	2.9	-	nC
V_{plat}	plateau voltage		-	2.6	-	V
$Q_{g(tot)}$	total gate charge	I_D = 0 A; V_{DS} = 0 V; V_{GS} = 4.5 V	-	6.7	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 12 V; f = 1 MHz; Figure 14	-	680	-	pF
C_{oss}	output capacitance		-	280	-	pF
C_{rss}	reverse transfer capacitance		-	135	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 0 V; f = 1 MHz	-	1090	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 1 Ω; V_{GS} = 4.5 V; R_G = 5.6 Ω	-	9	-	ns
t_r	rise time		-	18	-	ns
$t_{d(off)}$	turn-off delay time		-	16	-	ns
t_f	fall time		-	33	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 15 A; V_{GS} = 0 V; Figure 13	-	0.86	1.2	V
t_{rr}	reverse recovery time	I_S = 15 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	34	-	ns
Q_r	recovered charge		-	12	-	nC

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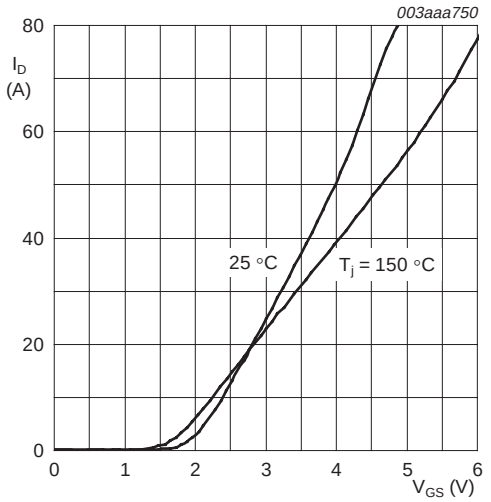
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



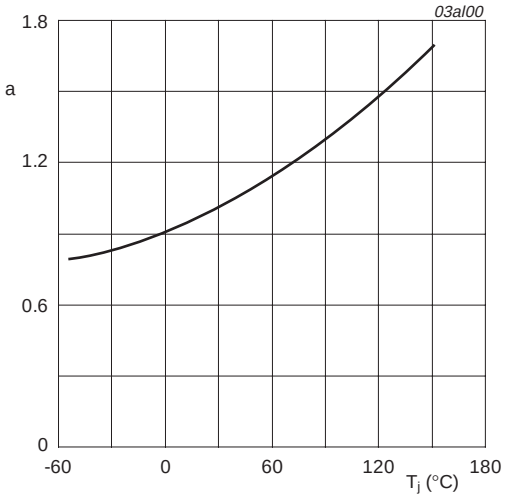
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

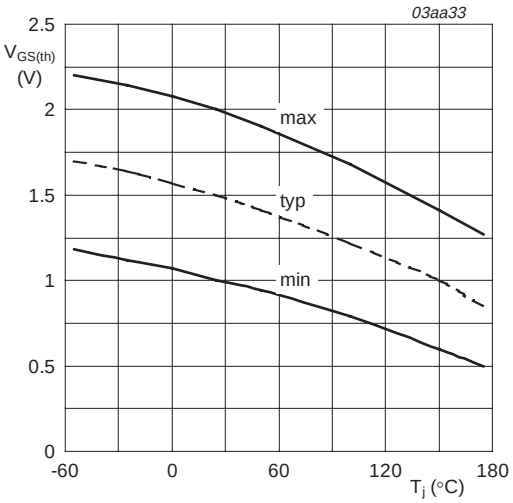
Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25\,^{\circ}C)}}$$

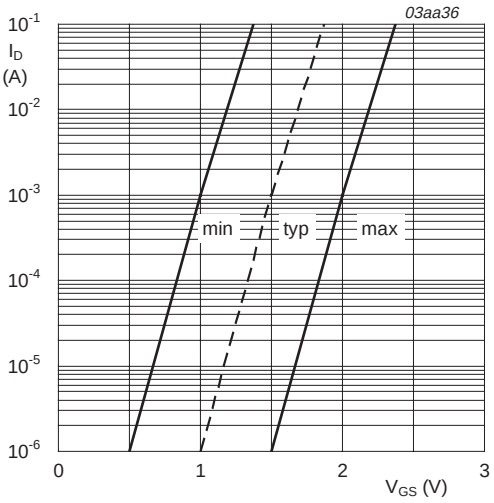
Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature

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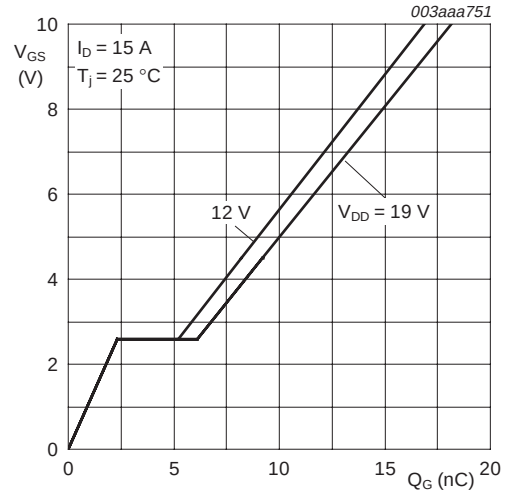
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



I_D = 15 A; V_{DS} = 12 V and 19 V

Fig 11. Gate-source voltage as a function of gate charge; typical values

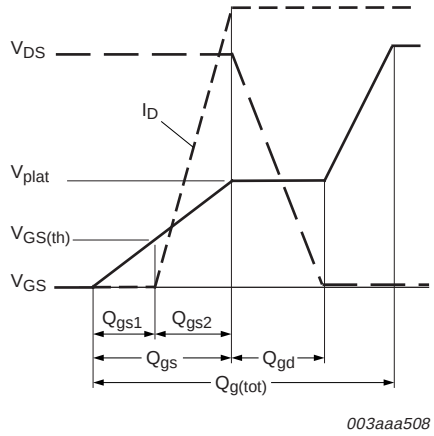
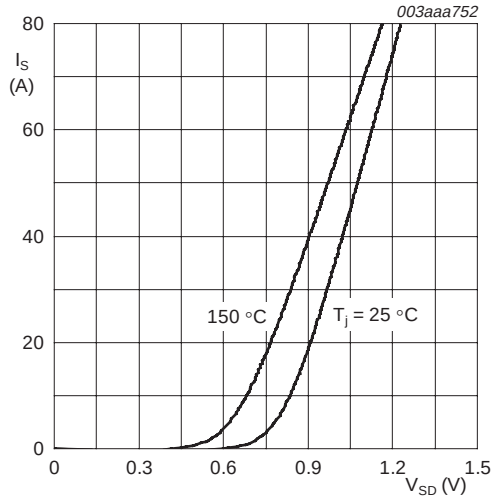


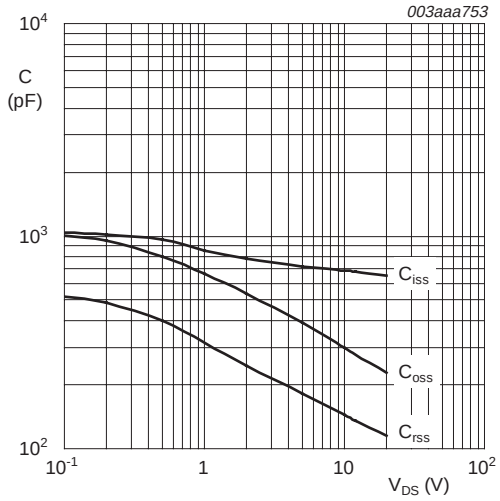
Fig 12. Gate charge waveform definitions

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T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



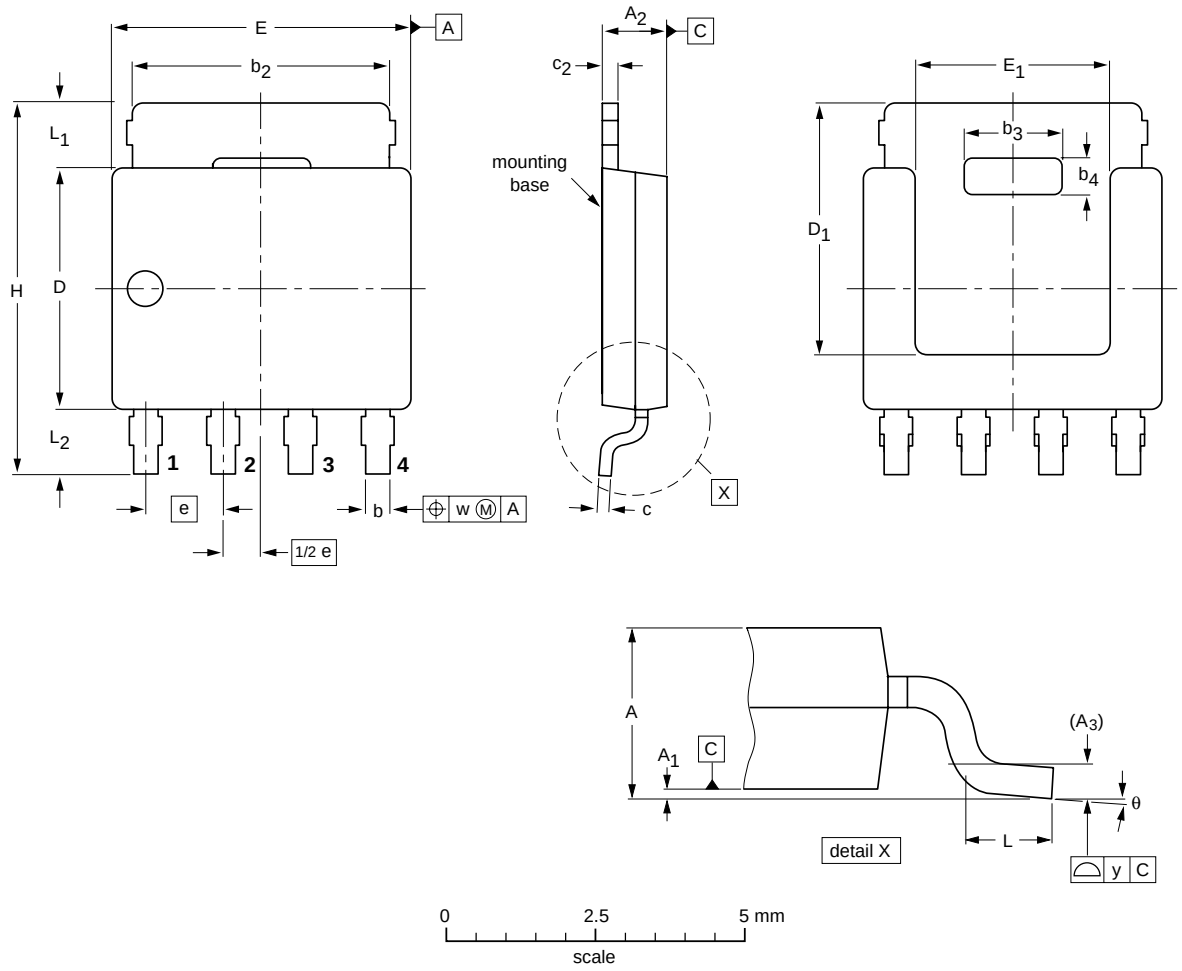
V_{GS} = 0 V; f = 1 MHz

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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7. Package outline

Plastic single-ended surface mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1^{(1)}$ max	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~03-09-15~~ 04-10-13

Fig 15. Package outline SOT669 (LFPAK)

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8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH16030L_1	20050224	Product data sheet	-	9397 750 14431	-

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9. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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