24LC16B

16K I²C Serial EEPROM
Extended (-55°C to +125°C) Operating Temperatures

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges
24LC16B	2.5V-5.5V	400 kHz	M

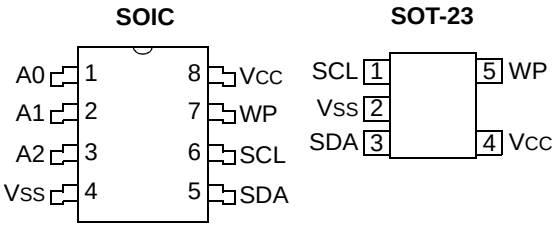
Features

- Single Supply with Operation down to 2.5V
- Low-Power CMOS Technology:
  - Active current 1 mA, typical
  - Standby current, 1 µA, typical
- 2-Wire Serial Interface, I²C Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- Page Write Time 5 ms Maximum
- Self-Timed Erase/Write Cycle
- 16-Byte Page Write Buffer
- Hardware Write-Protect
- ESD Protection >4,000V
- More than 1 Million Erase/Write Cycles
- Data Retention >200 Years
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
  - Extended (M): -55°C to +125°C

Description

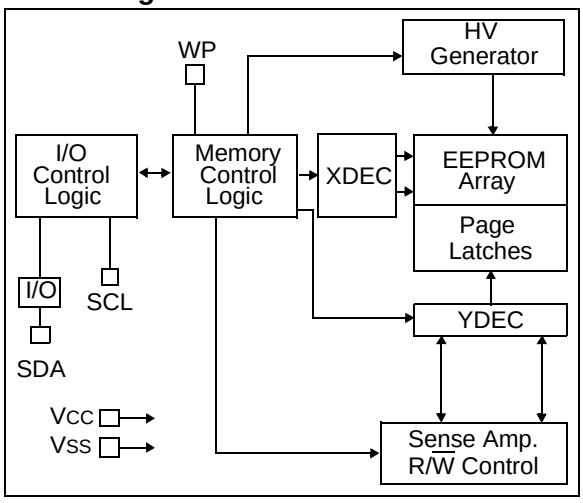
The Microchip Technology Inc. 24LC16B is a 16 Kbit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 2.5V with standby and active currents of only 1 µA and 1 mA, respectively. The 24LC16B also has a page write capability for up to 16 bytes of data. The 24LC16B is available in the standard 8-pin SOIC and 5-lead SOT-23 packages.

Package Types



Note: Pins A0, A1 and A2 are not used by the 24LC16B (no internal connections).

Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-55°C to +125°C

ESD protection on all pins .....≥4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Extended (M): TA = -55°C to +125°C, VCC = +2.5V to +5.5V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level Input Voltage	0.7 VCC	—	—	V	
D2	VIL	Low-Level Input Voltage	—	—	0.3 VCC	V	
D3	VHYS	Hysteresis of Schmitt Trigger Inputs	0.05 VCC	—	—	V	**Note 1**
D4	VOL	Low-Level Output Voltage	—	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D5	ILI	Input Leakage Current	—	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	—	±1	µA	VOUT = VSS or VCC
D7	CIN	Pin Capacitance (all inputs/outputs)	—	—	10	pF	VCC = 5.0V (**Note 1**) TA = 25°C, FCLK = 1 MHz
	COUT						
D8	ICCWRITE	Operating current	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
D9	ICCREAD		—	0.01	1	mA	
D10	ICCS	Standby Current	—	—	1	µA	+85°C, SDA = SCL = VCC WP = VSS
			—	—	5	µA	+125°C, SDA = SCL = VCC WP = VSS

Note 1: This parameter is periodically sampled and not 100% tested.

2: Typical measurements taken at room temperature.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Extended (M): T_A = -55°C to +125°C, V_{CC} = +2.5V to +5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock Frequency	—	400	kHz	
2	T_{HIGH}	Clock High Time	600	—	ns	
3	T_{LOW}	Clock Low Time	1300	—	ns	
4	T_R	SDA and SCL Rise Time **(Note 1)**	—	300	ns	**Note 1**
5	T_F	SDA and SCL Fall Time	—	300	ns	**Note 1**
6	$T_{HD:STA}$	Start Condition Hold Time	600	—	ns	
			4000	—	ns	
7	$T_{SU:STA}$	Start Condition Setup Time	600	—	ns	
8	$T_{HD:DAT}$	Data Input Hold Time	0	—	ns	**Note 2**
9	$T_{SU:DAT}$	Data Input Setup Time	100	—	ns	
10	$T_{SU:STO}$	Stop Condition Setup Time	600	—	ns	
11	T_{AA}	Output Valid from Clock **(Note 2)**	—	900	ns	
12	T_{BUF}	Bus Free Time: Bus time must be free before a new transmission can start	1300	—	ns	
13	T_{OF}	Output Fall Time from V_{IH} Minimum to V_{IL} Maximum	20+0.1C_B	250	ns	
14	T_{SP}	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	**Notes 1** and **3**
15	T_{WC}	Write Cycle Time (byte or page)	—	5	ms	
16		Endurance	1M	—	cycles	Page mode, +25°C, 5.5V **(Note 4)**

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's website at www.microchip.com.

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FIGURE 1-1: BUS TIMING DATA

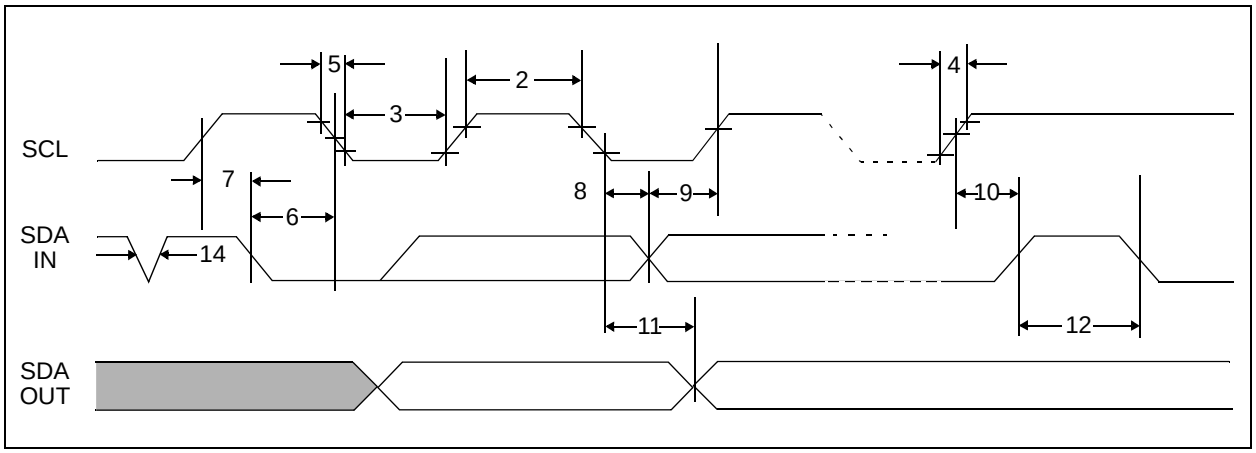
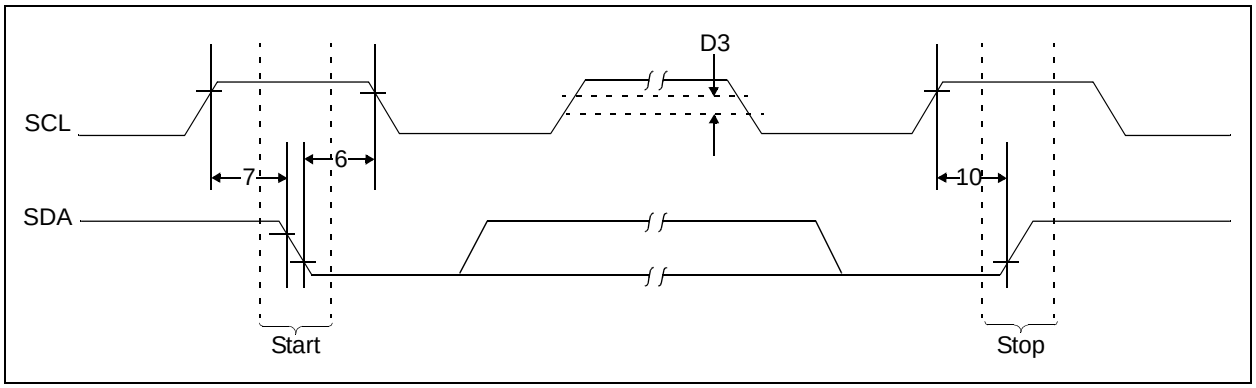


FIGURE 1-2: BUS TIMING START/STOP



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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-pin SOIC	5-pin SOT-23	Description
A0	1	—	Not Connected
A1	2	—	Not Connected
A2	3	—	Not Connected
VSS	4	2	Ground
SDA	5	3	Serial Address/Data I/O
SCL	6	1	Serial Clock
WP	7	5	Write-Protect Input
VCC	8	4	+2.5V to +5.5V Power Supply

2.1 Serial Address/Data Input/Output (SDA)

SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating Start and Stop conditions.

2.2 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

2.3 Write-Protect (WP)

The WP pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to VCC, write operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

2.4 A0, A1, A2

The A0, A1 and A2 pins are not used by the 24LC16B. They may be left floating or tied to either VSS or VCC.

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3.0 FUNCTIONAL DESCRIPTION

The 24LC16B supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24LC16B works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the master device and is, theoretically, unlimited (although only the last sixteen will be stored when doing a write operation). When an overwrite does occur it will replace data in a first-in first-out (FIFO) fashion.

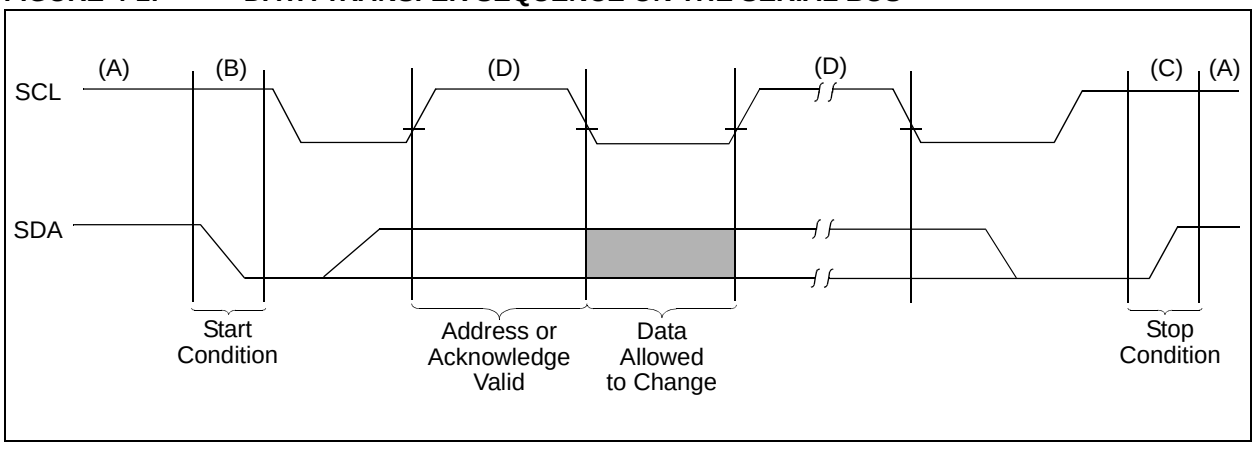
4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24LC16B does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC16B) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



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5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a four-bit control code. For the 24LC16B, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Block Select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word-blocks of memory are to be accessed. These bits are, in effect, the three Most Significant bits (MSb) of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore, the protocol can support only one 24LC16B per system.

The last bit of the Control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the Start condition, the 24LC16B monitors the SDA bus, checking the device type identifier being transmitted and, upon receiving a '1010' code, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC16B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 5-1: CONTROL BYTE ALLOCATION

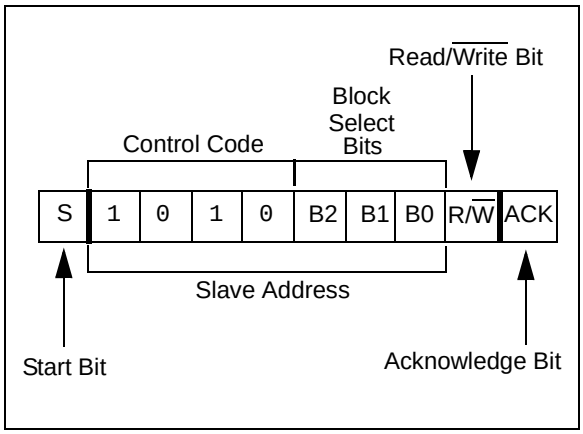
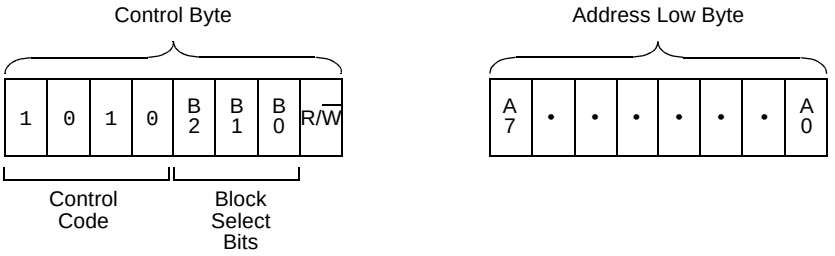


FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATION

6.1 Byte Write

Following the Start condition from the master, the device code (four bits), the block address (three bits) and the R/$\overline{W}$ bit, which is a logic low, are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the Address Pointer of the 24LC16B. After receiving another Acknowledge signal from the 24LC16B, the master device will transmit the data word to be written into the addressed memory location. The 24LC16B acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and, during this time, the 24LC16B will not generate Acknowledge signals (Figure 6-1).

Note:	When doing a write of less than 16 bytes, the data in the rest of the page is refreshed along with the data bytes being written. This will force the entire page to endure a write cycle; for this reason, endurance is specified per page.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC16B in the same way as in a byte write. However, instead of generating a Stop condition, the master transmits up to 16 data bytes to the 24LC16B, which are temporarily stored in the on-chip page buffer and will be written into memory once the master has transmitted a Stop condition. Upon receipt of each word, the four lower-order Address Pointer bits are internally incremented by one. The higher-order 7 bits of the word address remain constant. If the master should transmit more than 16 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 6-2).

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page-size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (000-7FF) when the pin is tied to VCC. If tied to VSS, the write protection is disabled.

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FIGURE 6-1: BYTE WRITE

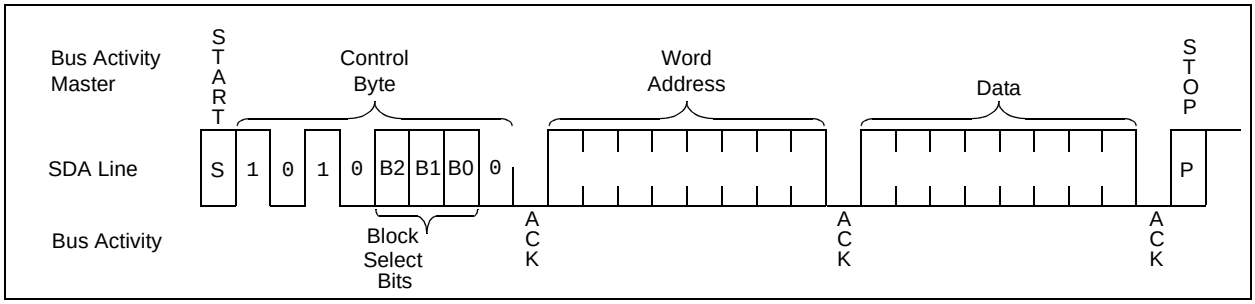
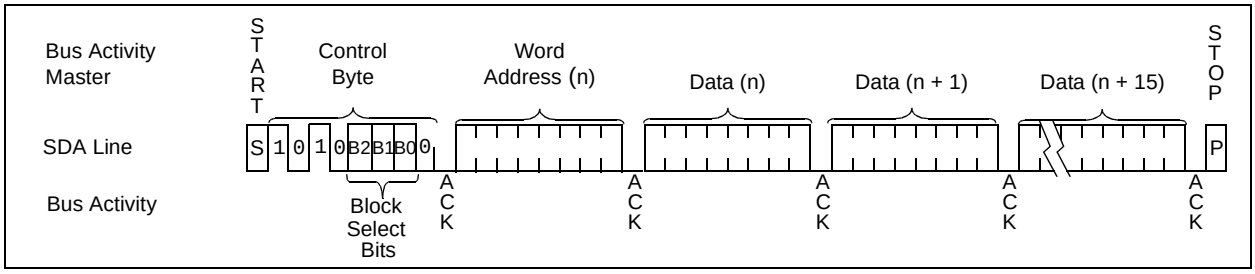


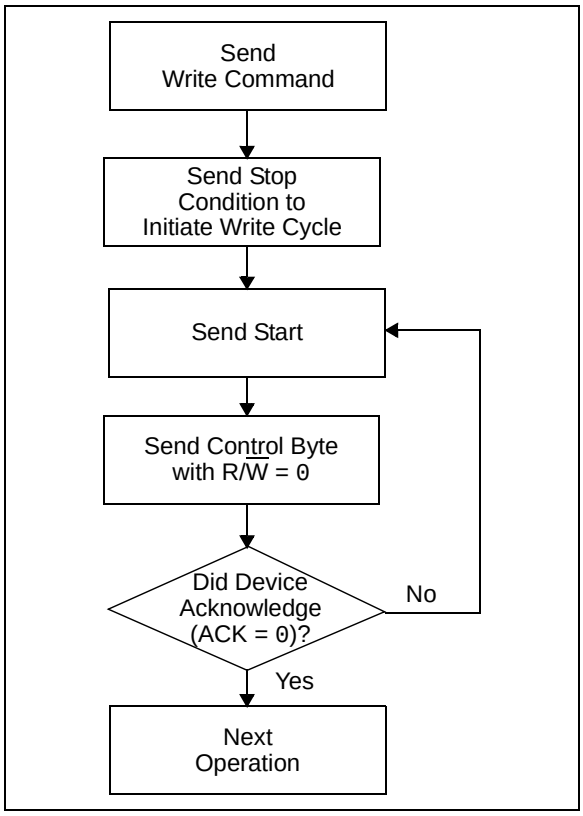
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally-timed write cycle and ACK polling can then be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for a flow diagram of this operation.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



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8.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24LC16B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address 'n', the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to '1', the 24LC16B issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24LC16B discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24LC16B as part of a write operation. Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24LC16B will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24LC16B will discontinue transmission (Figure 8-2).

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24LC16B transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24LC16B to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 24LC16B contains an internal Address Pointer that is incremented by one upon completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24LC16B employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5V at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

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FIGURE 8-1: CURRENT ADDRESS READ

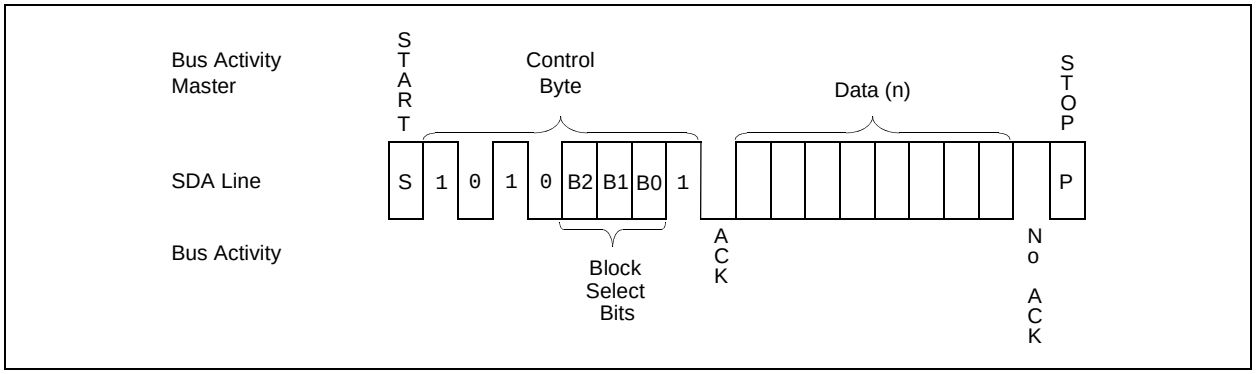


FIGURE 8-2: RANDOM READ

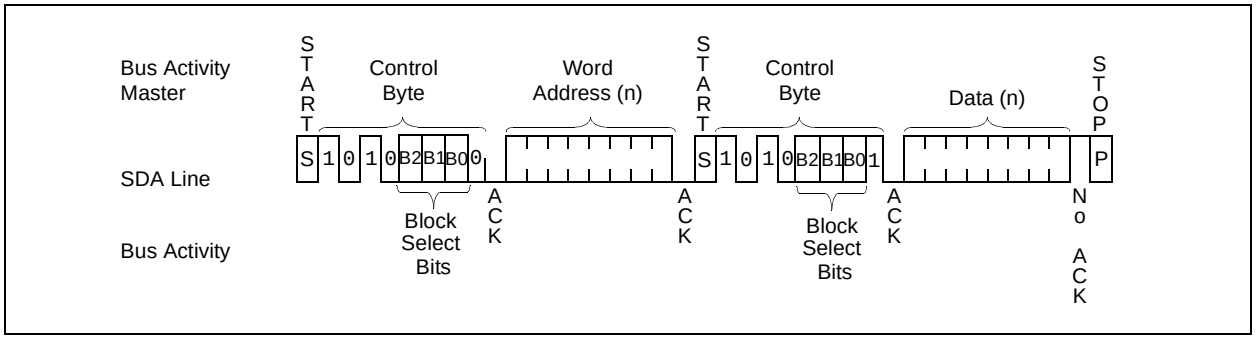
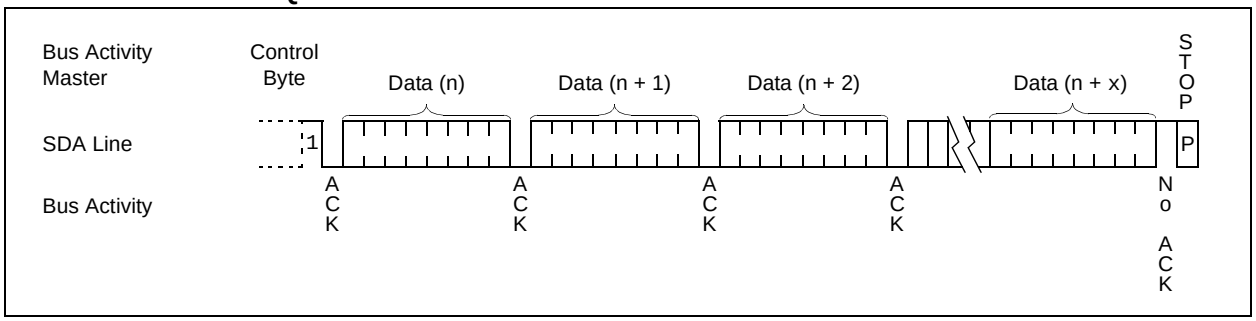


FIGURE 8-3: SEQUENTIAL READ

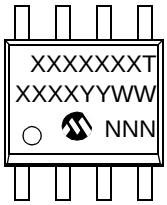


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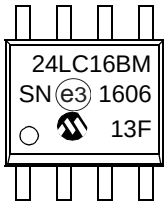
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

8-Lead SOIC (3.90 mm)



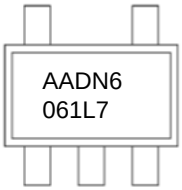
Example:



5-Lead SOT-23



Example:



Part Number	1st Line Marking Codes	
	SOIC	SOT-23
24LC16B	24LC16BT	AADNY

Legend:	XX...X	Part number or part number code
	T	Temperature (M)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	JEDEC® designator for Matte Tin (Sn)

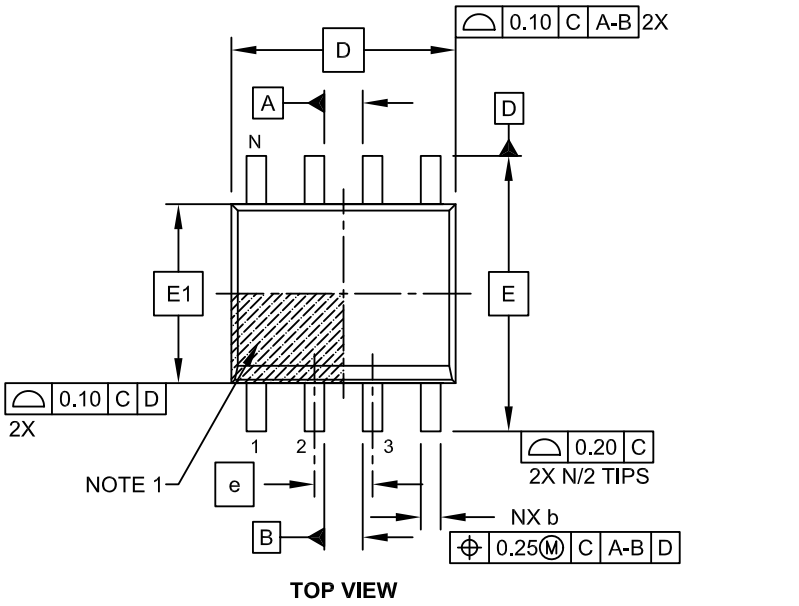
Note: For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

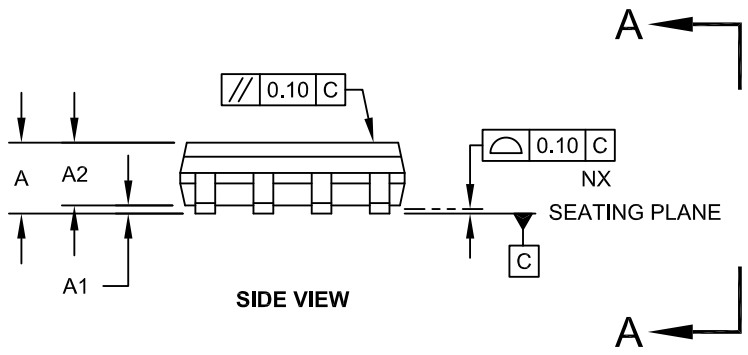
*****Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

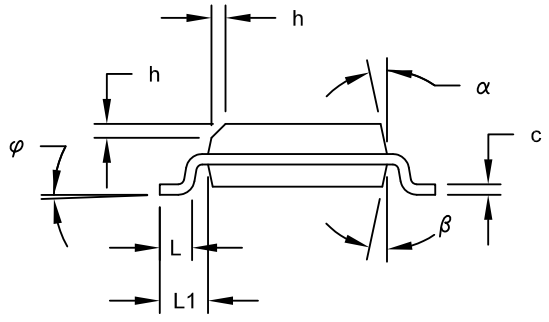
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



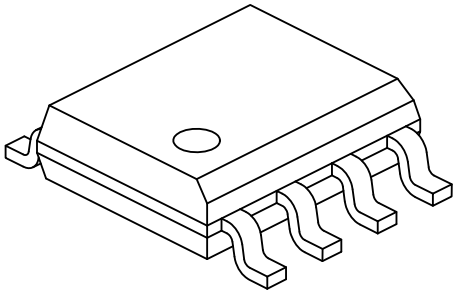
VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

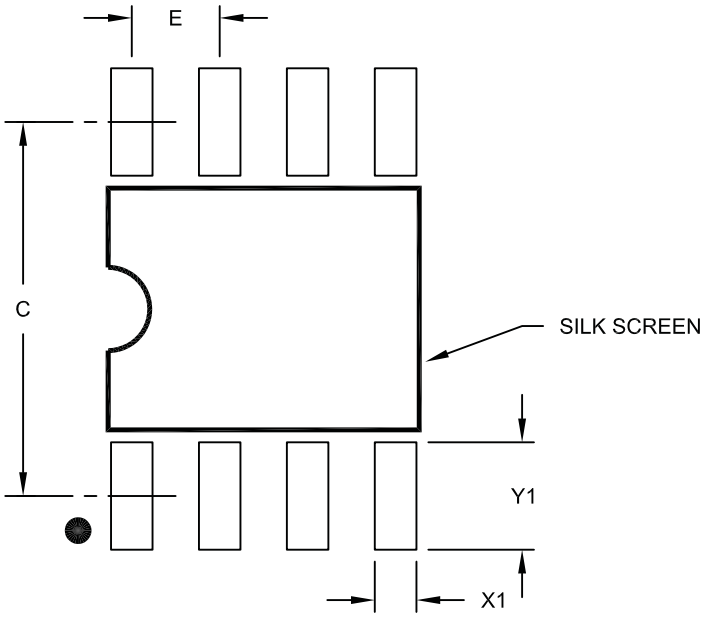
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

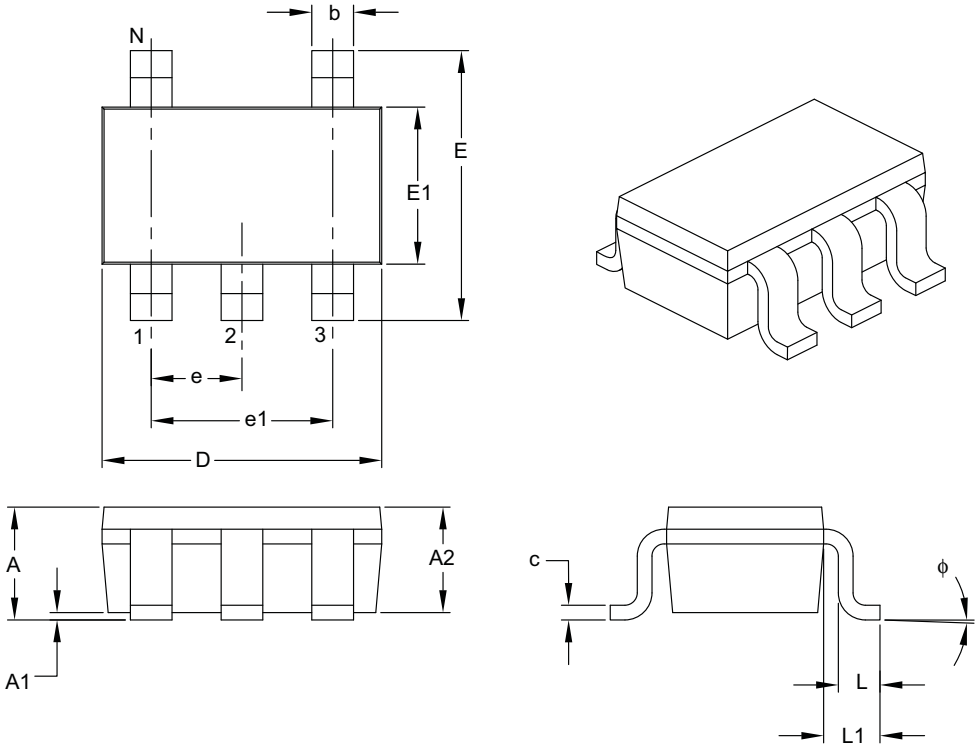
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

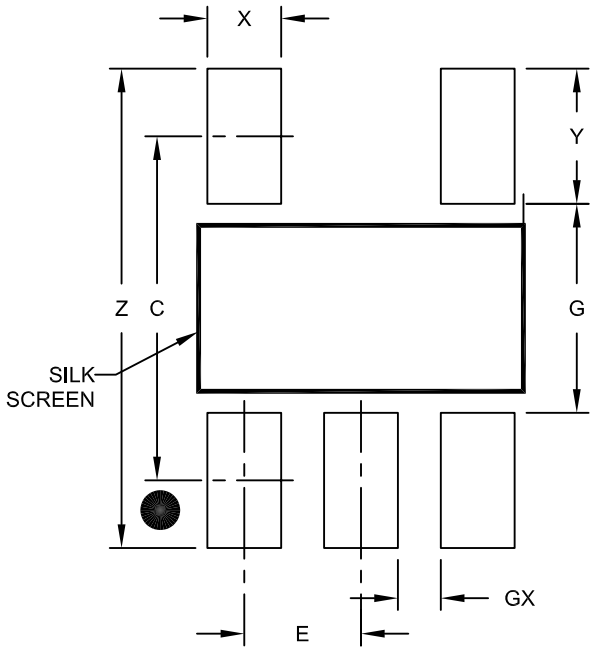
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

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APPENDIX A: REVISION HISTORY

Revision A (10/2009)

Initial release of this document.

Revision B (03/2016)

Added 5-Lead SOT-23 package.

NOTES:

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PART NO.	[X](1)	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	24LC16B:	= 2.5V, 16 Kbit I^2C Serial EEPROM
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	M	= –55°C to +125°C
Package:	SN OT	= Plastic SOIC (3.90 mm body), 8-lead = Plastic SOT-23, 5-lead (Tape and Reel only)

Examples:

a) 24LC16B-M/SN = Extended temp., 2.5V, SOIC package.

b) 24LC16BT-M/OT = Tape and Reel, Extended temp., 2.5V, SOT-23 package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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