LM5025 Active Clamp Voltage Mode PWM Controller

1 Features

- Internal Start-Up Bias Regulator
- 3-A Compound Main Gate Driver
- Programmable Line Undervoltage Lockout (UVLO) With Adjustable Hysteresis
- Voltage Mode Control With Feed-Forward
- Adjustable Dual-Mode Overcurrent Protection
- Programmable Overlap or Deadtime Between the Main and Active Clamp Outputs
- Volt × Second Clamp
- Programmable Soft-Start
- Leading Edge Blanking
- Single Resistor Programmable Oscillator
- Oscillator UP and DOWN Sync Capability
- Precision 5-V Reference
- Thermal Shutdown

2 Applications

- Server Power Supplies
- 48-V Telecom Power Supplies
- 42-V Automotive Applications
- High-Efficiency DC-to-DC Power Supplies

3 Description

The LM5025 PWM controller contains all of the features necessary to implement power converters using the active clamp and reset technique. The device can be configured to control either a P-channel clamp switch or an N-channel clamp switch. With the active clamp technique, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp and reset techniques.

Two control outputs are provided, the main power switch control (OUT_A), and the active clamp switch control (OUT_B). The active clamp output can be configured for either a specified overlap time (for P-channel switch applications) or a specified deadtime (for N_channel applications). The two internal compound gate drivers parallel both MOS and bipolar devices, providing superior gate drive characteristics. This controller is designed for high-speed operation including an oscillator frequency range up to 1 MHz and total PWM and current sense propagation delays less than 100 ns.

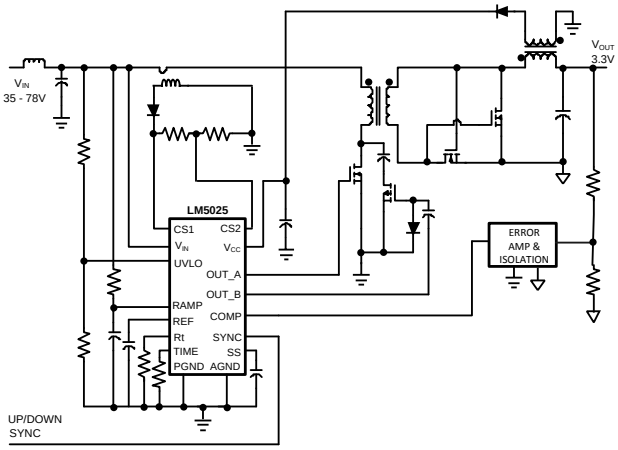
The LM5025 includes a high-voltage start-up regulator that operates over a wide input range of 13 V to 90 V. Additional features include: line undervoltage lockout (UVLO), soft-start, oscillator UP and DOWN sync capability, precision reference and thermal shutdown.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5025	TSSOP (16)	5.00 mm × 4.40 mm
	WSON (16)	5 00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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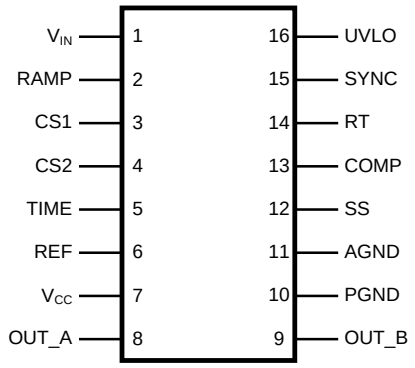
5 Pin Configuration and Functions

PW and NHQ Packages
16-Pin TSSOP and WSON
Top View



Pin Functions

PIN		I/O (1)	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	V_{IN}	I	Source input voltage	Input to start-up regulator. Input 13 V to 90 V, with transient capability to 100 V.
2	RAMP	I	Modulator ramp signal	An external RC circuit from Vin sets the ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET, initiated by either the internal clock or the V*Sec Clamp comparator.
3	CS1	I	Current sense input for cycle-by-cycle limiting	If CS1 exceeds 0.25 V the outputs goes into Cycle-by-Cycle current limit. CS1 is held low for 50 ns after OUT_A switches high providing leading edge blanking.
4	CS2	I	Current sense input for soft restart	If CS2 exceeds 0.25 V the outputs are disabled and a soft-start commences. The soft-start capacitor is fully discharged and then released with a pullup current of 1 µA. After the first output pulse (when SS = 1 V), the SS charge current reverts back to 20 µA. CS2 is held low for 50 ns after OUT_A switches high, providing leading edge blanking.
5	TIME	I	Output overlap and deadtime control	An external resistor (R_{SET}) sets either the overlap time or dead time for the active clamp output. An R_{SET} resistor connected between TIME and GND produces in-phase OUT_A and OUT_B pulses with overlap. An R_{SET} resistor connected between TIME and REF produces out-of-phase OUT_A and OUT_B pulses with deadtime.
6	REF	O	Precision 5-V reference output	Maximum output current: 10-mA locally decouple with a 0.1-µF capacitor. Reference stays low until the line UVLO and the V_{CC} UV comparators are satisfied.
7	V_{CC}	P	Output from the internal high-voltage start-up regulator. The V_{CC} voltage is regulated to 7.6 V	If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator shutdowns, reducing the IC power dissipation.
8	OUT_A	O	Main output driver	Output of the main switch PWM output gate driver. Output capability of 3-A peak sink current.
9	OUT_B	O	Active clamp output driver	Output of the active clamp switch gate driver. Capable of 1.25-A peak sink current..
10	PGND	G	Power ground	Connect directly to analog ground.
11	AGND	G	Analog ground	Connect directly to power ground. For the WSON package option the exposed pad is electrically connected to AGND.
12	SS	I	Soft-start control	An external capacitor and an internal 20-µA current source set the soft-start ramp. The SS current source is reduced to 1 µA initially following a CS2 overcurrent event or an over temperature event.

(1) P = power, G = ground, I = input, O = Output, I/O = Input/output

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Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
13	COMP	I	Input to the pulse width modulator	An internal 5-KΩ resistor pullup is provided on this pin. The external opto-coupler sinks current from COMP to control the PWM duty cycle.
14	RT	I	Oscillator timing resistor pin	An external resistor connected from RT to ground sets the internal oscillator frequency.
15	SYNC	I	Oscillator UP and DOWN synchronization input	The internal oscillator can be synchronized to an external clock with a frequency 20% lower than the internal oscillator's free running frequency. There is no constraint on the maximum sync frequency.
16	UVLO	I	Line undervoltage shutdown	An external voltage divider from the power source sets the shutdown comparator levels. The comparator threshold is 2.5 V. Hysteresis is set by an internal current source (20 µA) that is switched on or off as the UVLO pin potential crosses the 2.5-V threshold.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	V_{IN} to GND	–0.3	100	V
	V_{CC} to GND	–0.3	16	
CS1, CS2 to GND		–0.3	1	V
All other inputs to GND		–0.3	7	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[1]	Human-body model (HBM), per ANSI/ESDA/JEDEC JS01[2]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[3]	±500	

(1) For detailed information on soldering plastic TSSOP and WSON packages, refer to the Packaging Data Book.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN} voltage	13		90	V
External voltage applied to V_{CC}	8		15	V
Operating junction temperature	–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		LM5025 PW (TSSOP) 16-PINS	LM5025 NHQ (WSON) 16-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.7	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.8	25.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.3	9.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.6	9.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Specifications are T_J = 25°C. Unless otherwise specified: V_{IN} = 48 V, V_{CC} = 10 V, RT = 31.3 kΩ, R_{SET} = 27.4 kΩ[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STARTUP REGULATOR							
V_{CC} Reg	V_{CC} regulation	No load	T_J = 25°C		7.6		V
			T_J = –40°C to 125°C	7.3		7.9	
	V_{CC} current limit[2]		T_J = 25°C		25		mA
			T_J = –40°C to 125°C	20			
I-V_{IN}	Startup regulator leakage (external Vcc Supply)	V_{IN} = 100 V	T_J = 25°C		165		µA
			T_J = –40°C to 125°C			500	
	Shutdown current (Iin)	UVLO = 0 V	T_J = 25°C		350		µA
			T_J = –40°C to 125°C			450	
V_{CC} SUPPLY							
	V_{CC} undervoltage lockout voltage (positive going V_{cc})	T_J = 25°C			V_{CC} Reg – 120 mV		V
		T_J = –40°C to 125°C		V_{CC} Reg – 220 mV			
	V_{CC} undervoltage hysteresis	T_J = 25°C			1.5		V
		T_J = –40°C to 125°C		1		2	
	V_{CC} supply current (I_{CC})	C_{gate} = 0	T_J = –40°C to 125°C			4.2	mA
REFERENCE SUPPLY							
V_{REF}	Ref voltage	I_{REF} = 0 mA	T_J = 25°C		5		V
			T_J = –40°C to 125°C	4.85		5.15	
	Ref voltage regulation	I_{REF} = 0 to 10 mA	T_J = 25°C		25		mV
			T_J = –40°C to 125°C			50	
	Ref current limit	T_J = 25°C			20		mA
		T_J = –40°C to 125°C		10			
CURRENT LIMIT							
CS1 Prop	CS1 delay to output	CS1 step from 0 to 0.4 V, Time to onset of OUT transition (90%), C_{gate} = 0			40		ns
CS2 Prop	CS2 delay to output	CS2 step from 0 to 0.4 V, Time to onset of OUT transition (90%), C_{gate} = 0			50		ns
	Leading edge blanking time				50		ns
	Cycle by cycle threshold voltage (CS1)	T_J = 25°C			0.25		V
		T_J = –40°C to 125°C		0.22		0.28	
	Cycle skip threshold voltage (CS2)	Resets SS capacitor; auto restart	T_J = 25°C		0.25		V
			T_J = –40°C to 125°C	0.22		0.28	

(1) All electrical characteristics having room temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Device thermal limitations may limit usable range.

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Electrical Characteristics (continued)

Specifications are T_J = 25°C. Unless otherwise specified: V_{IN} = 48 V, V_{CC} = 10 V, RT = 31.3 kΩ, R_{SET} = 27.4 kΩ(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CS sink impedance (clocked)	I_{CS} = 10 mA	T_J = 25°C		30		Ω
		T_J = –40°C to 125°C			50	
SOFT-START						
Soft-start current source normal	T_J = 25°C			22		µA
	T_J = –40°C to 125°C		17		27	
Soft-start current source following a CS2 event	T_J = 25°C			1		µA
	T_J = –40°C to 125°C		0.5		1.5	
OSCILLATOR						
Frequency1		T_J = 25°C	180	200	220	kHz
		T_J = –40°C to 125°C	175		225	
Frequency2	RT = 10.4 KΩ	T_J = 25°C		580		kHz
		T_J = –40°C to 125°C	500		660	
Sync frequency	T_J = –40°C to 125°C		160			kHz
Sync threshold				2		V
Minimum sync pulse width	T_J = –40°C to 125°C				100	ns
PWM COMPARATOR						
Delay to output	COMP step 5 V to 0 V, Time to onset of OUT_A transition low			40		ns
Duty cycle	T_J = –40°C to 125°C		0%		80%	
COMP to PWM offset	T_J = 25°C			1		V
	T_J = –40°C to 125°C		0.7		1.3	
COMP open circuit voltage	T_J = –40°C to 125°C		4.3		5.9	V
COMP short circuit current	COMP = 0 V	T_J = 25°C		1		mA
		T_J = –40°C to 125°C	0.6		1.4	
VOLT × SECOND CLAMP						
Ramp clamp level	Delta RAMP measured from onset of OUT_A to Ramp peak, COMP = 5 V	T_J = 25°C		2.5		V
		T_J = –40°C to 125°C	2.4		2.6	
UVLO SHUTDOWN						
Undervoltage shutdown threshold	T_J = 25°C			2.5		V
	T_J = –40°C to 125°C		2.44		2.56	
Undervoltage shutdown hysteresis	T_J = 25°C			20		µA
	T_J = –40°C to 125°C		16		24	
OUTPUT SECTION						
OUT_A high saturation	MOS device at Iout = –10 mA	T_J = 25°C		5		Ω
		T_J = –40°C to 125°C			10	
OUT_A low saturation	MOS device at Iout = 10 mA	T_J = 25°C		6		Ω
		T_J = –40°C to 125°C			9	
OUT_B high saturation	MOS device at Iout = –10 mA	T_J = 25°C		10		Ω
		T_J = –40°C to 125°C			20	
OUT_B low saturation	MOS device at Iout = 10 mA	T_J = 25°C		12		Ω
		T_J = –40°C to 125°C			18	
OUTPUT_B peak current sink	Bipolar device at Vcc/2			1		A
OUTPUT_A peak current sink	Bipolar device at Vcc/2			3		A
OUTPUT_A rise time	C_{gate} = 2.2 nF			20		ns
OUTPUT_A fall time	C_{gate} = 2.2 nF			15		ns
OUTPUT_B rise time	C_{gate} = 1 nF			20		ns
OUTPUT_B fall time	C_{gate} = 1 nF			15		ns

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Electrical Characteristics (continued)

Specifications are T_J = 25°C. Unless otherwise specified: V_{IN} = 48 V, V_{CC} = 10 V, RT = 31.3 kΩ, R_{SET} = 27.4 kΩ(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT TIMING CONTROL							
	Overlap time	R_{SET} = 38 kΩ connected to GND, 50% to 50% transitions	T_J = 25°C		105		ns
			T_J = –40°C to 125°C	75		135	
	Deadtime	R_{SET} = 29.5 kΩ connected to REF, 50% to 50% transitions	T_J = 25°C		105		ns
			T_J = –40°C to 125°C	75		135	
THERMAL SHUTDOWN							
T_{SD}	Thermal shutdown threshold				165		°C
	Thermal shutdown hysteresis				25		°C

6.6 Typical Characteristics

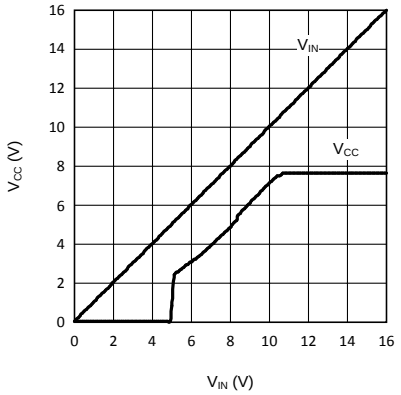

Figure 1. V_{CC} Regulator Start-Up Characteristics, V_{CC} vs Vin

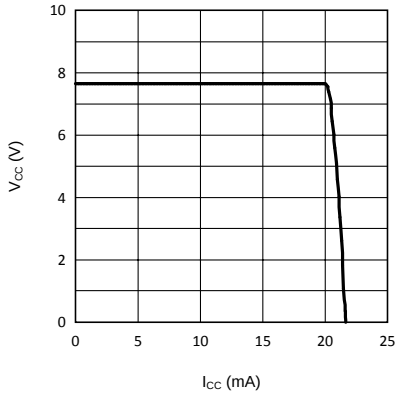

Figure 2. V_{CC} vs I_{CC}

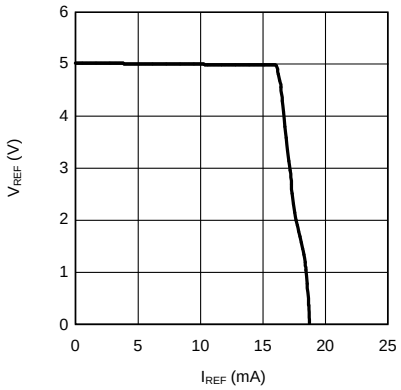

Figure 3. V_{REF} vs I_{REF}

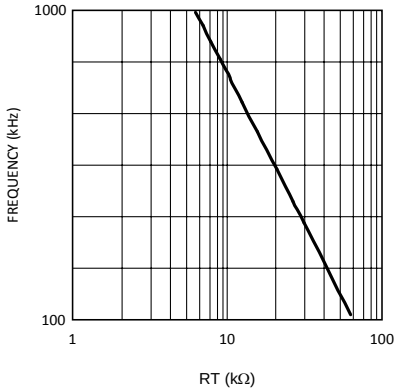

Figure 4. Oscillator Frequency vs RT

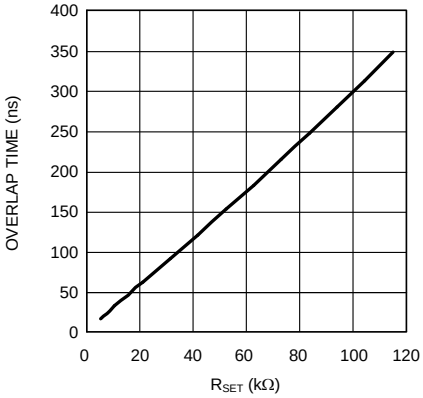

Figure 5. Overlap Time vs R_{SET}

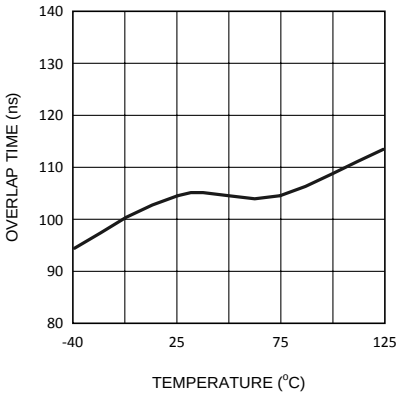

Figure 6. Overlap Time vs Temperature R_{SET} = 38 K

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Typical Characteristics (continued)

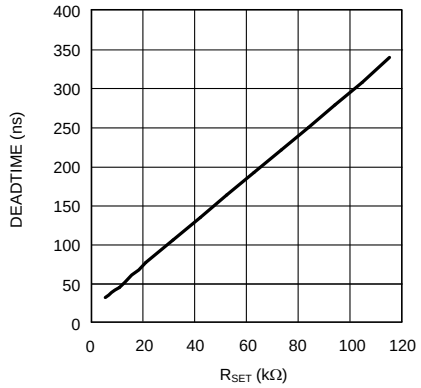

Figure 7. Dead Time vs R_{SET}

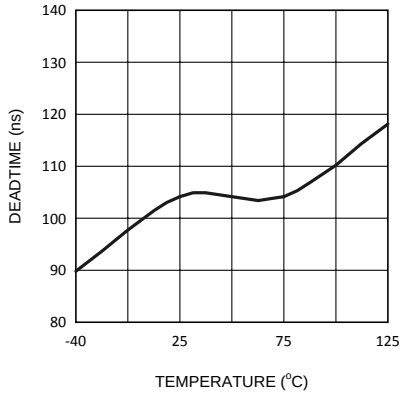

Figure 8. Dead Time vs Temperature R_{SET} = 29.5 K

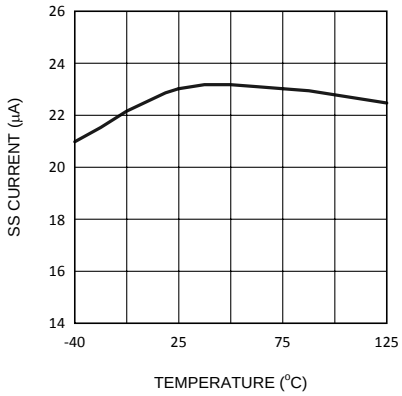

Figure 9. SS Pin Current vs Temperature

7 Detailed Description

7.1 Overview

The LM5025 PWM controller contains all of the features necessary to implement power converters using the active clamp reset technique. The device can be configured to control either a P-channel clamp switch or an N-channel clamp switch. With the active clamp technique higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp and reset techniques. Two control outputs are provided, the main power switch control (OUT_A), and the active clamp switch control (OUT_B). The active clamp output can be configured for either a specified overlap time (for P-channel switch applications) or a specified dead time (for N_channel applications). The two internal compound gate drivers parallel both MOS and bipolar devices, providing superior gate-drive characteristics. This controller is designed for high-speed operation including an oscillator frequency range up to 1 MHz and total PWM and current sense propagation delays less than 100 ns. The LM5025 includes a high-voltage start-up regulator that operates over a wide input of 13 V to 90 V. Additional features include: line undervoltage lockout (UVLO), soft-start, oscillator UP and DOWN sync capability, precision reference and thermal shutdown.

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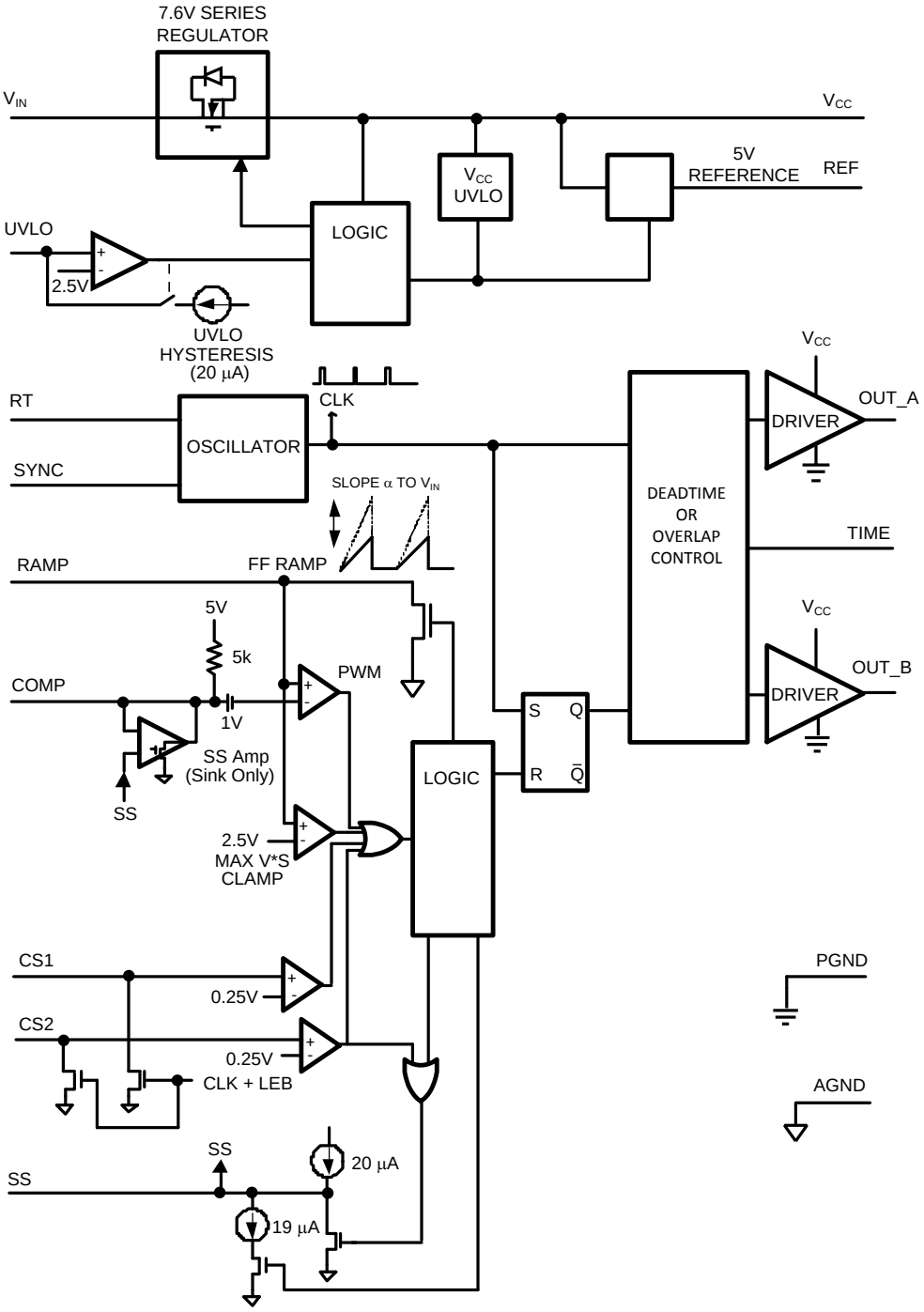
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Voltage Start-Up Regulator

The LM5025 contains an internal high-voltage start-up regulator that allows the input pin (V_{IN}) to be connected directly to the line voltage. The regulator output is internally current limited to 20 mA. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. The recommended capacitance for the V_{CC} regulator is 0.1 µF to 100 µF. When the voltage on the V_{CC} pin reaches the regulation point of 7.6 V and the internal voltage reference (REF) reaches its regulation point of 5 V, the controller outputs are enabled. The outputs remains enabled until V_{CC} falls below 6.2 V or the line undervoltage lock out detector indicates that V_{IN} is out of range. In typical applications, an auxiliary transformer winding is connected through a diode to the V_{CC} pin. This winding must raise the V_{CC} voltage above 8 V to shut off the internal start-up regulator. Powering V_{CC} from an auxiliary winding improves efficiency while reducing the controller power dissipation.

The external V_{CC} capacitor must be sized such that the capacitor and V_{CC} self-bias maintains a V_{CC} voltage greater than 6.2 V during the initial start-up. During a fault mode when the converter auxiliary winding is inactive, external current draw on the V_{CC} line must be limited so the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the controller.

An external start-up regulator or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the V_{IN} pins together and feeding the external bias voltage into the two pins.

7.3.2 Line Undervoltage Detector

The LM5025 contains a line undervoltage lock out (UVLO) circuit. An external set-point voltage divider from Vin to GND, sets the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin is greater than 2.5 V when Vin is in the desired operating range. If the undervoltage threshold is not met, all functions of the controller are disabled and the controller remains in a low-power standby state. UVLO hysteresis is accomplished with an internal 20-µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.5-V threshold, the current source is turned off, causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable and disable function. Pulling the UVLO pin below the 2.5-V threshold disables the converter.

7.3.3 PWM Outputs

The relative phase of the main (OUT_A) and active clamp outputs (OUT_B) can be configured for the specific application. For active clamp configurations using a ground referenced P-channel clamp switch, the two outputs must be in phase with the active clamp output overlapping the main output. For active clamp configurations using a high side N-channel switch, the active clamp output must be out of phase with main output and there must be a dead time between the two gate drive pulses. A distinguishing feature of the LM5025 is the ability to accurately configure either dead time (both off) or overlap time (both on) of the gate driver outputs. The overlap and deadtime magnitude is controlled by the resistor value connected to the TIME pin of the controller. The opposite end of the resistor can be connected to either REF for deadtime control or GND for overlap control. The internal configuration detector senses the connection and configures the phase relationship of the main and active clamp outputs.

7.3.4 Compound Gate Drivers

The LM5025 contains two unique compound gate drivers, which parallel both MOS and bipolar devices to provide high-drive current throughout the entire switching event. The bipolar device provides most of the drive current capability and provides a relatively constant sink current that is ideal for driving large power MOSFETs. As the switching event nears conclusion and the bipolar device saturates, the internal MOS device continues to provide a low-impedance to compete the switching event.

During turnoff at the Miller plateau region, typically around 2 V to 3 V, is where gate driver current capability is needed most. The resistive characteristics of all MOS gate drivers are adequate for turnon, because the supply to output voltage differential is fairly large at the Miller region. During turnoff however, the voltage differential is small and the current source characteristic of the bipolar gate driver is beneficial to provide fast drive capability.

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Feature Description (continued)

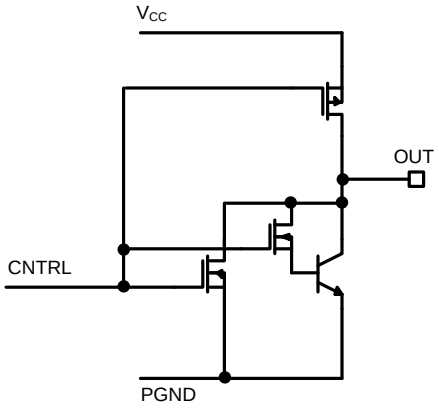

Figure 10. Compound Gate Drivers

7.3.5 PWM Comparator

The PWM comparator compares the ramp signal (RAMP) to the loop error signal (COMP). This comparator is optimized for speed to achieve minimum controllable duty cycles. The internal 5-kΩ pullup resistor, connected between the internal 5-V reference and COMP can be used as the pullup for an optocoupler. The comparator polarity is such that 0 V on the COMP pin produces a zero-duty cycle on both gate driver outputs.

7.3.6 Volt Second Clamp

The volt × second clamp comparator compares the ramp signal (RAMP) to a fixed 2.5-V reference. By proper selection of RFF and CFF, the maximum ON time of the main switch can be set to the desired duration. The ON time set by volt × second clamp varies inversely with the line voltage because the RAMP capacitor is charged by a resistor connected to Vin while the threshold of the clamp is a fixed voltage (2.5 V).

The C_{FF} ramp capacitor is discharged at the conclusion of every cycle by an internal discharge switch controlled by either the internal clock or by the V × S Clamp comparator, whichever event occurs first.

7.3.7 Current Limit

The LM5025 contains two modes of overcurrent protection. If the sense voltage at the CS1 input exceeds 0.25 V the present power cycle is terminated (cycle-by-cycle current limit). If the sense voltage at the CS2 input exceeds 0.25 V, the controller terminates the present cycle, discharge the soft-start capacitor and reduce the soft-start current source to 1 µA. The soft-start (SS) capacitor is released after being fully discharged and slowly charges with a 1-µA current source. When the voltage at the SS pin reaches approximately 1 V, the PWM comparator produces the first output pulse at OUT_A. After the first pulse occurs, the soft-start current source reverts to the normal 20-µA level. Fully discharging and then slowly charging the SS capacitor protects a continuously overloaded converter with a low-duty cycle hiccup mode.

These two modes of overcurrent protection allows the user great flexibility to configure the system behavior in overload conditions. If it is desired for the system to act as a current source during an overload, then the CS1 cycle-by-cycle current limiting must be used. In this case the current sense signal must be applied to the CS1 input and the CS2 input must be grounded. If during an overload condition it is desired for the system to briefly shutdown, followed by soft-start retry, then the CS2 hiccup current limiting mode must be used. In this case the current sense signal must be applied to the CS2 input and the CS1 input must be grounded. This shutdown and soft-start retry repeats indefinitely while the overload condition remains. The hiccup mode greatly reduces the thermal stresses to the system during heavy overloads. The cycle-by-cycle mode has higher system thermal dissipations during heavy overloads, but provides the advantage of continuous operation for short duration overload conditions.

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Feature Description (continued)

In some systems it is possible use both modes concurrently, whereby slight overload conditions activate the CS1 cycle-by cycle mode, while more severe overloading activates the CS2 hiccup mode. Operating both modes concurrently requires that the slope of the inductor current be sufficient to reach the CS2 threshold before the CS1 function turns off the main output switch. This requires a high dv/dt at the current sense pin. The signal must be fast enough to reach the second-level threshold before the first threshold detector (CS1) turns off the gate driver. Excessive filtering on the CS pin, an extremely low-value current sense resistor or an inductor that does not saturate with excessive loading may prevent the second-level threshold from ever being reached.

TI recommends a small RC filter, located near the controller, for each of the CS pins. Each CS input has an internal FET that discharges the current sense filter capacitor at the conclusion of every cycle, to improve dynamic performance. This same FET remains on an additional 50 ns at the start of each main switch cycle to attenuate the leading edge spike in the current sense signal.

The LM5025 CS comparators are very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and GND). If a current sense transformer is used, both leads of the transformer secondary must be routed to the filter network , which must be located close to the IC. If a sense resistor in the source of the main switch MOSFET is used for current sensing, a low-inductance type of resistor is required. When designing with a current sense resistor, all of the noise sensitive low-power ground connections must be connected together near the IC GND and a single connection must be made to the power ground (sense resistor ground point).

Figure 11. Current Limit

7.3.8 Oscillator and Sync Capability

The LM5025 oscillator is set by a single external resistor connected between the RT pin and GND.

The RT resistor must be located very close to the device and connected directly to the pins of the IC (RT and GND).

A unique feature of LM5025 is the ability to synchronize the oscillator to an external clock with a frequency that is either higher or lower than the frequency of the internal oscillator. The lower frequency sync frequency range is 80% of the free running internal oscillator frequency. There is no constraint on the maximum SYNC frequency. A minimum pulse width of 100 ns is required for the synchronization clock . If the synchronization feature is not required, the SYNC pin must be connected to GND to prevent any abnormal interference. The internal oscillator can be completely disabled by connecting the RT pin to REF. Once disabled, the sync signal acts directly as the master clock for the controller. Both the frequency and the maximum duty cycle of the PWM controller can be controlled by the SYNC signal (within the limitations of the volt × second clamp). The maximum duty cycle (D) is (1D) of the SYNC signal.

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Feature Description (continued)

7.3.9 Feed-Forward Ramp

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to V_{IN} and GND are required to create the PWM ramp signal. The slope of the signal at the RAMP pin varies in proportion to the input line voltage. This varying slope provides line feedforward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal at the COMP pin by the pulse width modulator comparator to control the duty cycle of the main switch output. The volt second clamp comparator also monitors the RAMP pin and if the ramp amplitude exceeds 2.5 V the present cycle is terminated. The ramp signal is reset to GND at the end of each cycle by either the internal clock or the volt second comparator, whichever occurs first.

7.3.10 Soft-Start

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. At power on, a 20-µA current is sourced out of the soft-start pin (SS) into an external capacitor. The capacitor voltage ramps up slowly and limits the COMP pin voltage and therefore the PWM duty cycle. In the event of a fault as determined by V_{CC} undervoltage, line undervoltage (UVLO), or second-level current limit, the output gate drivers are disabled and the soft-start capacitor is fully discharged. When the fault condition is no longer present a soft-start sequence is initiated. Following a second-level current limit detection (CS2), the soft-start current source is reduced to 1 µA until the first output pulse is generated by the PWM comparator. The current source returns to the nominal 20-µA level after the first output pulse (approximately 1 V at the SS pin).

7.3.11 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low-power standby state with the output drivers and the bias regulator disabled. The device restarts after the thermal hysteresis (typically 25°C). During a restart after thermal shutdown, the soft-start capacitor is fully discharged and then charged in the low-current mode (1 µA) similar to a second-level current limit event. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating.

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7.4 Device Functional Modes

The LM5025 active clamp voltage mode PWM controller has six functional modes. The modes transition diagram is shown in Figure 12.

- UVLO Mode
- Soft-Start Mode
- Normal Operation Mode
- Cycle-by-Cycle Current Limit Mode
- Hiccup Mode
- Thermal Shut Down Mode

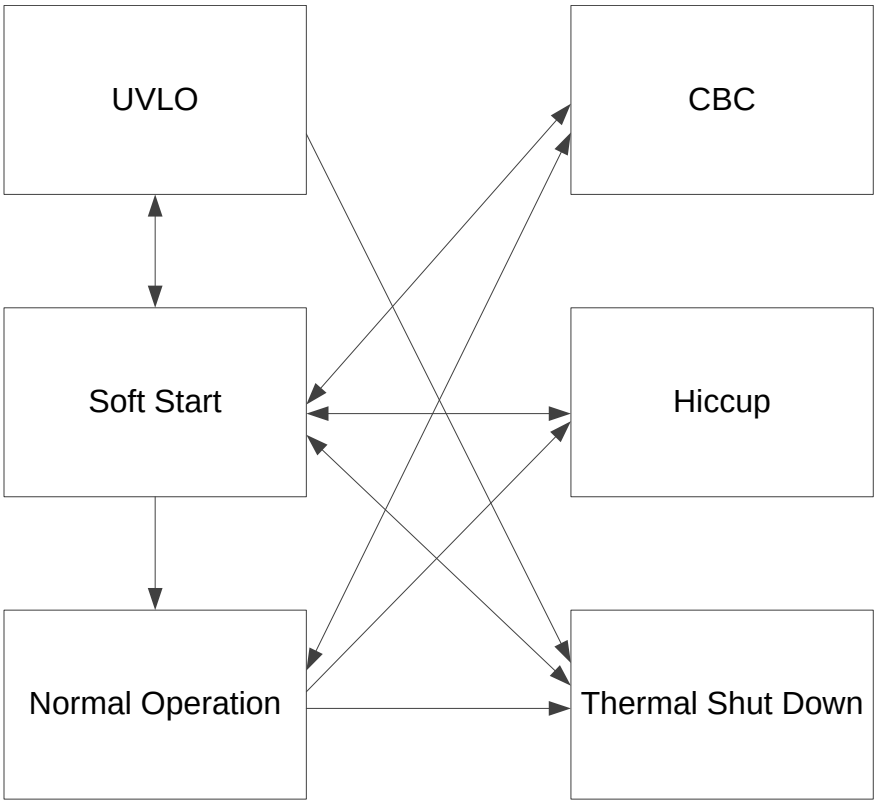

Figure 12. Functional Mode Transition Diagram

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5025 PWM controller contains all of the features necessary to implement power converters using the active clamp and reset technique. This section provides design guidance for a typical active clamp forward converter design. An actual application schematic of a 36-V to 78-V input, 3.3-V, 30-A output active clamp forward converter is also provided in Figure 21.

8.2 Typical Application

Figure 13 shows a simplified schematic of an active clamp forward power converter.

Power converters based on the forward topology offer high-efficiency and good power-handling capability in applications up to several hundred Watts. The operation of the transformer in a forward topology does not inherently self-reset each power switching cycle, a mechanism to reset the transformer is required. The active clamp reset mechanism is presently finding extensive use in medium-level power converters in the 50 W to 200 W range.

The forward converter is derived from the Buck topology family, employing a single modulating power switch. The main difference between the topologies is the forward topology employs a transformer to provide input and output ground isolation and a step down or step up function.

Each cycle, the main primary switch turns on and applies the input voltage across the primary winding. The transformer turns the voltage to a lower-level on the secondary side. The clamp capacitor along with the reset switch reverse biases the transformer primary each cycle when the main switch turns off. This reverse voltage resets the transformer. The clamp capacitor voltage is VIN / (1-D).

The secondary rectification employs self-driven synchronous rectification to maintain high-efficiency and ease of drive.

Feedback from the output is processed by an amplifier and reference, generating an error voltage, which is coupled back to the primary side control through an opto-coupler. The LM5025 voltage mode controller pulse width modulates the error signal with a ramp signal derived from the input voltage. Deriving the ramp signal slope from the input voltage provides line feed-forward, which improves line transient rejection. The LM5025 also provides a controlled delay necessary for the reset switch.

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Typical Application (continued)

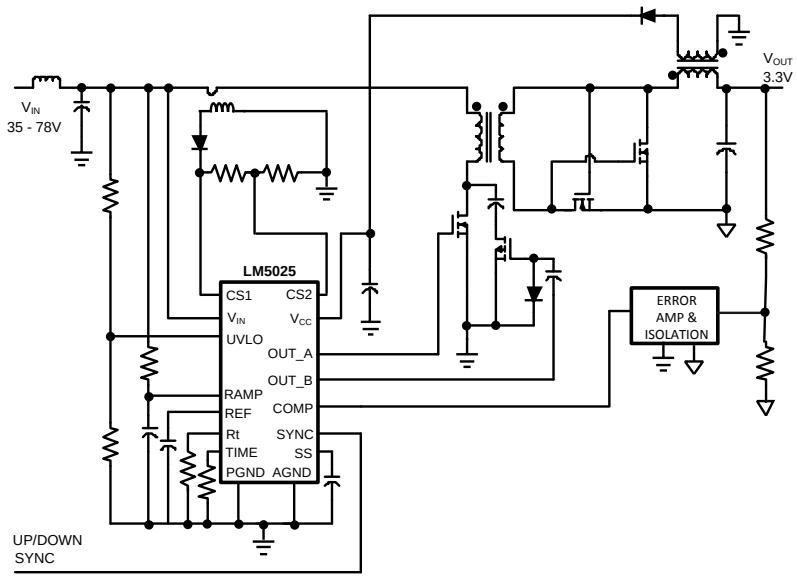

Figure 13. Simplified Active Clamp Forward Power Converter

8.2.1 Design Requirements

This typical application provides an example of a fully-functional power converter based on the active clamp forward topology in an industry standard half-brick footprint.

The design requirements are:

- Input: 36 V to 78 V (100-V peak)
- Output Voltage: 3.3 V
- Output Current: 0 A to 30 A
- Measured Efficiency: 90.5% at 30 A, 92.5% at 15 A
- Frequency of Operation: 230 kHz
- Board Size: 2.3 × 2.4 × 0.5 inches
- Load Regulation: 1%
- Line Regulation: 0.1%
- Line UVLO, Hiccup Current Limit

8.2.2 Detailed Design Procedure

Before the controller design begins, the power stage design must be completed. This section describes the calculations needed to configure the LM5025 controller to meet the power stage design requirements.

8.2.2.1 Oscillator

The desired switching frequency F is set by a resistor connected between RT pin and ground. The resistance value R_T is calculated from Equation 1:

$$R_T = (5725/F)^{1.026} \quad (1)$$

where

- F is in kHz and R_T in kΩ.

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Typical Application (continued)

8.2.2.2 Soft-Start Ramp Time and Hiccup Interval

The soft-start ramp time and hiccup internal is programmed by a capacitor (C_{SS}) on the SS pin to ground. The soft-start ramp time is determined by comparing the SS pin voltage with COMP pin voltage. When the SS voltage is less than COMP voltage, the COMP voltage is clamped by SS voltage. The PWM duty is limited by the clamped COMP voltage, so that soft-start can be achieved. The first PWM pulse is generated after COMP voltage reaches 1 V. So the soft-start ramp time of the output voltage can be estimated by Equation 2:

$$T_{SS}(\text{ms}) = C_{SS}(\text{nF}) \times \frac{V_{SS} - 1\,\text{V}}{20\,\mu\text{A}}$$

where

- V_{SS} is the steady state COMP pin voltage. This voltage is determined by the output voltage, voltage divider, and the compensation network. (2)

In hiccup mode, the SS current source is reduced to 1 µA. When the first PWM pulse is generated, the current source switches to 20 µA, and the power supply tries to start up again. The hiccup interval can be calculated by Equation 3:

$$T_{hiccup}(\text{ms}) = C_{SS}(\text{nF}) \times \frac{1\,\text{V}}{1\,\mu\text{A}} \quad (3)$$

8.2.2.3 Feed-Forward Ramp and Maximum On Time Clamp

An example illustrates the use of the Volt × Second Clamp comparator to achieve a 50% duty cycle limit, at 200 KHz, at a 48-V line input: A 50% duty cycle at a 200 KHz requires a 2.5 µs of ON time. At 48-V input the Volt × Second product is 120 V × µs (48 V × 2.5 µs). To achieve this clamp level, see Equation 4 and Equation 5:

$$R_{FF} \times C_{FF} = V_{IN} \times T_{ON} / 2.5\,\text{V} \quad (4)$$

$$48 \times 2.5\,\mu\text{F} / 2.5 = 48\,\mu\text{F} \quad (5)$$

Select C_{FF} = 470 pF

R_{FF} = 102 kΩ

The recommended capacitor value range for C_{FF} is 100 pF to 1000 pF.

8.2.2.4 Dead Times

The magnitude of the overlap and dead time can be calculated as follows in Equation 6 and Equation 7:

$$\text{Overlap Time (ns)} = 2.8 \times R_{SET} - 1.2 \quad (6)$$

$$\text{Dead Time (ns)} = 2.9 \times R_{SET} + 20$$

where

- R_{SET} in kΩ, Time in ns (7)

Typical Application (continued)

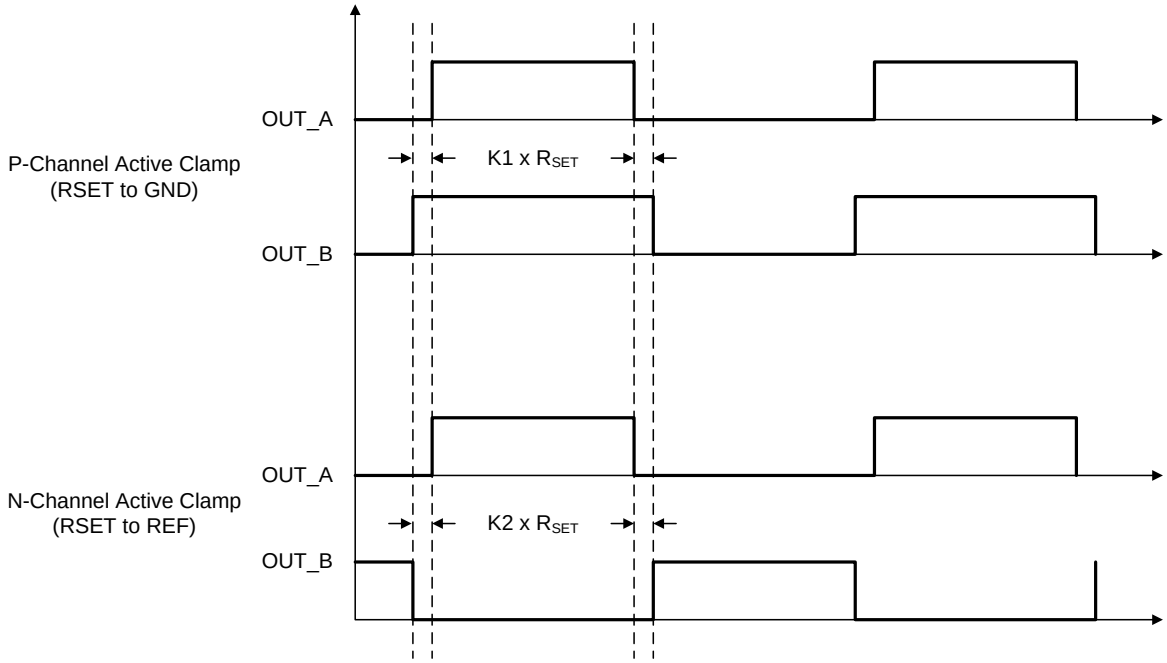

Figure 14. PWM Outputs

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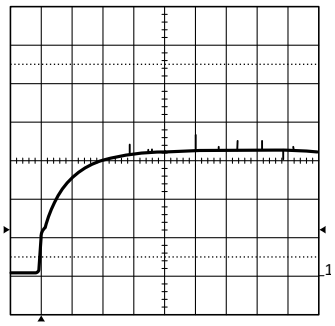
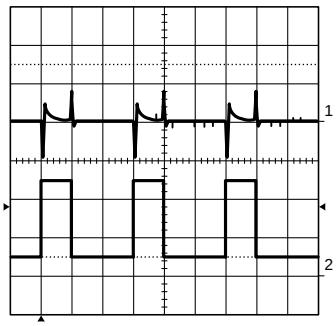
Typical Application (continued)

8.2.3 Application Curves



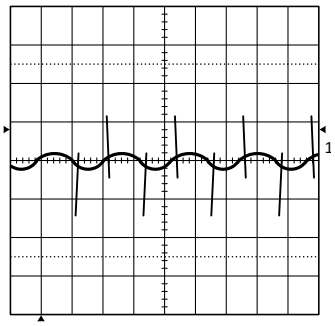
Conditions: input voltage = 48 VDC, output current = 5 A
Trace 1: output voltage Volts/div = 0.5 V
Horizontal resolution = 1 ms/div

Figure 15. Output Voltage During Typical Startup



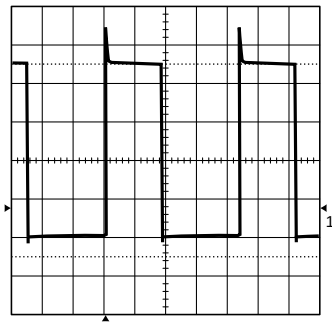
Conditions: input voltage = 48 VDC, output current = 5 A to 25 A
Trace 1: output voltage Volts/div = 0.5 V
Trace 2: output current, Amps/div = 10 A
Horizontal resolution = 1 µs/div

Figure 16. Transient Response



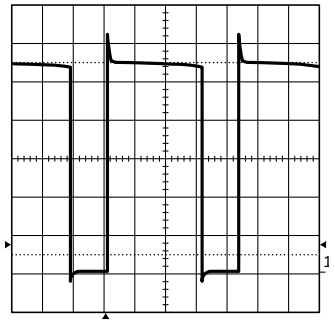
Conditions: input voltage = 48 VDC, output current = 30 A
Bandwidth limit = 25 MHz
Trace 1: output ripple voltage Volts/div = 50 mV
Horizontal resolution = 2 µs/div

Figure 17. Output Ripple



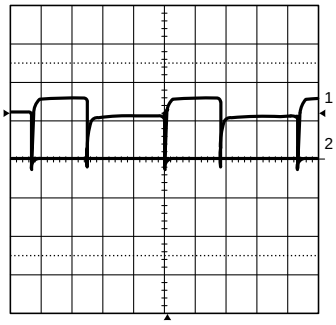
Conditions: input voltage = 38 VDC, output current = 25 A
Trace 1: Q1 drain voltage Volts/div = 20 V
Horizontal resolution = 1 µs/div

Figure 18. Drain Voltage



Conditions: input voltage = 78 VDC, output current = 25 A
Trace 1: Q1 drain voltage Volts/div = 20 V
Horizontal resolution = 1 µs/div

Figure 19. Drain Voltage



Conditions: input voltage = 48 VDC, output current = 5 A
Synchronous rectifier, Q3 gate Volts/div = 5 V
Trace 1: synchronous rectifier, Q3 gate Volts/div = 5 V
Trace 2: synchronous rectifier, Q5 gate Volts/div = 5 V
Horizontal resolution = 1 µs/div

Figure 20. Gate Voltages of the Synchronous Rectifiers

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Typical Application (continued)

8.2.4 System Example

Figure 21 shows an application circuit with 36-V to 78-V input and 3.3-V, 30-A output capability.

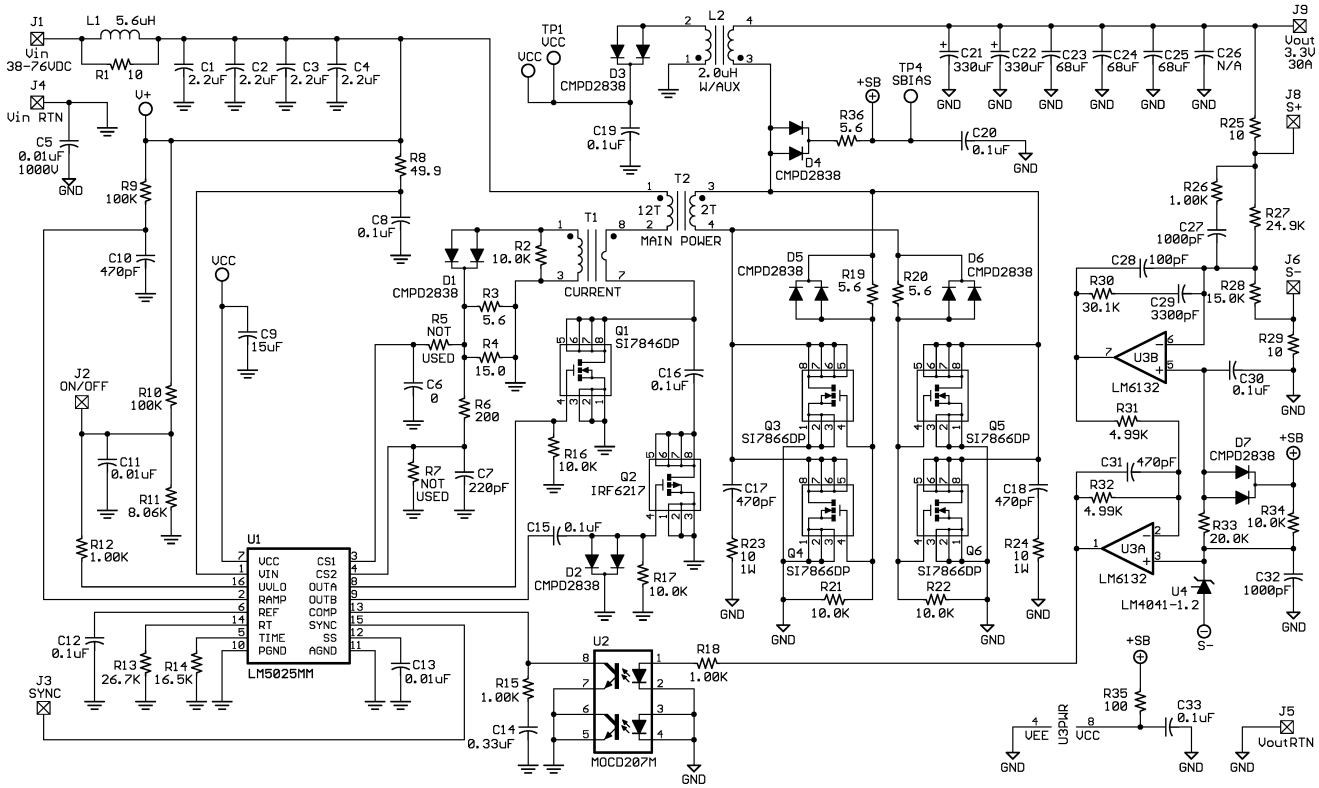

Figure 21. Application Circuit

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9 Power Supply Recommendations

V_{CC} pin is the power supply for the device. There must be a 0.1-µF to approximately 100-µF capacitor directly from V_{CC} to ground. REF pin must be bypassed to ground as close as possible to the device using a 0.1-µF capacitor.

10 Layout

10.1 Layout Guidelines

- Connect two grounds PGND (power ground) and AGND (analog ground) directly as device ground ICGND. The connection must be as close to the pins as possible.
- If there are multiple PCB layers and there is a inner ground layer, use two vias or one big via on GND and connect them to the inner ground layer (ICGND).
- The power stage ground PSGND should be separated with the ICGND. PSGND and ICGND should be connected at a single point close to the device.
- The bypass capacitors to the V_{CC} pin and REF pin should be as close as possible to the pins and ground (ICGND).
- The filtering capacitors connected to CS1 and CS2 pins should have connections as short as possible to ICGND; if an inner ground layer is available, use vias to connect the capacitors to the ground layer (ICGND).
- The resistors and capacitors connected to the timing configuration pins should be as close as possible to the pins and ground (ICGND).

10.2 Layout Example

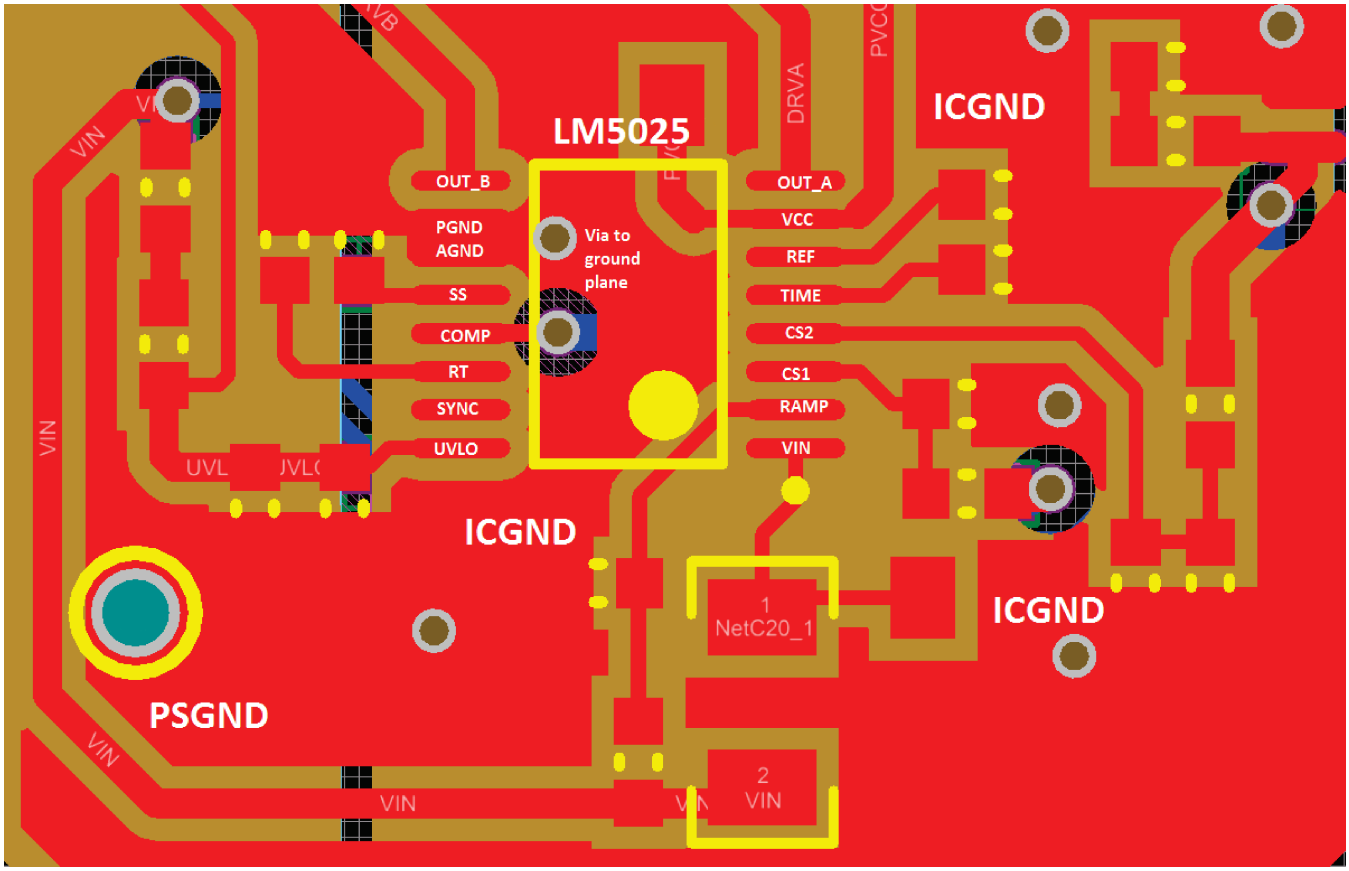

Figure 22. LM5025 Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *LM5025 Isolated Active Clamp Forward Converter Ref Design User Guide*, SNVU096

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5025MTC/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LM5025 MTC	Samples
LM5025MTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LM5025 MTC	Samples
LM5025SD/NOPB	ACTIVE	WSON	NHQ	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5025SD	Samples
LM5025SDX/NOPB	ACTIVE	WSON	NHQ	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5025SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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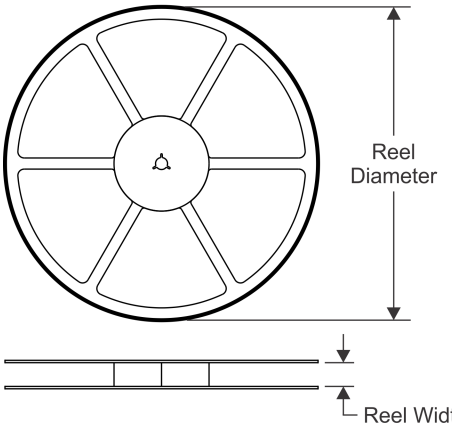
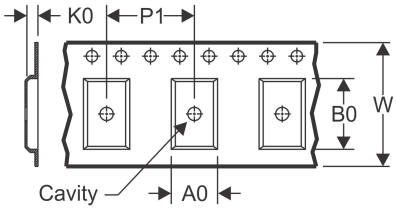
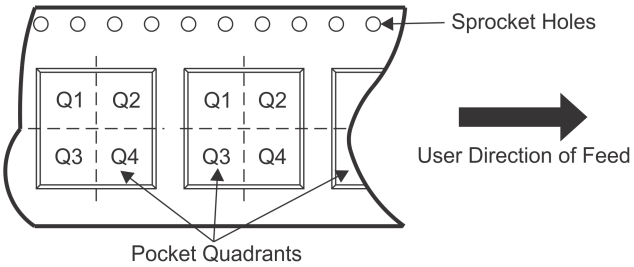


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

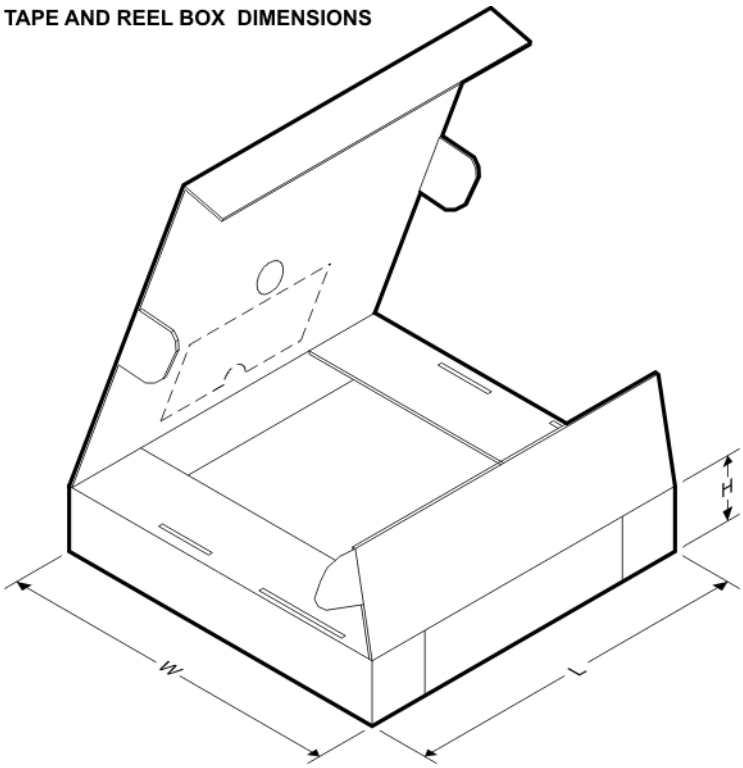
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5025MTCX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5025SD/NOPB	WSON	NHQ	16	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM5025SDX/NOPB	WSON	NHQ	16	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

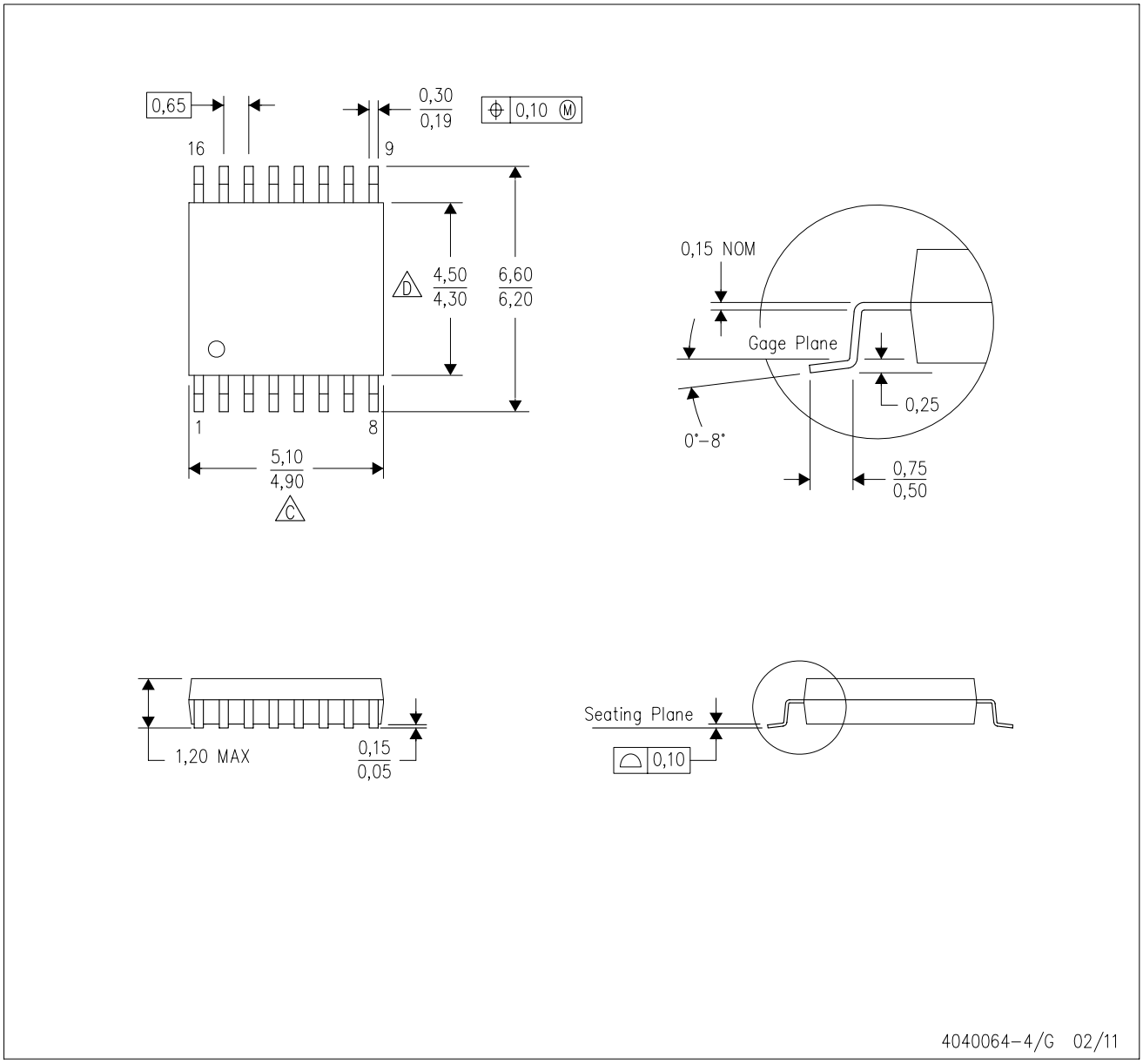
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

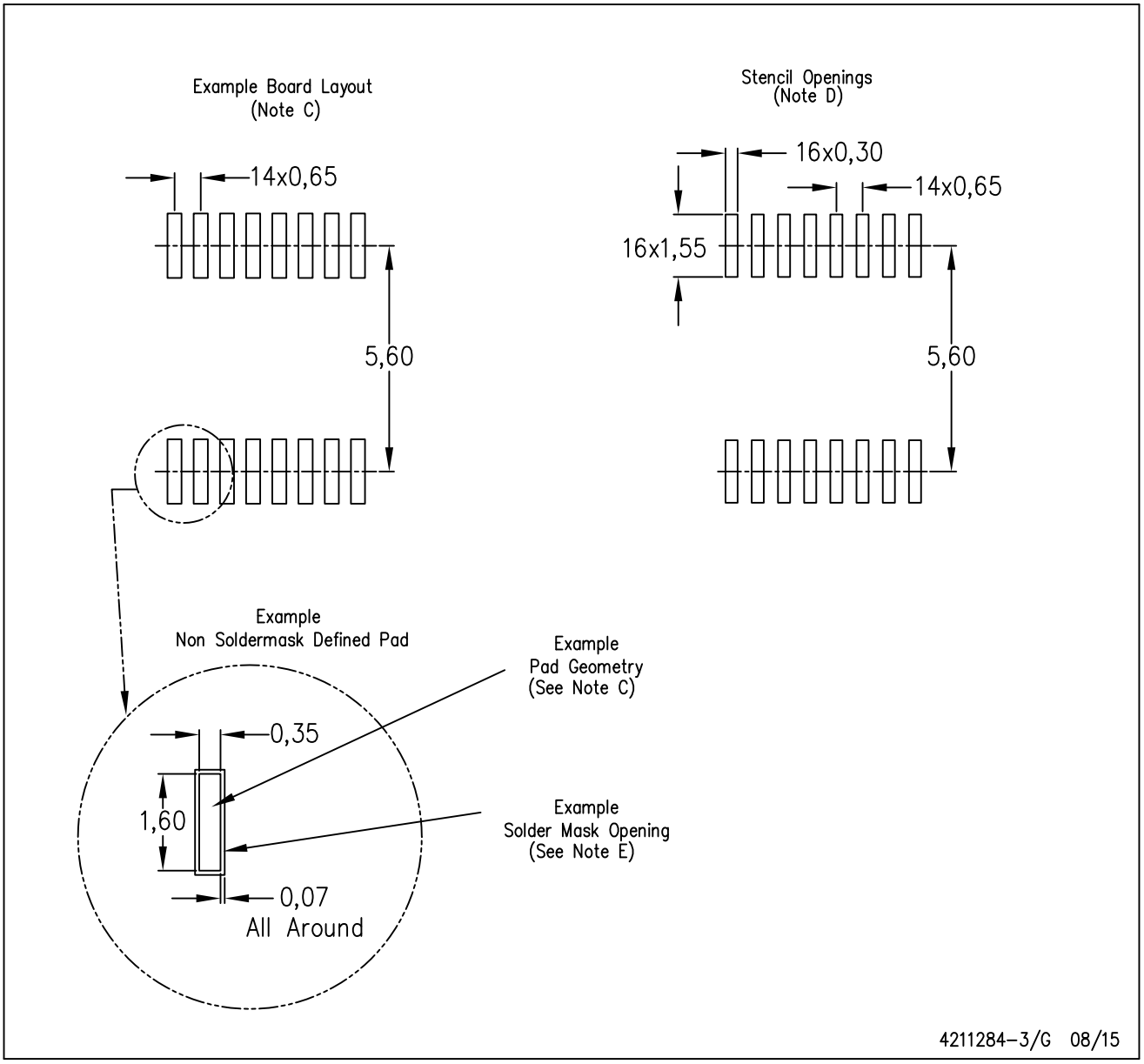
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5025MTCX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5025SD/NOPB	WSON	NHQ	16	1000	210.0	185.0	35.0
LM5025SDX/NOPB	WSON	NHQ	16	4500	367.0	367.0	35.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



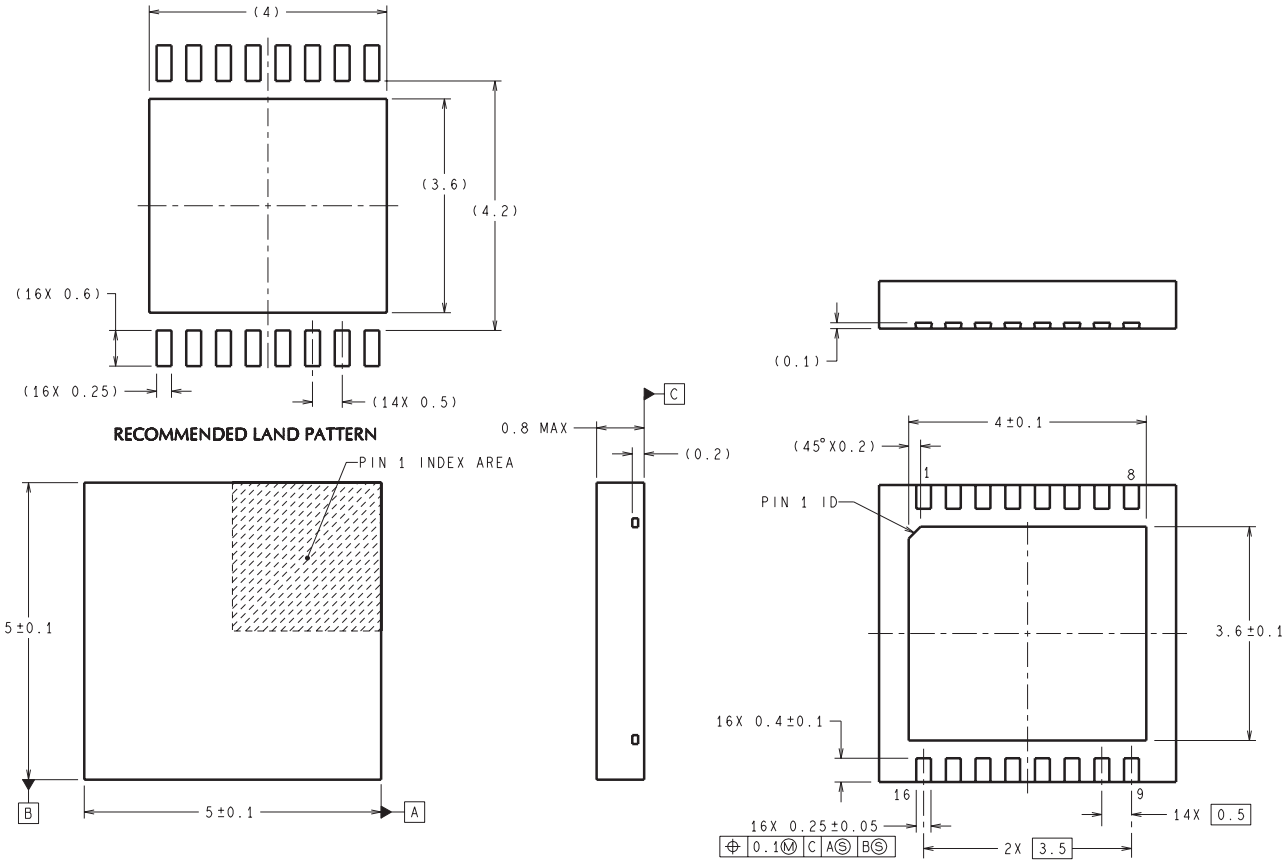
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

NHQ0016A



SDA16A (Rev A)

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