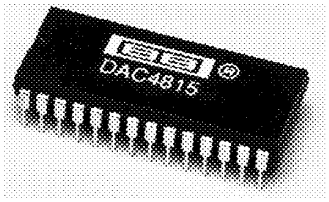
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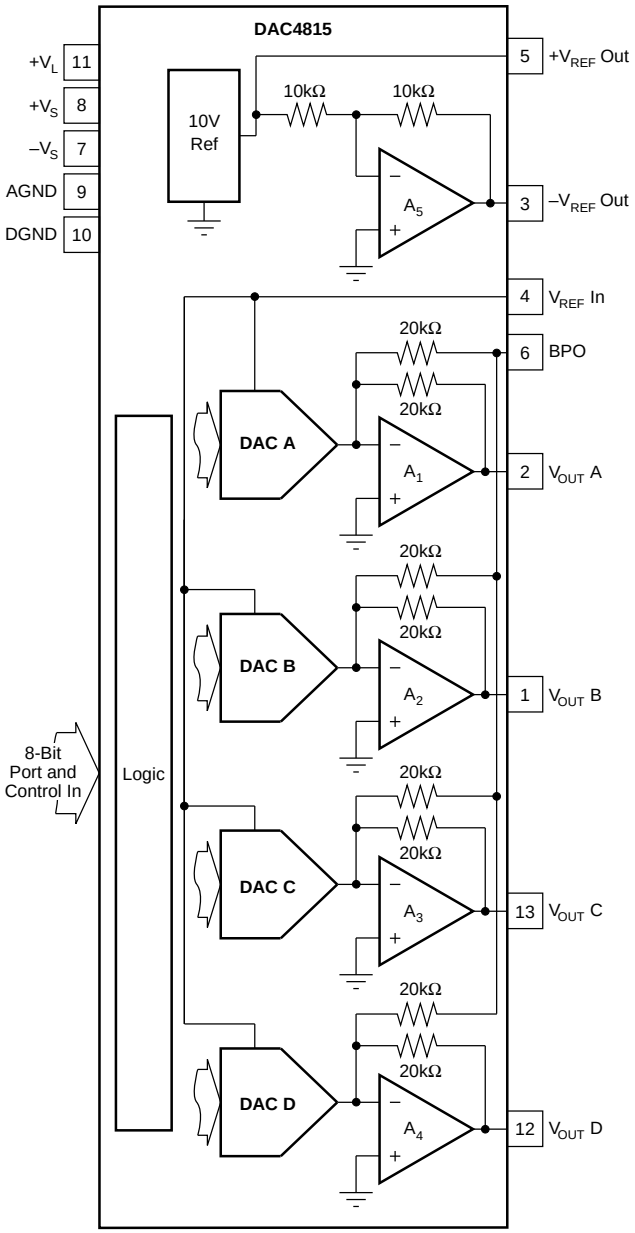


DAC4815

Quad 12-Bit Digital-to-Analog Converter (8-Bit Port Interface)

FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER, 600mW (150mW/DAC)
- LOW GAIN DRIFT, 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- BIPOLAR OUTPUT
- CLEAR/RESET TO BIPOLAR ZERO



DESCRIPTION

The DAC4815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC4815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for bipolar ±10V output range.

The DAC4815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to bipolar zero. This feature is useful for power-on reset or system calibration. The DAC4815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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PDS-1112B
Printed in U.S.A. October, 1993

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4815AP			DAC4815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		2		5	*		*	V
V_{IL} (Input Low Voltage)		0		0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		±1.5/–1				±1	LSB
Bipolar Zero Error			±20			±10	mV	
Gain Error	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V			30			*	ppmFSR/V
	V_L = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift			±5	±30		*	±20	ppm/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			*			mA
	T_A = –40°C to +85°C	+5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			*	ppm/V
(ΔV_{OUT} vs ΔV_S)								
–REFERENCE OUTPUT, Inverter								
–10V Reference		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			30			*		mA
REFERENCE INPUT								
Reference Input Resistance		1.75	2.5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		3.5	5		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[4]	C_L = 100pF							
Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±4			*		mA
DIGITAL CROSSTALK	Full Scale Transition		3			*		nV-s
	C_L= 100pF							
DIGITAL-TO-ANALOG								
GLITCH IMPULSE			30			*		nV-s
POWER SUPPLY								
$+V_S$ and $–V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+20	+24		*	*	mA
$–I_S$			–20	–25.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.4	2		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			10			*	mA
Total Power, All DACs			600	753		*	*	mW

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

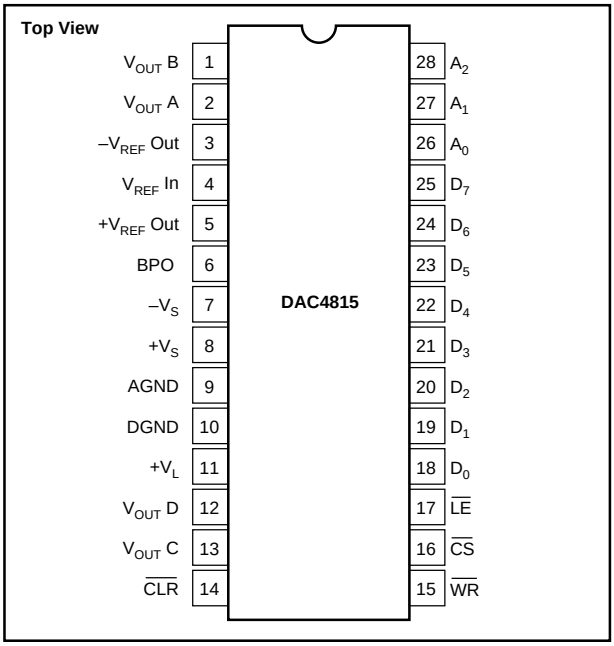
PARAMETER	CONDITIONS	DAC4815AP			DAC4815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes effect of voltage output DAC, voltage references. (4) Guaranteed but not tested.

PIN DESIGNATIONS

PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	V_{OUT} B	Analog output voltage, DAC B	28	A_2	Address line 2 input
2	V_{OUT} A	Analog output voltage, DAC A	27	A_1	Address line 1 input
3	$–V_{REF}$ Out	Negative reference voltage output (–10V output)	26	A_0	Address line 0 input
4	V_{REF} In	± Reference voltage input	25	D_7	Data bit 7 input
5	$+V_{REF}$ Out	Positive reference voltage output (+10V output)	24	D_6	Data bit 6 input
6	BPO	Bipolar offset input, DAC A, B, C, and D	23	D_5	Data bit 5 input
7	$–V_S$	Negative analog power supply, –15V input	22	D_4	Data bit 4 input
8	$+V_S$	Positive analog power supply, +15V input	21	D_3	Data bit 3 input
9	AGND	Analog common	20	D_2	Data bit 2 input
10	DGND	Digital common	19	D_1	Data bit 1 input
11	$+V_L$	Positive logic power supply, +5V input	18	D_0	Data bit 0 input
12	V_{OUT} D	Analog output voltage, DAC D	17	$\overline{LE}$	Latch data enable, DAC A, B, C, and D
13	V_{OUT} C	Analog output voltage, DAC C	16	$\overline{CS}$	Chip select enable, DAC A, B, C, and D
14	$\overline{CLR}$	Asynchronous input reset to zero	15	$\overline{WR}$	Write input, DAC A, B, C, and D

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$–V_S$ to AGND	0V,–18V
AGND to DGND	±0.3V
Any digital input to GND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $±V_S$
Reference Short Circuit	Continuous to common or $+V_S$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	LINEARITY ERROR (LSB)
DAC4815AP	±1
DAC4815BP	±1/2

PACKAGE INFORMATION

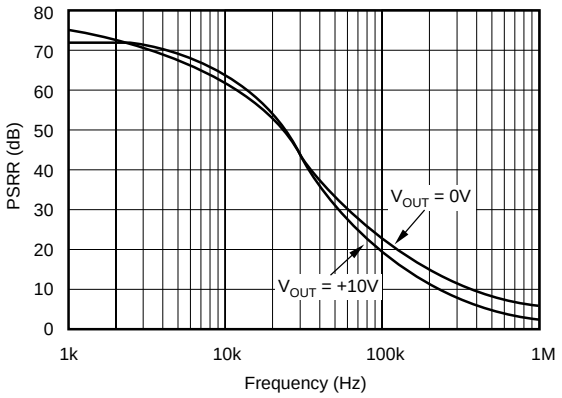
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC4815AP	28-Pin Plastic DIP	215
DAC4815BP	28-PIn Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

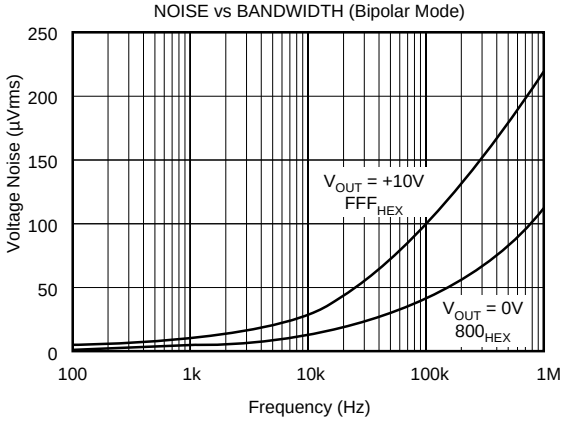
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

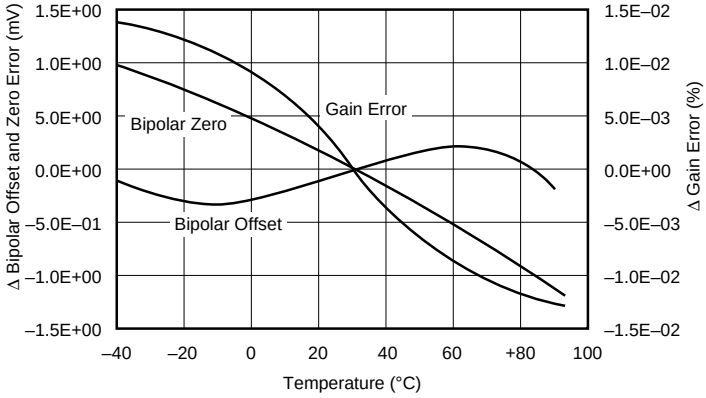
PSRR vs FREQUENCY (Bipolar Mode)



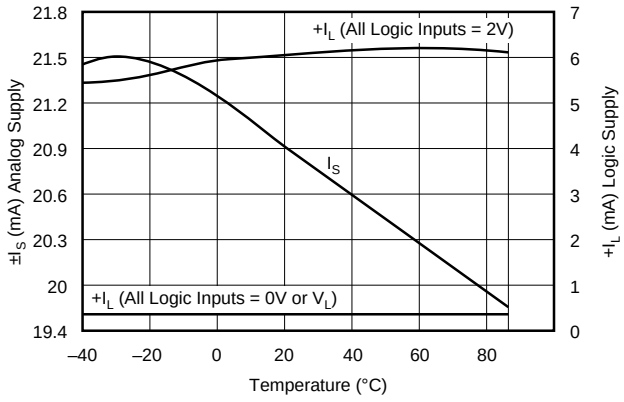
NOISE vs BANDWIDTH (Bipolar Mode)



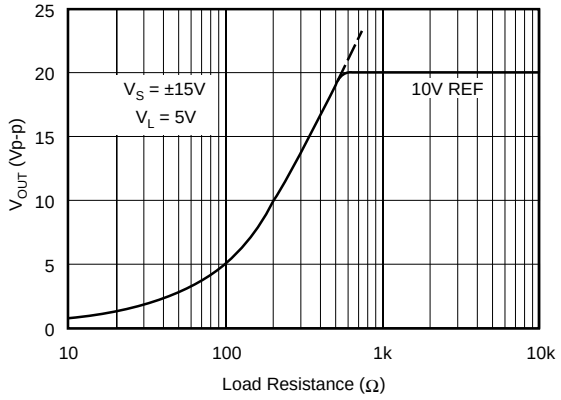
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



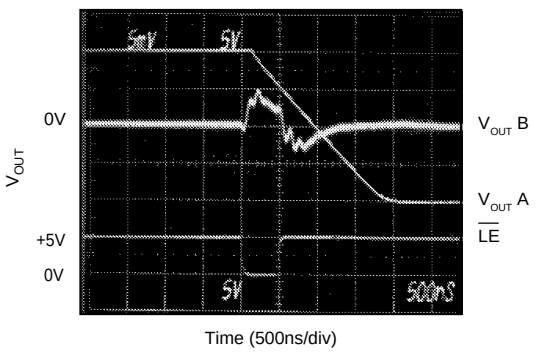
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



CROSSTALK (Bipolar Mode)



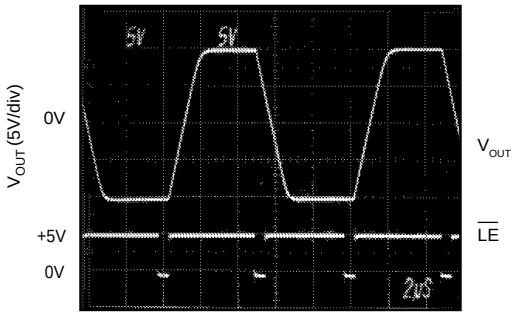
Time (500ns/div)

NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of $\overline{LE}$ signal.

TYPICAL PERFORMANCE CURVES (CONT)

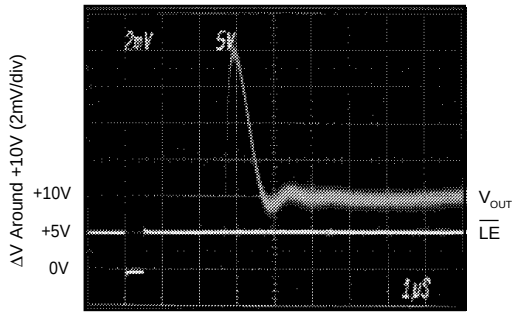
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

FULL-SCALE OUTPUT SWING
BIPOLAR (20V Step)



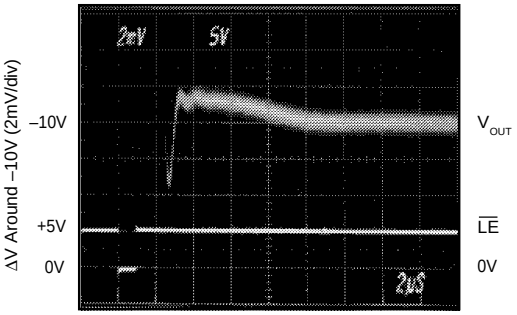
Time (2µs/div)

SETTLING TIME
BIPOLAR (–10V to +10V)



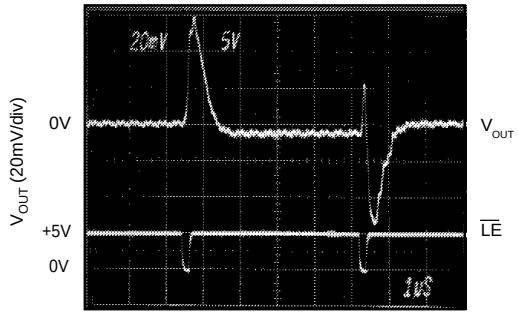
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



Time (2µs/div)

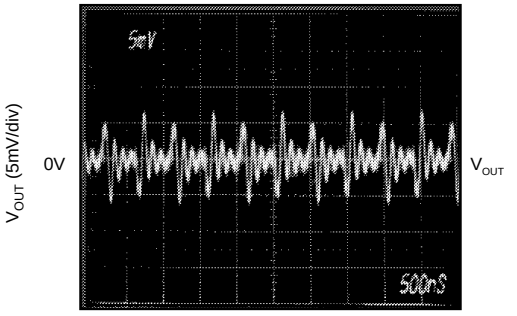
MAJOR CARRY GLITCH



Time (1µs/div)

NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

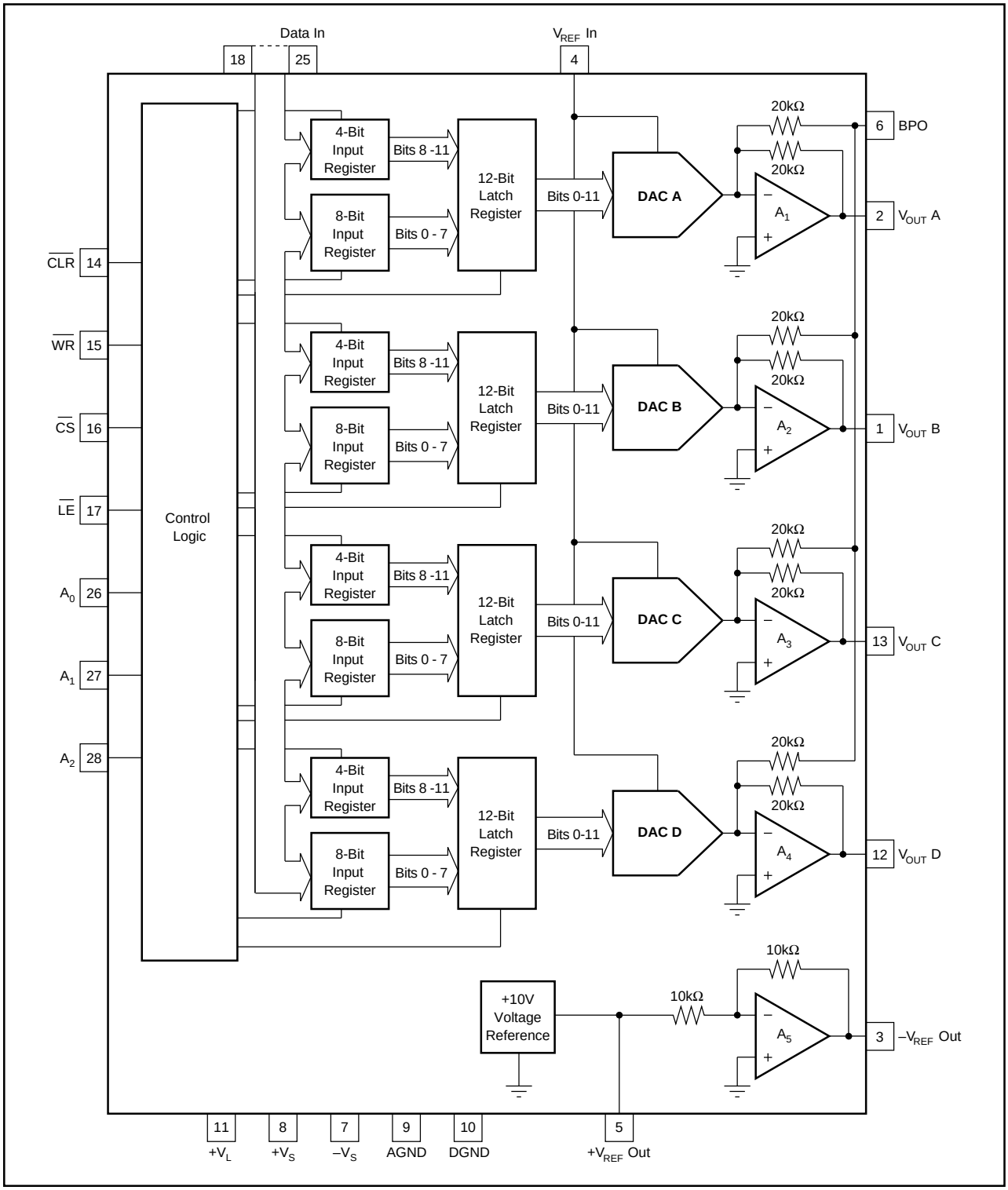
DIGITAL FEEDTHROUGH



Time (500ns/div)

DAC output noise due to activity on digital inputs with latch disabled.

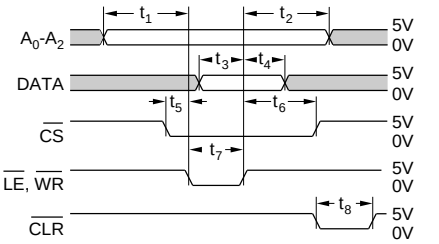
FUNCTIONAL BLOCK DIAGRAM, DAC4815 — Quad 12-bit DAC, 8-bit Port



TIMING CHARACTERISTICS

$+V_L$ = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Address Valid to Write Setup Time	20ns
t_2—Address Valid to Write Hold Time	10ns
t_3—Data Setup Time	30ns
t_4—Data Hold Time	10ns
t_5—Chip Select to $\overline{LE}$ or Write Setup Time	0ns
t_6—Chip Select to $\overline{LE}$ or Write Hold Time	0ns
t_7—Write Pulse Width	40ns
t_8—Clear Pulse Width	40ns



NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns.

(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

$\overline{CLR}$	$\overline{LE}$	$\overline{CS}$	$\overline{WR}$	A_2	A_1	A_0	FUNCTION
1	1	0	0	0	0	0	DAC A LS input register loaded with D7-D0(LSB)
1	1	0	0	0	0	1	DAC A MS input register loaded with D3(MSB)-D0
1	1	0	0	0	1	0	DAC B LS input register loaded with D7-D0(LSB)
1	1	0	0	0	1	1	DAC B MS input register loaded with D3(MSB)-D0
1	1	0	0	1	0	0	DAC C LS input register loaded with D7-D0(LSB)
1	1	0	0	1	0	1	DAC C MS input register loaded with D3(MSB)-D0
1	1	0	0	1	1	0	DAC D LS input register loaded with D7-D0(LSB)
1	1	0	0	1	1	1	DAC D MS input register loaded with D3(MSB)-D0
1	0	0	1	X	X	X	All DAC registers updated simultaneously from input registers
1	0	0	0	X	X	X	All DAC registers are transparent
1	X	1	X	X	X	X	No data transfer
1	1	X	1	X	X	X	No data transfer
0	X	X	X	X	X	X	Input registers cleared = 000_{HEX}, DAC registers = 800_{HEX}

NOTE: X = Don't care.

DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4815 are TTL and 5V CMOS compatible. Input codes for the DAC4815 are BOB (Bipolar Offset Binary). See Figure 3 for ±10V bipolar connection.

BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	BIPOLAR (BOB)
FFF_{HEX}	+Full Scale
800_{HEX}	Zero
$7FF_{HEX}$	Zero – 1 LSB
000_{HEX}	–Full Scale

INTEGRAL OR RELATIVE LINEARITY

This term, also know as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX}.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the $\overline{WR}$ signal is brought low. The data are latched in the input register when the $\overline{WR}$ goes high. Data are then transferred from the input registers to the DAC latch registers by bringing $\overline{LE}$ low. The data are latched in the DAC latch registers when $\overline{LE}$ goes high. All DACs are updated simultaneously.

When $\overline{CLR}$ is brought low, the input registers are cleared to 000_{HEX} while the DAC registers = 800_{HEX}. If $\overline{LE}$ is brought low after $\overline{CLR}$ the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or OV (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a –10V reference are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

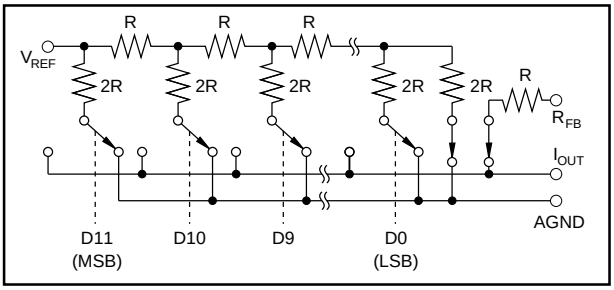


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

POWER SUPPLY CONNECTIONS

The DAC4815 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

±10V OUTPUT RANGE CONNECTION

For a ±10V bipolar output connect the DAC4815 as shown in Figure 3.

CONNECTION TO DIGITAL BUS

DAC4815s can easily be connected to a µprocessor bus. Decode your address lines to derive the control signals shown in Figure 4. Only one $\overline{LATCH}$ signal is required for a system where all DAC4815s are updated simultaneously. If your want to update DAC4815s independently, use separate $\overline{LATCH}$ signals. The $\overline{LATCH}$ and $\overline{WRITE}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

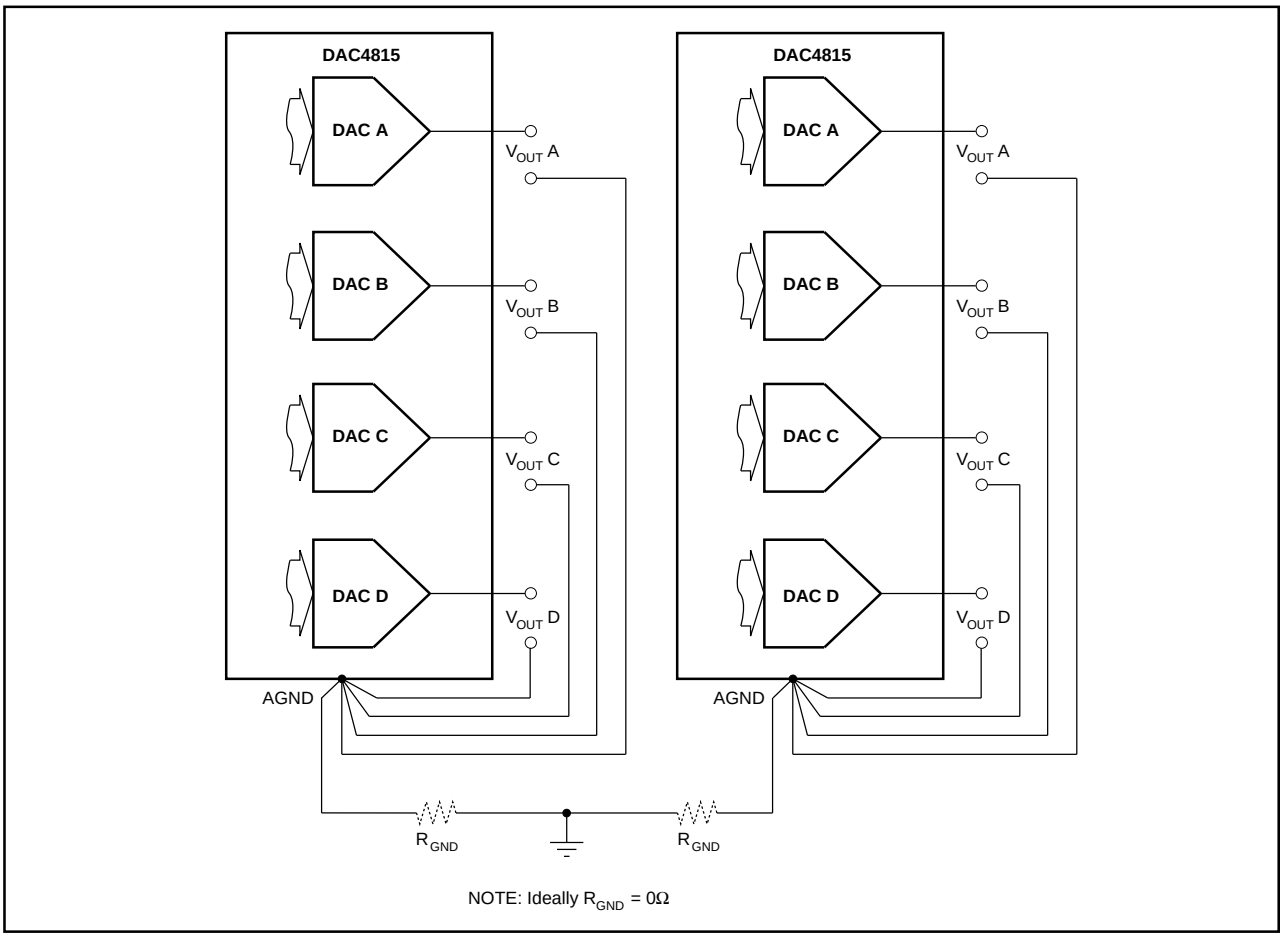


FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.

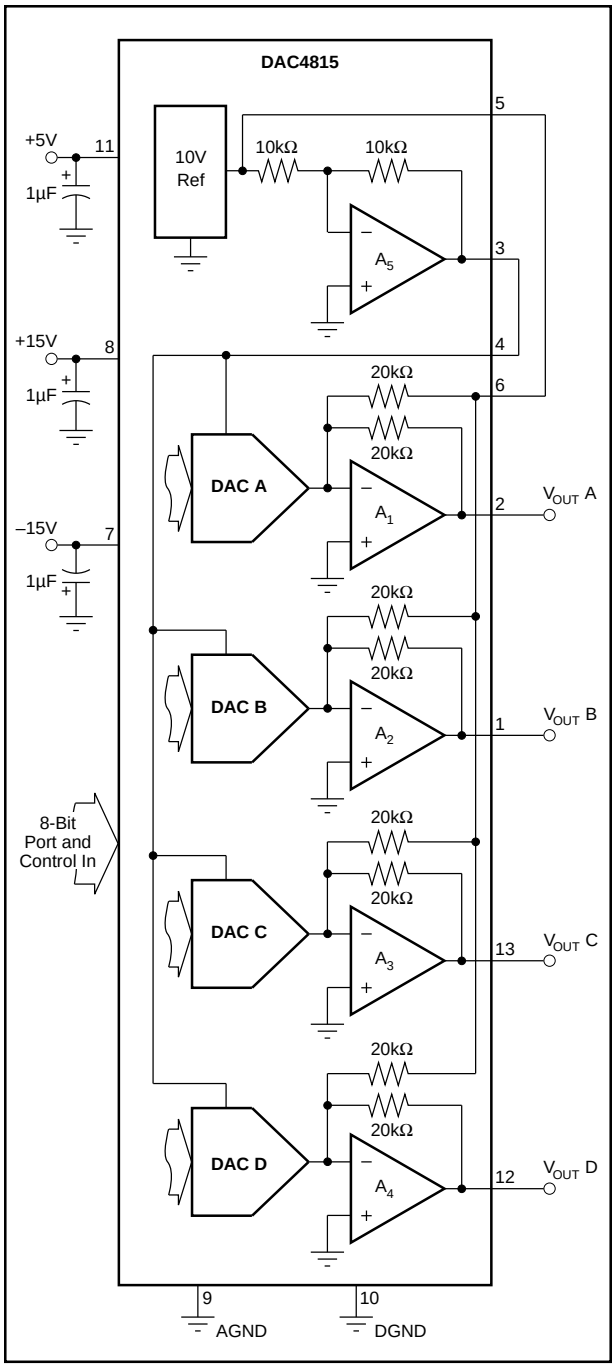


FIGURE 3. Analog Connections for ±10V DAC Output.

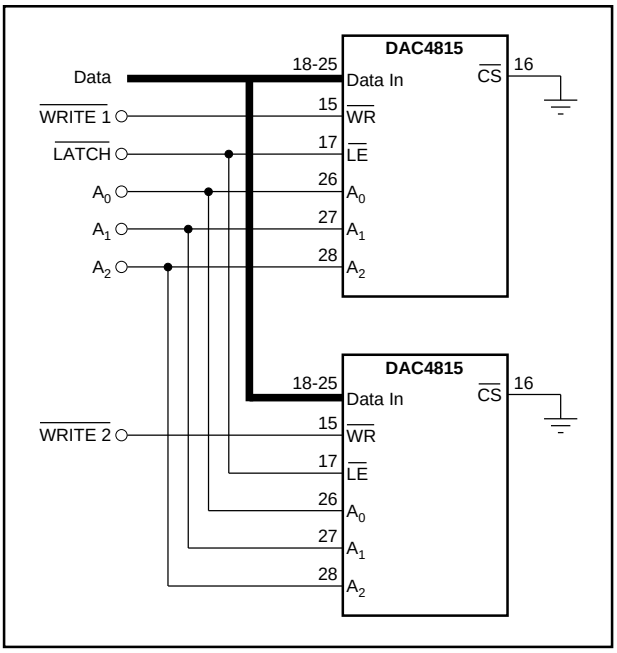


FIGURE 4. Logic Connections for Multiple DAC4815 Packages.

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