MP62055

3.3V/5V, Single-Channel 500mA Current-Limited Power Distribution Switch

The Future of Analog IC Technology

DESCRIPTION

The MP62055 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62055 analog switch features 115mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with a guaranteed current limit, making it ideal for load switching applications. The MP62055 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP62055 is available in TSOT23-5 package.

FEATURES

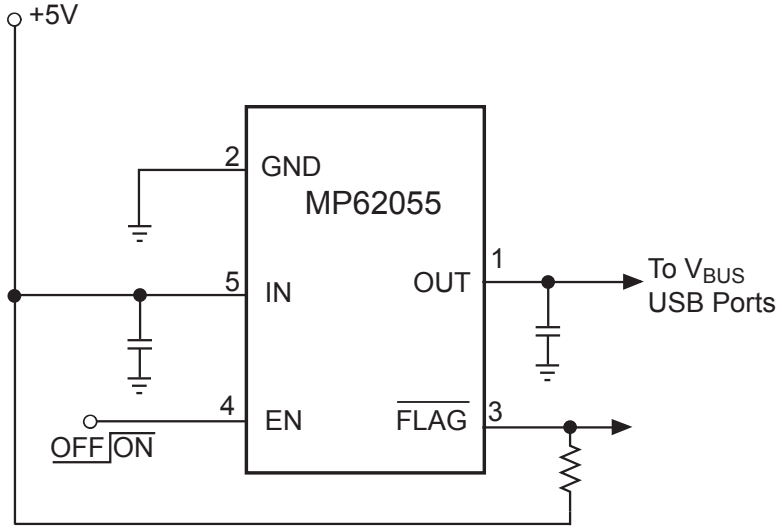
- 500mA Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 90uA Quiescent Current
- 115mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- TSOT23-5 Package
- UL File # E322138

APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Set-top-box
- USB Power Distribution

"MPS" and "The Future of Analog IC Technology" are Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



SINGLE-CHANNEL

UL Recognized Component

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

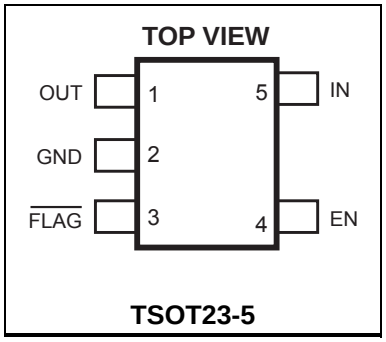
ORDINARY INFORMATION

Part Number	Enable	Switch	Maximum Continuous Load Current	Typical Short-Circuit Current @ T_A=25℃	Package	Top Marking	Free Air Temperature (T_A)
MP62055EJ	Active High	Single	500mA	1100mA	TSOT23-5	6G	–20°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP62055EJ–Z).

For RoHS Compliant Packaging, add suffix –LF (eg. MP62055EJ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN .....-0.3V to +6V
EN, FLAG, OUT to GND .....-0.3V to +6V
Continuous Power Dissipation (T_A = +25°C)(2)
…….0.56W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature.....–65°C to +150°C
Operating Junct. Temp (T_J).....–20°C to +125°C

Thermal Resistance (3)	θ_{JA}	θ_{JC}
TSOT23-5	220	110 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage
3) Measured on JESD51-7 4-layer PCB.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS (4)

V_{IN}=5V, T_A=+25°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
IN Voltage Range		2.7		5.5	V
Supply Current	Single Channel		90	120	μA
Shutdown Current	Device Disable, V_{OUT}=float, V_{IN}=5.5V		1		μA
Off Switch Leakage	Device Disable, V_{IN}=5.5V		1		μA
Current Limit		550		1100	mA
Trip Current	Current Ramp (slew rate≤100A/s) on Output		1	1.4	A
Under-voltage Lockout	Rising Edge	1.95		2.65	V
Under-voltage Hysteresis			250		mV
FET On Resistance	I_{OUT}=100mA, and -20°C<T_A<85°C		115	155	mΩ
EN Input Logic High Voltage		2			V
EN Input Logic Low Voltage				0.8	V
FLAG Output Logic Low Voltage	I_{SINK}=5mA			0.4	V
FLAG Output High Leakage Current	V_{IN}=V_{FLAG}=5.5V			1	μA
Thermal Shutdown			140		°C
Thermal Shutdown Hysteresis			20		°C
V_{OUT} Rising Time, Tr (5)	VIN=5.5V, CL=1uF, RL=11Ω		0.9		ms
	VIN=2.7V, CL=1uF, RL=11Ω		1.7		ms
V_{OUT} Falling Time, Tf (5)	VIN=5.5V, CL=1uF, RL=11Ω			0.5	ms
	VIN=2.7V, CL=1uF, RL=11Ω			0.5	ms
Turn On Time, Ton (6)	CL=100μF, RL=11Ω			3	ms
Turn Off Time, Toff (6)	CL=100μF, RL=11Ω			10	ms
FLAG Deglitch Time		4	8	15	ms
EN Input Leakage			1		μA
Reverse Leakage Current	OUT=5.5V, IN=GND		0.2		μA

NOTE:

4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
5) Measured from 10% to 90%.
6) Measured from (50%) EN signal to (90%) output signal.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	OUT	Power-Distribution Switch Output.
2	GND	Ground
3	$\overline{\text{FLAG}}$	IN-to-OUT Over-current, active-low output flag. Open-Drain.
4	EN	Enable Input. Active High.
5	IN	Input Voltage. Accepts 2.7V to 5.5V input.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25ºC, unless otherwise noted.

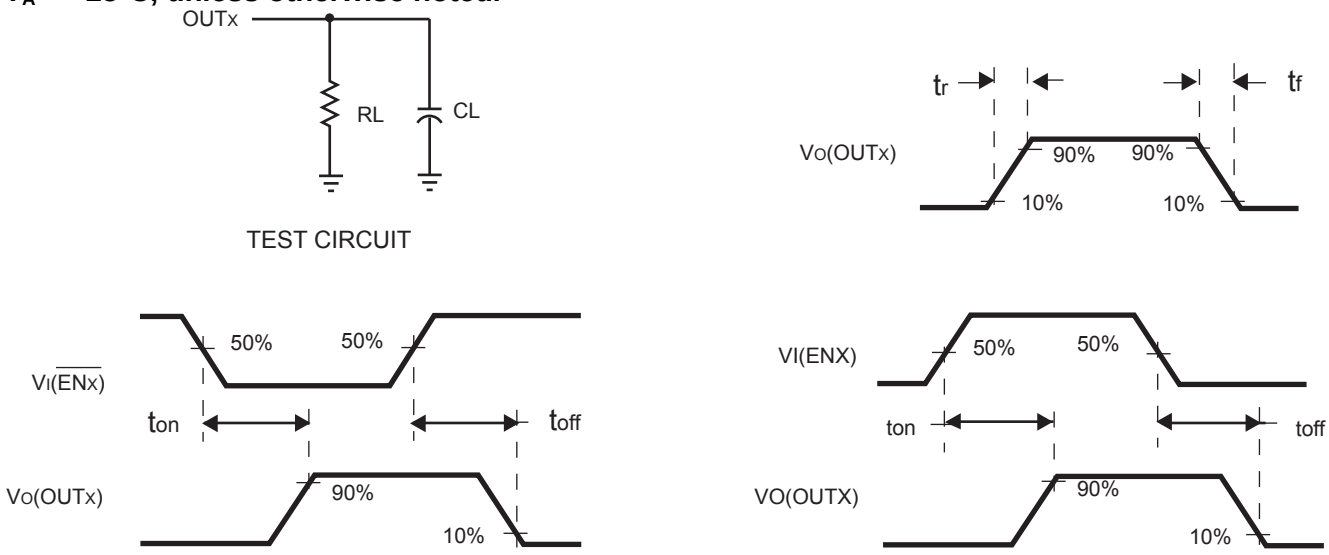


Figure 1—Test Circuit and Voltage Waveforms

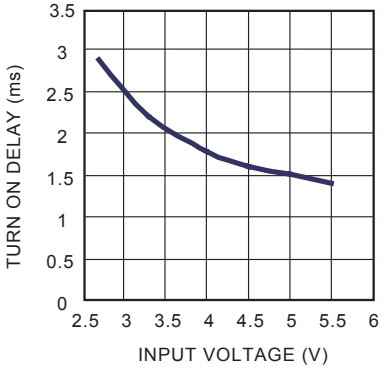
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=5.5V, C_L = 2.2µF, T_A = +25ºC, unless otherwise noted.

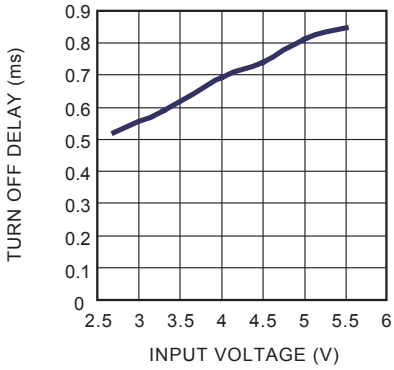
Turn on Delay vs. Input Votage

V_{EN}=5V, R_L=11Ω



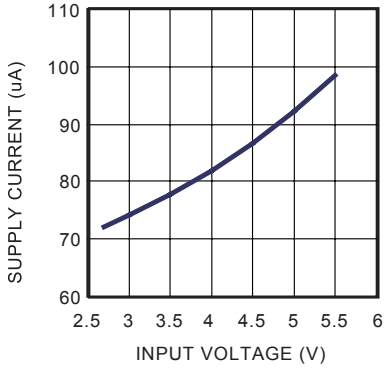
Turn off Delay vs. Input Votage

V_{EN}=5V, R_L=11Ω



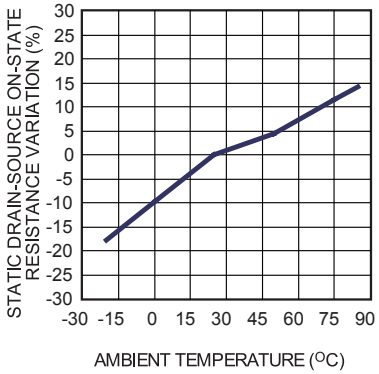
Supply Current, Output Enabled vs. Input Voltage

V_{EN}=5V



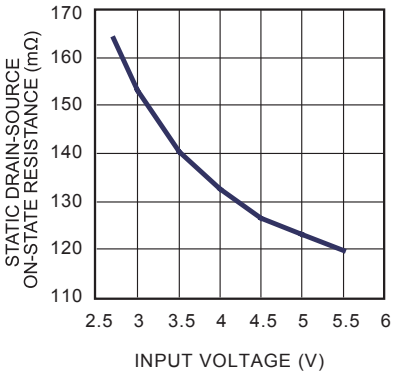
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

V_{IN}=5V, I_O=0.1A



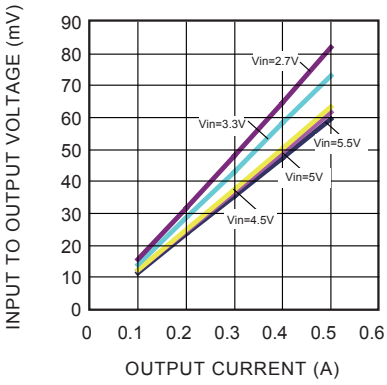
Static Drain-Source On-State Resistance vs. Input Voltage

V_{EN}=5V, I_{OUT}=0.5A



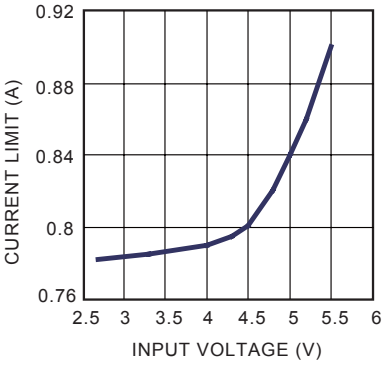
Input to Output Voltage vs. Load Current

V_{EN}=5V

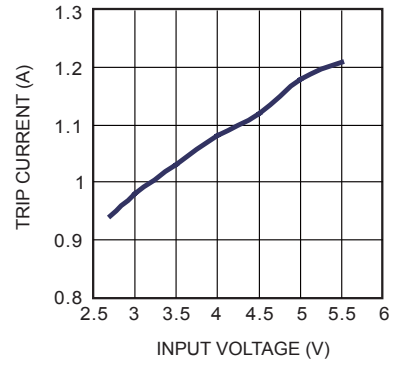


Current Limit vs. Input Voltage

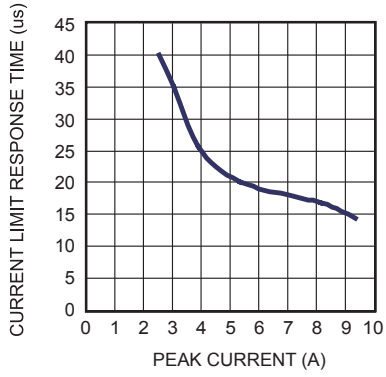
V_{EN}=5V



Threshold Trip Current vs. Input Voltage



Current Limit Response Time vs. Peak Current



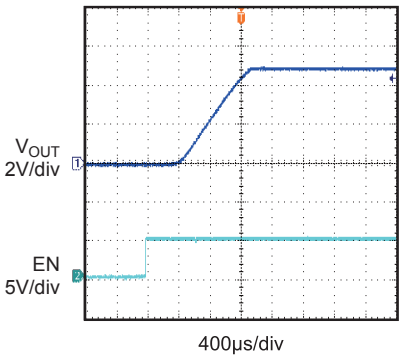
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5.5V, C_L = 2.2µF, T_A = +25ºC, unless otherwise noted.

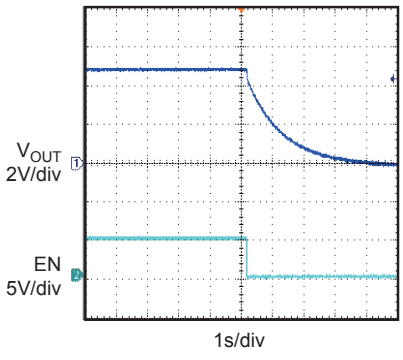
Turn On Delay and Rise Time with 0.1uF Load

V_{EN}=5V, C_L=0.1uF



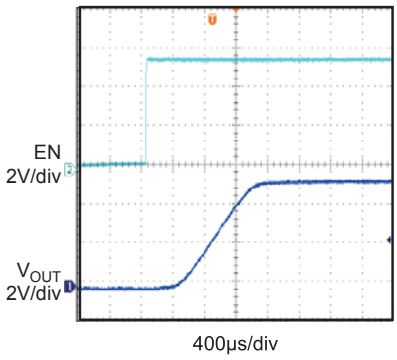
Turn Off Delay and Fall Time with 0.1uF Load

V_{EN}=5V, C_L=0.1uF



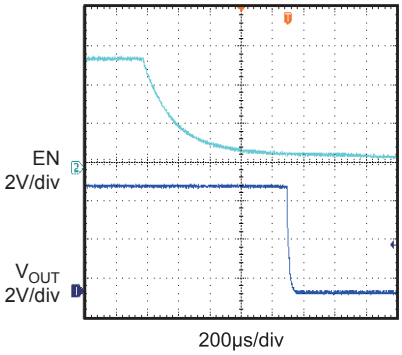
Turn On Delay and Rise Time

R_L=11Ω, C_L=1uF

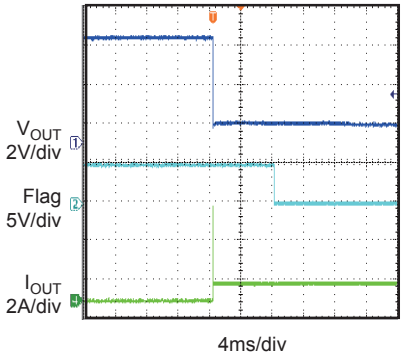


Turn Off Delay and Fall Time

R_L=11Ω, C_L=1uF

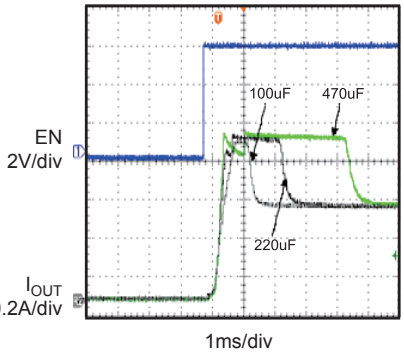


1Ω Load Connected to Enabled Device

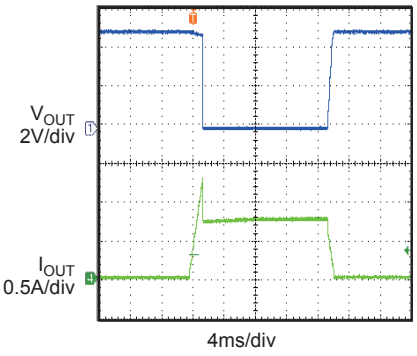


Inrush Current with Different Load Capacitance

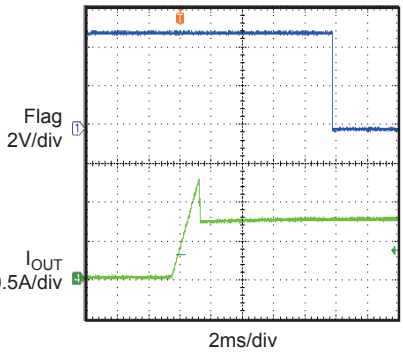
R_L=11Ω, Start up by EN



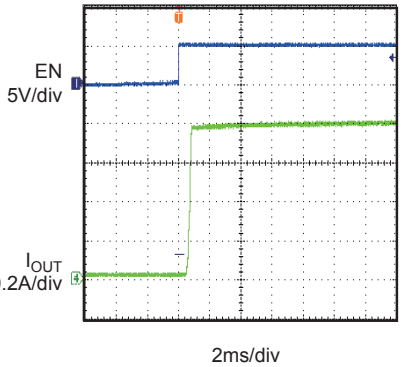
Threshold Trip Current with Ramped Load on Enabled Device



Ramped Load on Enabled Device



Short Circuit Current, Device Enabled into Short



MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

FUNCTION BLOCK DIAGRAM

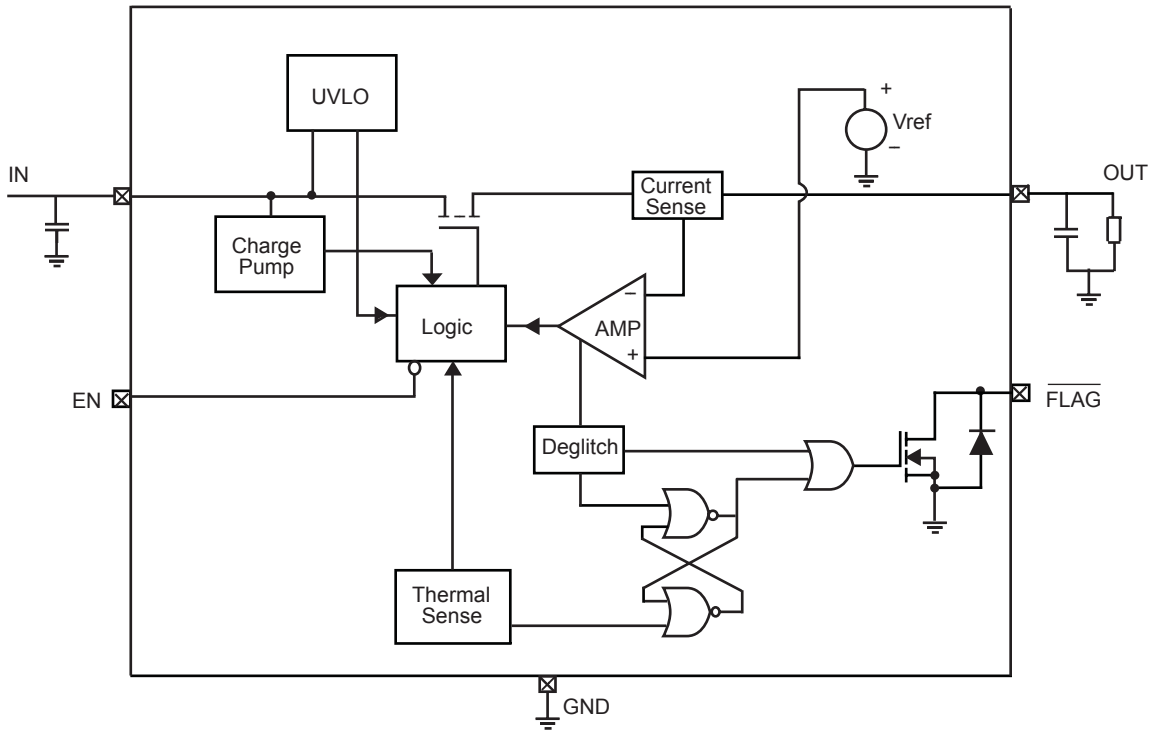


Figure 2—Functional Block Diagram

DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62055 switches into to a constant-current mode (current limit value). MP62055 will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

Trigger overcurrent protection for different overload conditions occurring in applications:

1) The output has been shorted or overloaded before the device is enabled or input applied. MP62055 detects the short or overload and immediately switches into a constant-current mode.
2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.
3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. The MP62055 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during an over temp. or a voltage lockout.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62055 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

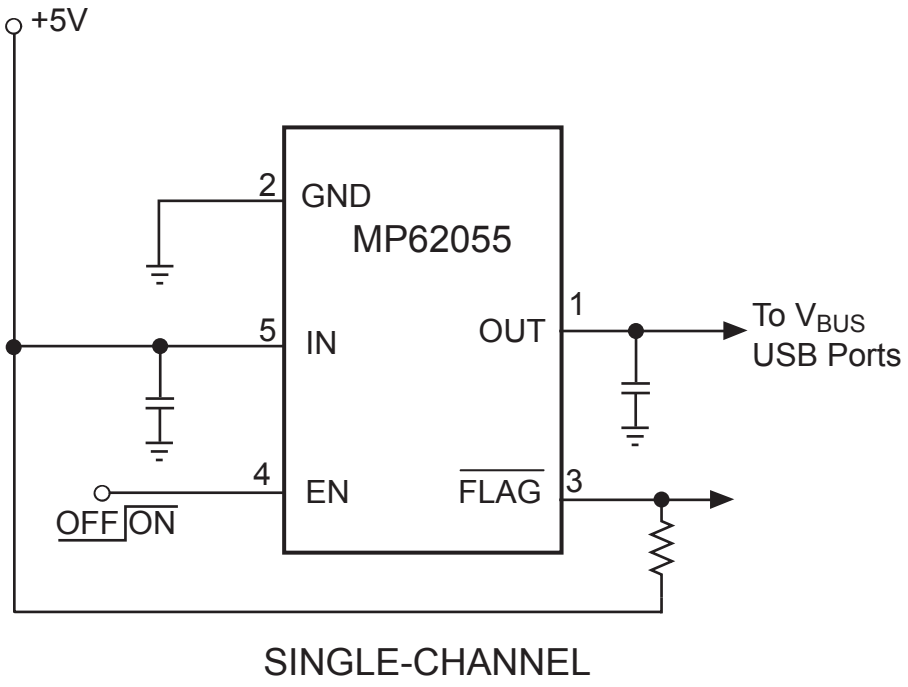
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

APPLICATION INFORMATION

Power-Supply Considerations

Over 10µF capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.



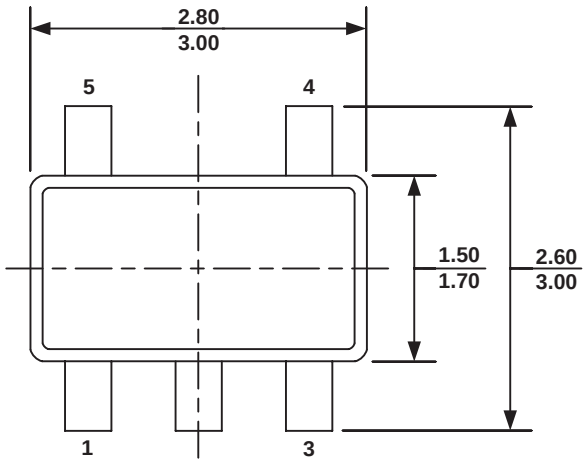
SINGLE-CHANNEL

Figure 3—Application Circuit

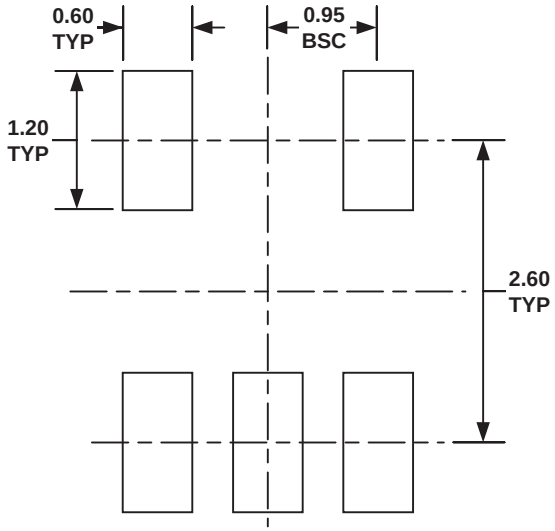
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

PACKAGE INFORMATION

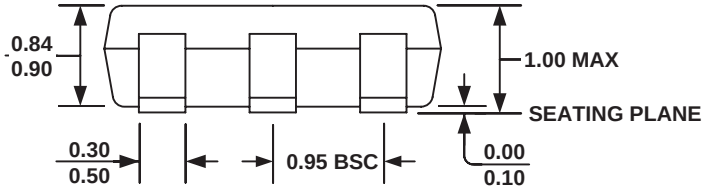
TSOT23-5



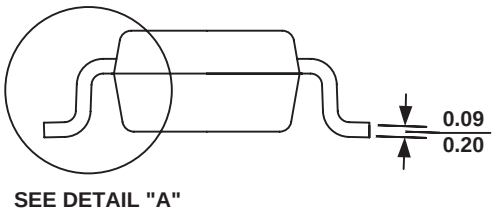
TOP VIEW



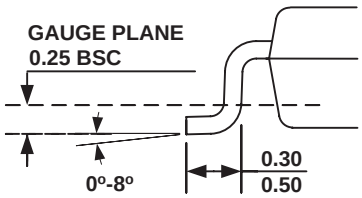
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL A

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.