

|                            |                          |                   |             |
|----------------------------|--------------------------|-------------------|-------------|
| 4K                         | Commercial<br>Industrial | X2804A<br>X2804AI | 512 x 8 Bit |
| Electrically Erasable PROM |                          |                   |             |

## FEATURES

- Simple Byte Write Operation
  - Internally Latched Address and Data
  - Self Timed Write
  - Noise Protected  $\overline{WE}$  Pin
- Reliable N-Channel Floating Gate MOS Technology
- Single 5V Supply
- High Reliability
  - Endurance: 10,000 Writes Per Byte
  - Data Retention: 100 Years
- Byte Write Time: 10 ms Max.
- Fast Access Time: 250 ns Max.
- Low Power Dissipation
  - Active Current: 80 mA Max.
  - Standby Current: 50 mA Max.

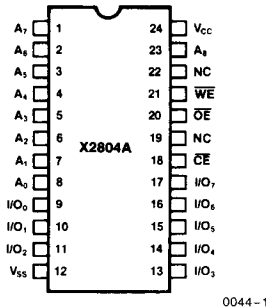
## DESCRIPTION

The Xicor X2804A is a 512 x 8 E<sup>2</sup>PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2804A is compatible with the JEDEC approved pinout for byte-wide memories.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 10,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

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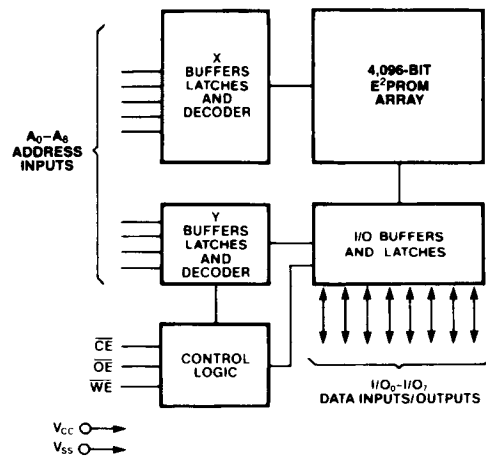
## PIN CONFIGURATION



## PIN NAMES

|                                    |                   |
|------------------------------------|-------------------|
| A <sub>0</sub> –A <sub>8</sub>     | Address Inputs    |
| I/O <sub>0</sub> –I/O <sub>7</sub> | Data Input/Output |
| WE                                 | Write Enable      |
| $\overline{CE}$                    | Chip Enable       |
| $\overline{OE}$                    | Output Enable     |
| V <sub>CC</sub>                    | +5V               |
| V <sub>SS</sub>                    | Ground            |
| NC                                 | No Connect        |

## FUNCTIONAL DIAGRAM



# X2804A, X2804AI

## ABSOLUTE MAXIMUM RATINGS\*

|                                              |                 |
|----------------------------------------------|-----------------|
| Temperature Under Bias                       |                 |
| X2804A                                       | −10°C to +85°C  |
| X2804AI                                      | −65°C to +135°C |
| Storage Temperature                          | −65°C to +150°C |
| Voltage on any Pin with<br>Respect to Ground | −1.0V to +7V    |
| D.C. Output Current                          | 5 mA            |
| Lead Temperature<br>(Soldering, 10 Seconds)  | 300°C           |

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. OPERATING CHARACTERISTICS

X2804A  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ , unless otherwise specified.

X2804AI  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

| Symbol      | Parameter                  | X2804A Limits |                | X2804AI Limits |                | Units         | Test Conditions                                                                                    |
|-------------|----------------------------|---------------|----------------|----------------|----------------|---------------|----------------------------------------------------------------------------------------------------|
|             |                            | Min.          | Max.           | Min.           | Max.           |               |                                                                                                    |
| $I_{CC}$    | $V_{CC}$ Current (Active)  |               | 80             |                | 100            | mA            | $\overline{CE} = \overline{OE} = V_{IL}$<br>All I/O's = Open<br>Other Inputs = $V_{CC}$            |
| $I_{SB}$    | $V_{CC}$ Current (Standby) |               | 50             |                | 60             | mA            | $\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$<br>All I/O's = Open<br>Other Inputs = $V_{CC}$ |
| $I_{LI}$    | Input Leakage Current      |               | 10             |                | 10             | $\mu\text{A}$ | $V_{IN} = \text{GND to } V_{CC}$                                                                   |
| $I_{LO}$    | Output Leakage Current     |               | 10             |                | 10             | $\mu\text{A}$ | $V_{OUT} = \text{GND to } V_{CC}$                                                                  |
| $V_{IL(2)}$ | Input Low Voltage          | −1.0          | 0.8            | −1.0           | 0.8            | V             |                                                                                                    |
| $V_{IH(2)}$ | Input High Voltage         | 2.0           | $V_{CC} + 0.5$ | 2.2            | $V_{CC} + 1.0$ | V             |                                                                                                    |
| $V_{OL}$    | Output Low Voltage         |               | 0.4            |                | 0.4            | V             | $I_{OL} = 2.1 \text{ mA}$                                                                          |
| $V_{OH}$    | Output High Voltage        | 2.4           |                | 2.4            |                | V             | $I_{OH} = -400 \mu\text{A}$                                                                        |

**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $f = 1.0 \text{ MHz}$ ,  $V_{CC} = 5\text{V}$

| Symbol       | Test                     | Max. | Units | Conditions            |
|--------------|--------------------------|------|-------|-----------------------|
| $C_{I/O(1)}$ | Input/Output Capacitance | 10   | pF    | $V_{I/O} = 0\text{V}$ |
| $C_{IN(1)}$  | Input Capacitance        | 6    | pF    | $V_{IN} = 0\text{V}$  |

## A.C. CONDITIONS OF TEST

|                                   |                                          |
|-----------------------------------|------------------------------------------|
| Input Pulse Levels                | 0V to 3.0V                               |
| Input Rise and<br>Fall Times      | 10 ns                                    |
| Input and Output<br>Timing Levels | 1.5V                                     |
| Output Load                       | 1 TTL Gate and<br>$C_L = 100 \text{ pF}$ |

## MODE SELECTION

| CE | OE | WE | Mode                         | I/O       | Power   |
|----|----|----|------------------------------|-----------|---------|
| L  | L  | H  | Read                         | $D_{OUT}$ | Active  |
| L  | H  | L  | Write                        | $D_{IN}$  | Active  |
| H  | X  | X  | Standby and<br>Write Inhibit | High Z    | Standby |
| X  | L  | X  | Write Inhibit                | —         | —       |
| X  | X  | H  | Write Inhibit                | —         | —       |

**Notes:** (1) This parameter is periodically sampled and not 100% tested.

(2)  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.

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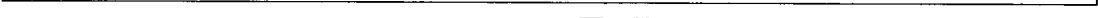
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Y2801A T<sub>a</sub> = 0°C to +30°C V<sub>cc</sub> = +5V ± 5% unless otherwise specified

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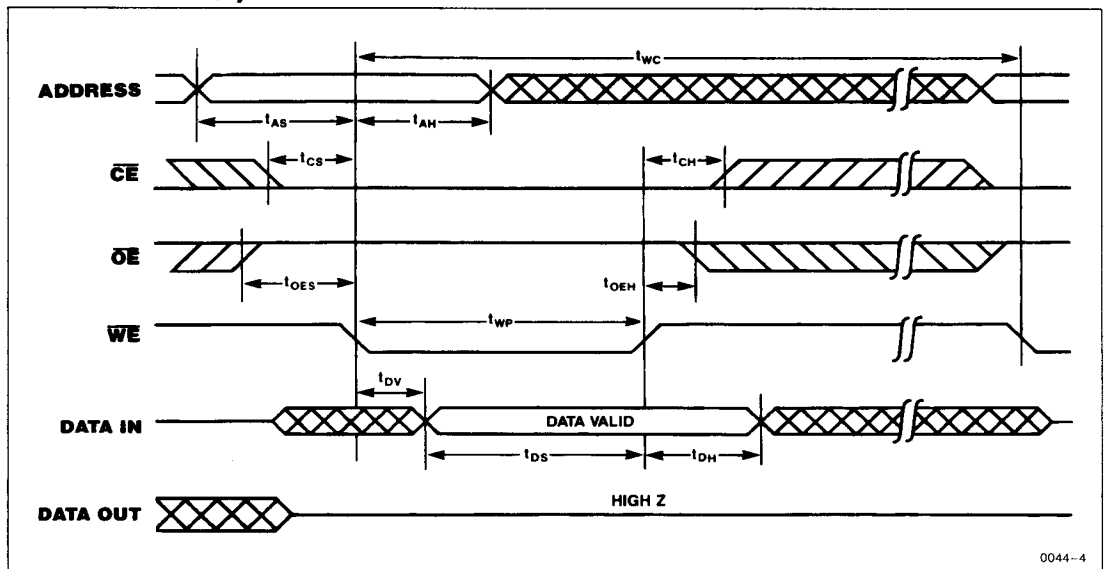


## X2804A, X2804AI

### Write Cycle Limits

| Symbol         | Parameter                         | X2804A-25<br>X2804AI-25 |      | X2804A<br>X2804AI |      | X2804A-35<br>X2804AI-35 |      | X2804A-45<br>X2804AI-45 |      | Units   |
|----------------|-----------------------------------|-------------------------|------|-------------------|------|-------------------------|------|-------------------------|------|---------|
|                |                                   | Min.                    | Max. | Min.              | Max. | Min.                    | Max. | Min.                    | Max. |         |
| $t_{WC}^{(7)}$ | Write Cycle Time                  |                         | 10   |                   | 10   |                         | 10   |                         | 10   | ms      |
| $t_{AS}$       | Address Setup Time                | 10                      |      | 10                |      | 10                      |      | 10                      |      | ns      |
| $t_{AH}$       | Address Hold Time                 | 120                     |      | 120               |      | 150                     |      | 150                     |      | ns      |
| $t_{CS}$       | Write Setup Time                  | 0                       |      | 0                 |      | 0                       |      | 0                       |      | ns      |
| $t_{CH}$       | Write Hold Time                   | 0                       |      | 0                 |      | 0                       |      | 0                       |      | ns      |
| $t_{CW}$       | Chip Enable to End of Write Input | 150                     |      | 150               |      | 175                     |      | 230                     |      | ns      |
| $t_{OES}$      | Output Enable Setup Time          | 10                      |      | 10                |      | 10                      |      | 10                      |      | ns      |
| $t_{OEH}$      | Output Enable Hold Time           | 10                      |      | 10                |      | 10                      |      | 10                      |      | ns      |
| $t_{WP}$       | Write Pulse Width                 | 150                     |      | 150               |      | 175                     |      | 230                     |      | ns      |
| $t_{WPH}$      | Write Control Recovery            | 50                      |      | 50                |      | 50                      |      | 50                      |      | ns      |
| $t_{DV}$       | Data Valid Time                   |                         | 1    |                   | 1    |                         | 1    |                         | 1    | $\mu$ s |
| $t_{DS}$       | Data Setup Time                   | 120                     |      | 135               |      | 175                     |      | 230                     |      | ns      |
| $t_{DH}$       | Data Hold Time                    | 15                      |      | 15                |      | 20                      |      | 30                      |      | ns      |

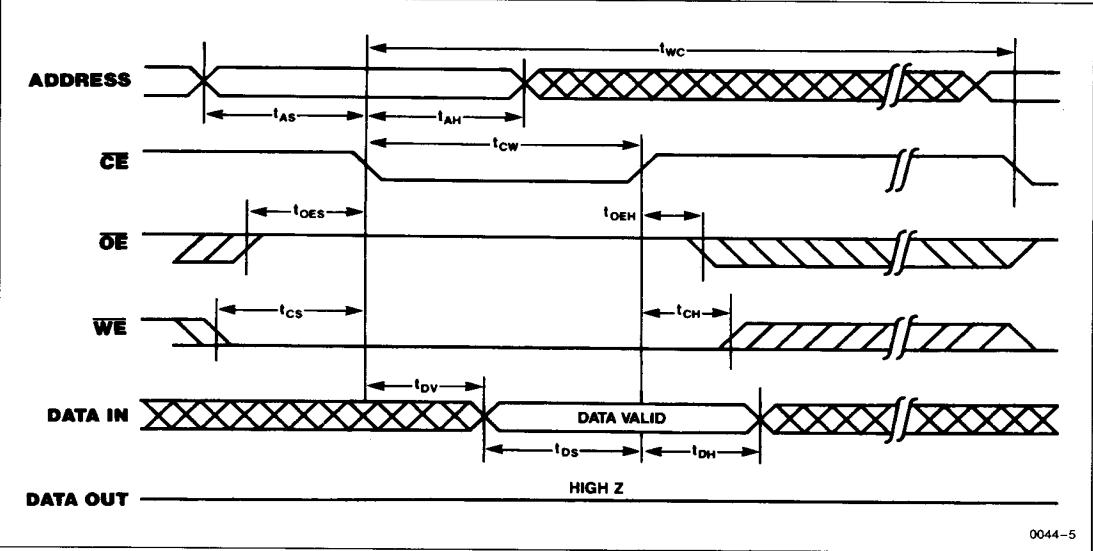
### WE Controlled Write Cycle



**Note:** (7)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

X2804A, X2804AI

$\overline{\text{CE}}$  Controlled Write Cycle



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## X2804A, X2804AI

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### PIN DESCRIPTIONS

#### Addresses ( $A_0$ – $A_8$ )

The Address inputs select an 8-bit memory location during a read or write operation.

#### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

#### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

#### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X2804A through the I/O pins.

#### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to the X2804A.

### DEVICE OPERATION

#### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

#### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X2804A supports both

a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first.

A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms. In order to take advantage of the typical write time as opposed to the maximum specified time, the user can poll the X2804A. The I/O pins are placed in the high impedance state during the internal programming cycle. Once the internal cycle is complete, the X2804A may be accessed without any limitations. Therefore, the host can poll an address with known data (preferably with zeroes), as soon as a compare is true, the X2804A is ready for another write cycle.

### WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse typically less than 20 ns will not initiate a write cycle.
- $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3V$ , typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH or  $\overline{CE}$  HIGH during power-on and power-off, will inhibit inadvertent writes.

# X2804A, X2804AI

## SYSTEM CONSIDERATIONS

Because the X2804A is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

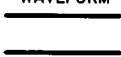
Because the X2804A has two power modes, standby and active, proper decoupling of the memory array is

of prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu$ F high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu$ F electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

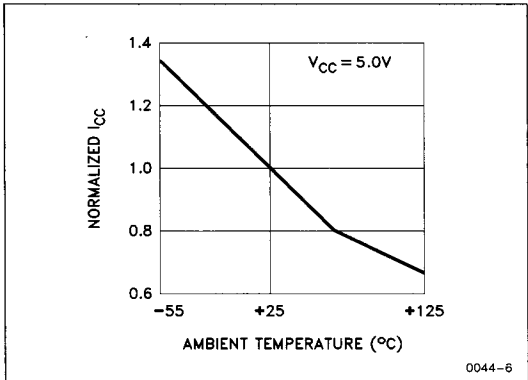
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SYMBOL TABLE

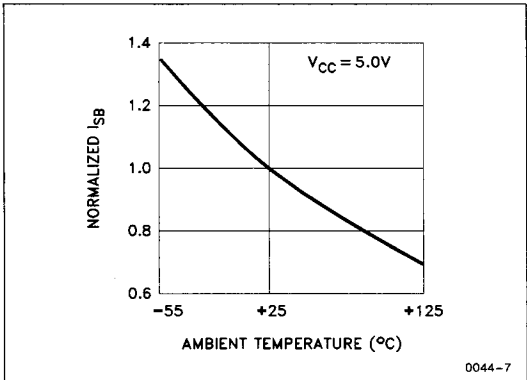
| WAVEFORM                                                                            | INPUTS                       | OUTPUTS                       |
|-------------------------------------------------------------------------------------|------------------------------|-------------------------------|
|    | Must be steady               | Will be steady                |
|    | May change from Low to High  | Will change from Low to High  |
|    | May change from High to Low  | Will change from High to Low  |
|   | Don't Care : Changes Allowed | Changing : State Not Known    |
|  | N/A                          | Center Line is High Impedance |

# X2804A, X2804AI

Normalized Active Supply Current  
vs. Ambient Temperature



Normalized Standby Supply Current  
vs. Ambient Temperature



Normalized Access Time  
vs. Ambient Temperature

