

512Kx8 Monolithic SRAM, SMD 5962-95600

FEATURES

- Access Times of 15, 17, 20, 25, 35, 45, 55ns
- Data Retention Function (LPA version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 32 lead JEDEC Approved Evolutionary Pinout
 - Ceramic Sidebrazed 600 mil DIP (Package 9)
 - Ceramic Sidebrazed 400 mil DIP (Package 326)
 - Ceramic 32 pin Flatpack (Package 344)
 - Ceramic Thin Flatpack (Package 321)
 - Ceramic SOJ (Package 140)
- 36 lead JEDEC Approved Revolutionary Pinout
 - Ceramic Flatpack (Package 316)
 - Ceramic SOJ (Package 327)
 - Ceramic LCC (Package 502)
- Single +5V ($\pm 10\%$) Supply Operation

The EDI88512CA is a 4 megabit Monolithic CMOS Static RAM.

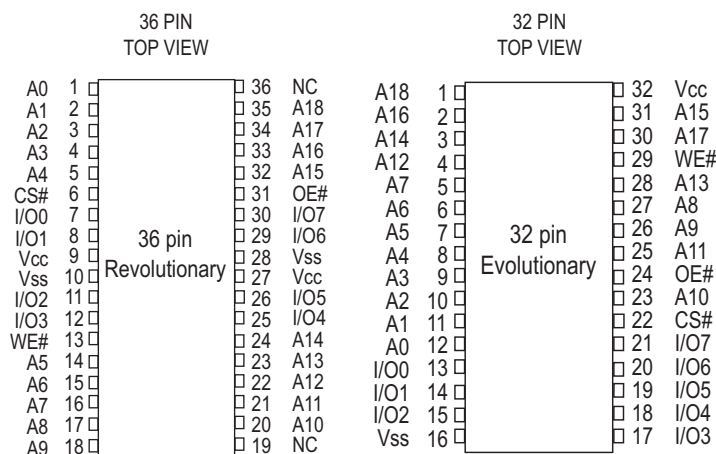
The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the four megabit device. All 32 pin packages are pin for pin upgrades for the single chip enable 128K x 8, the EDI88128CS. Pins 1 and 30 become the higher order addresses.

The 36 pin revolutionary pinout also adheres to the JEDEC standard for the four megabit device. The center pin power and ground pins help to reduce noise in high performance systems. The 36 pin pinout also allows the user an upgrade path to the future 2Mx8.

A Low Power version with Data Retention (EDI88512LPA) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

*This product is subject to change without notice.

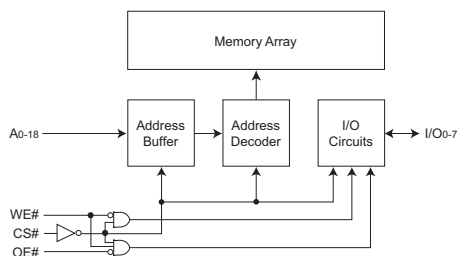
FIG. 1 PIN CONFIGURATION

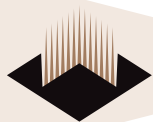


PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-18	Address Inputs
WE#	Write Enables
CS#	Chip Selects
OE#	Output Enable
Vcc	Power (+5V $\pm 10\%$)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Voltage on any pin relative to Vss	$-0.5 \leq T_A \leq 7.0$	V
Operating Temperature T_A (Ambient)		
Commercial	$0 \leq T_A \leq +70$	°C
Industrial	$-40 \leq T_A \leq +85$	°C
Military	$-55 \leq T_A \leq +125$	°C
Storage Temperature, Plastic	$-65 \leq T_A \leq +150$	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, T_J	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

OE#	CS#	WE#	Mode	Output	Power
X	H	X	Standby	High Z	I_{CC2}, I_{CC3}
H	L	H	Output Deselect	High Z	I_{CC1}
L	L	H	Read	Data Out	I_{CC1}
X	L	L	Write	Data In	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	3.0	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE

 $(T_A = +25^\circ\text{C})$

Parameter	Symbol	Condition	Max	Unit
Address Lines	C_i	$V_{IN} = V_{CC}$ or V_{SS} , $f = 1.0\text{MHz}$	12	pF
Data Lines	C_o	$V_{OUT} = V_{CC}$ or V_{SS} , $f = 1.0\text{MHz}$	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

 $(V_{CC} = 5V, T_A = -55^\circ\text{C}$ to $+125^\circ\text{C})$

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	$V_{IN} = 0V$ to V_{CC}	-10	10	A
Output Leakage Current	I_{LO}	$V_{I/O} = 0V$ to V_{CC}	-10	10	A
Operating Power Supply Current	I_{CC1}	$WE\#, CS\# = V_{IL}, I/O = 0mA$, Min Cycle (17ns) (20 -55ns)	—	250 225	mA
Standby (TTL) Power Supply Current	I_{CC2}	$CS\# \geq V_{IH}, V_{IN} \leq V_{IL}, V_{IN} \geq V_{IH}$	—	60	mA
Full Standby Power Supply Current	I_{CC3}	$CS\# \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	CA LPA	25 20	mA
Output Low Voltage	V_{OL}	$I_{OL} = 6.0mA$	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	V

NOTE: DC test conditions: $V_{IL} = 0.3V$, $V_{IH} = V_{CC} - 0.3V$

AC TEST CONDITIONS

Figure 1

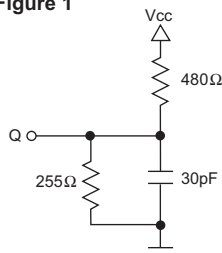
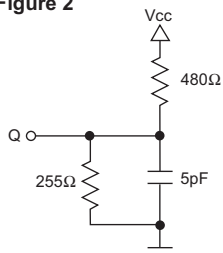
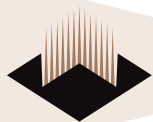


Figure 2



Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ} , t_{GHQZ} and t_{WLOZ} , $C_L = 5pF$ Figure 2)



AC CHARACTERISTICS – READ CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C)

Parameter	Symbol		15ns		17ns		20ns		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t _{AVQV}	t _{AA}		15		17		20		25		35		45		55	ns
Chip Enable Access Time	t _{ELQV}	t _{ACS}		15		17		20		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	2		3		3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}	0	7	0	7	0	8	0	10	0	15	0	20	0	20	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	0		0		0		0		0		0		0		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		8		8		10		12		15		25		30	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		0		0		0		0		ns
Output Disable to Output in High Z(1)	t _{GHQZ}	t _{OHZ}	0	7	0	7	0	8	0	10	0	15	0	20	0	20	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C)

Parameter	Symbol		15ns		17ns		20ns		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	15		17		20		25		35		45		55		ns
Chip Enable to End of Write	t _{ELWH}	t _{CW}	13		14		15		17		25		30		50		ns
	t _{ELEH}	t _{CW}	13		14		15		17		25		30		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		0		0		0		0		ns
	t _{AVEL}	t _{AS}	0		0		0		0		0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	13		14		15		17		25		30		50		ns
	t _{AVEH}	t _{AW}	13		14		15		17		25		30		50		ns
Write Pulse Width	t _{WLWH}	t _{WP}	13		14		15		17		25		30		45		ns
	t _{WLEH}	t _{WP}	13		14		15		17		25		30		45		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		0		0		0		0		0		ns
	t _{EHAX}	t _{WR}	0		0		0		0		0		0		0		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		0		0		0		ns
	t _{EHDX}	t _{DH}	0		0		0		0		0		0		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	8	0	8	0	8	0	10	0	25	0	30	0	30	ns
Data to Write Time	t _{DVWH}	t _{DW}	8		8		10		12		20		25		40		ns
	t _{DVEH}	t _{DW}	8		8		10		12		20		25		30		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.



FIG. 2 TIMING WAVEFORM - READ CYCLE

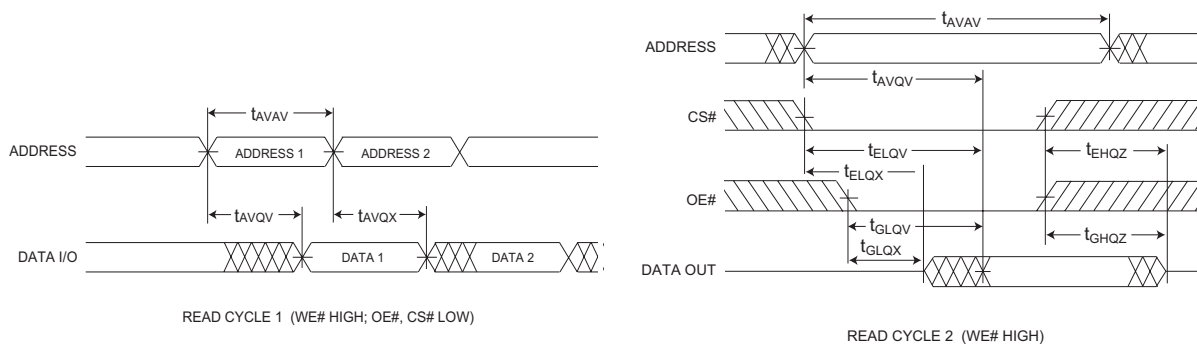


FIG. 3 WRITE CYCLE - WE# CONTROLLED

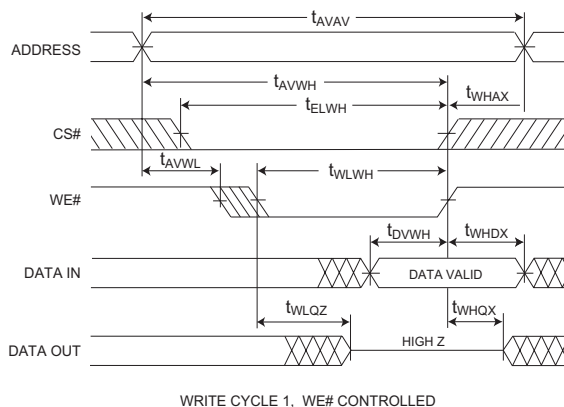
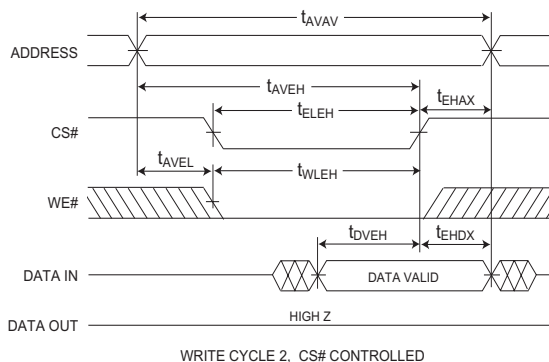
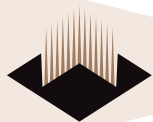
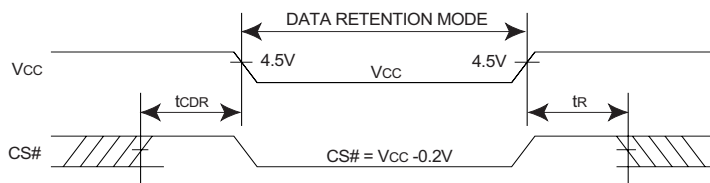


FIG. 4 WRITE CYCLE - CS# CONTROLLED

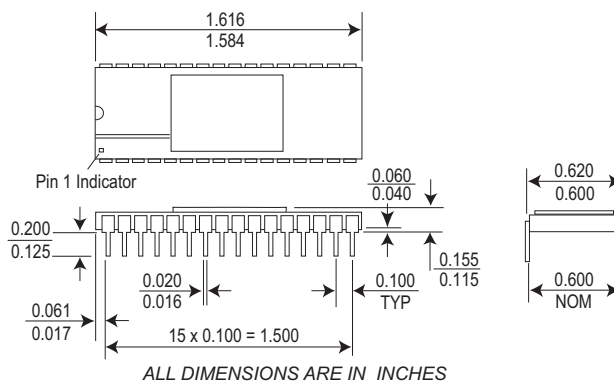
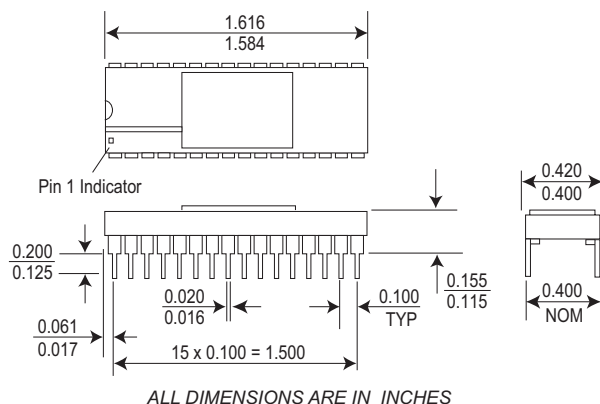
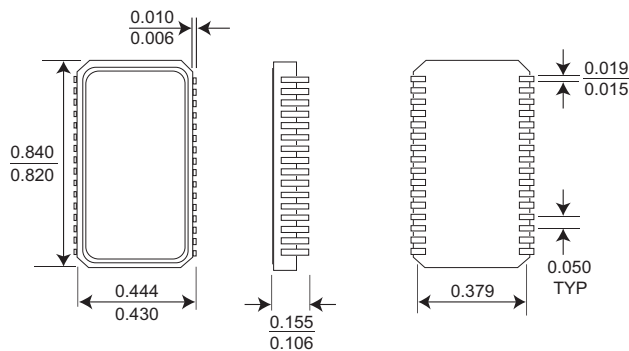


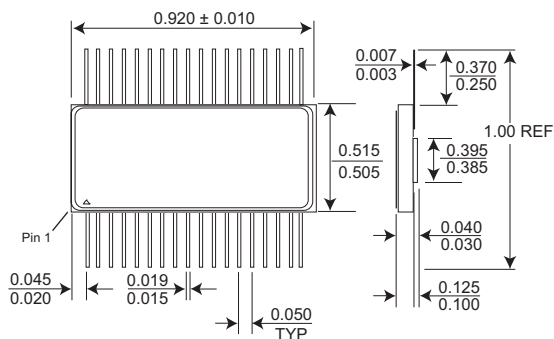
**DATA RETENTION CHARACTERISTICS (EDI88512LPA ONLY)** $(-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C})$

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{CC}	$V_{CC} = 2.0\text{V}$	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	$CS\# \geq V_{CC} - 0.2\text{V}$	–	–	2	mA
Chip Disable to Data Retention Time	t_{CDR}	$V_{IN} \geq V_{CC} - 0.2\text{V}$	0	–	–	ns
Operation Recovery Time	T_R	or $V_{IN} \leq 0.2\text{V}$	t_{AVAV}	–	–	ns

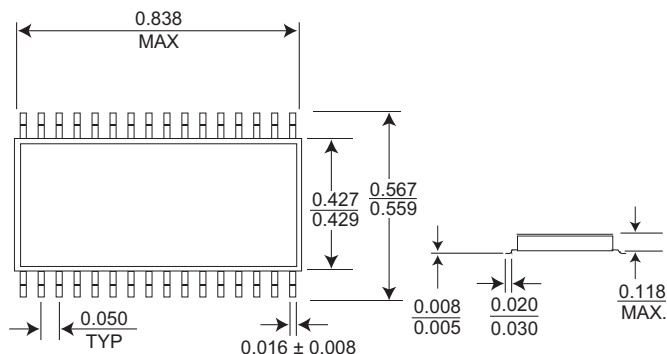
FIG. 5 DATA RETENTION - CS# CONTROLLED

DATA RETENTION, CS# CONTROLLED

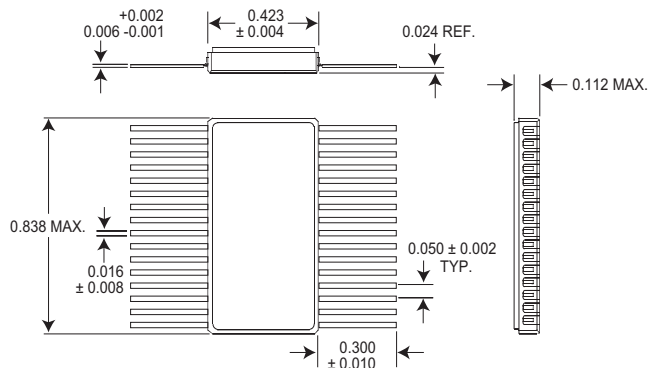
**PACKAGE 9: 32 LEAD SIDEBRAZED CERAMIC DIP, SMD 5962-95600XXMXA****PACKAGE 326: 32 LEAD SIDEBRAZED CERAMIC DIP****PACKAGE 140: 32 LEAD CERAMIC SOJ, SMD 5962-95600XXMUA**

**PACKAGE 316: 36 PIN CERAMIC FLATPACK, SMD 5962-95600XXMTA**

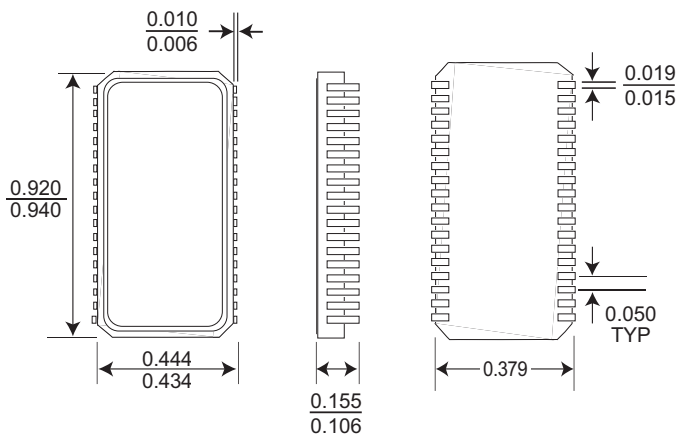
ALL DIMENSIONS ARE IN INCHES

PACKAGE 321: 32 PIN THINPACK™ FLATPACK, SMD 5962-95600XXMYA

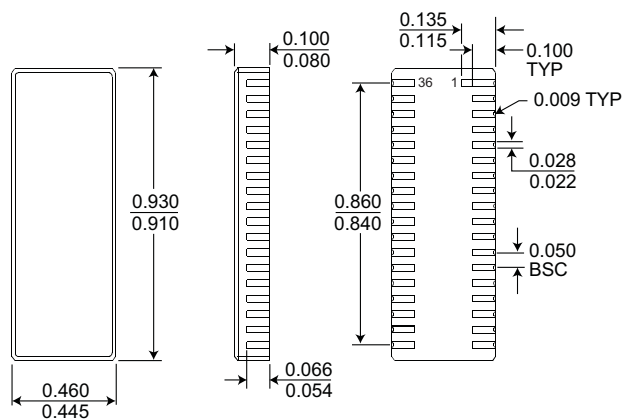
ALL DIMENSIONS ARE IN INCHES

PACKAGE 344: 32 PIN CERAMIC FLATPACK, SMD 5962-95600XXM9A

ALL DIMENSIONS ARE IN INCHES

**PACKAGE 327: 36 LEAD CERAMIC SOJ, SMD 5962-95600XXMMA**

ALL DIMENSIONS ARE IN INCHES

PACKAGE 502: 36 LEAD CERAMIC LCC, SMD 5962-95600XXMNA (PENDING)

ALL DIMENSIONS ARE IN INCHES



ORDERING INFORMATION

	EDI	8	8	512	CA	X	X	X
WHITE ELECTRONIC DESIGNS								
SRAM								
ORGANIZATION, 512Kx8								
TECHNOLOGY:								
CA = CMOS Standard Power								
LPA = Low Power								
ACCESS TIME (ns)								
PACKAGE TYPE:								
C = 32 lead Sidebrazed DIP, 600 mil (Package 9)								
K = 36 lead Ceramic LCC (Package 502)								
N = 32 lead Ceramic SOJ (Package 140)								
T = 32 lead Sidebrazed DIP, 400 mil (Package 326)								
B32 = 32 pin Ceramic Thinpack™ Flatpack (Package 321)								
F32 = 32 pin Ceramic Flatpack (Package 344)								
F36 = 36 pin Ceramic Flatpack (Package 316)								
N36 = 36 lead Ceramic SOJ (Package 327)								
DEVICE GRADE:								
B = MIL-STD-883 Compliant								
M = Military Screened								
I = Industrial								
C = Commercial								