

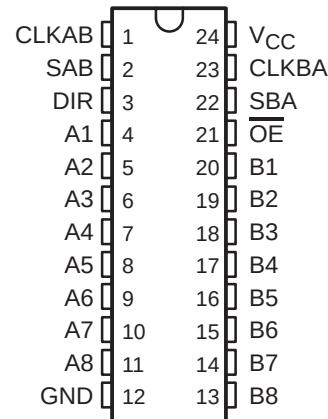
CD74FCT646

BiCMOS OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCBS735A – JULY 2000 – REVISED JULY 2000

- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From V_{CC}
- Controlled Output Edge Rates
- 64-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (EN) DIP

EN, M, OR SM PACKAGE
(TOP VIEW)



description

The CD74FCT646 is an octal bus transceiver with 3-state outputs. It consists of D-type flip-flops and control circuitry, arranged for multiplexed transmission of data directly from the input bus or from the internal registers. The device uses a small-geometry BiCMOS technology. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input.

The D-type flip-flops act as internal storage registers on the low-to-high transition of either CLKAB or CLKBA. Output-enable ($\overline{OE}$) and DIR inputs control the transceiver functions. Data present at the high impedance output can be stored in either register, or both; however, only one of the two buses can be enabled as outputs at any one time. The select-control (SAB and SBA) inputs can multiplex stored and transparent (real time) data. The direction control (DIR) determines which data bus receives data when $\overline{OE}$ is low. In the high-impedance state ($\overline{OE}$ high), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the DIR and $\overline{OE}$ terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

The outputs are a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below V_{CC} . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

$\overline{OE}$ and DIR control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either or both registers.

SAB and SBA can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{OE}$ is active (low). In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

The CD74FCT646 is characterized for operation from 0°C to 70°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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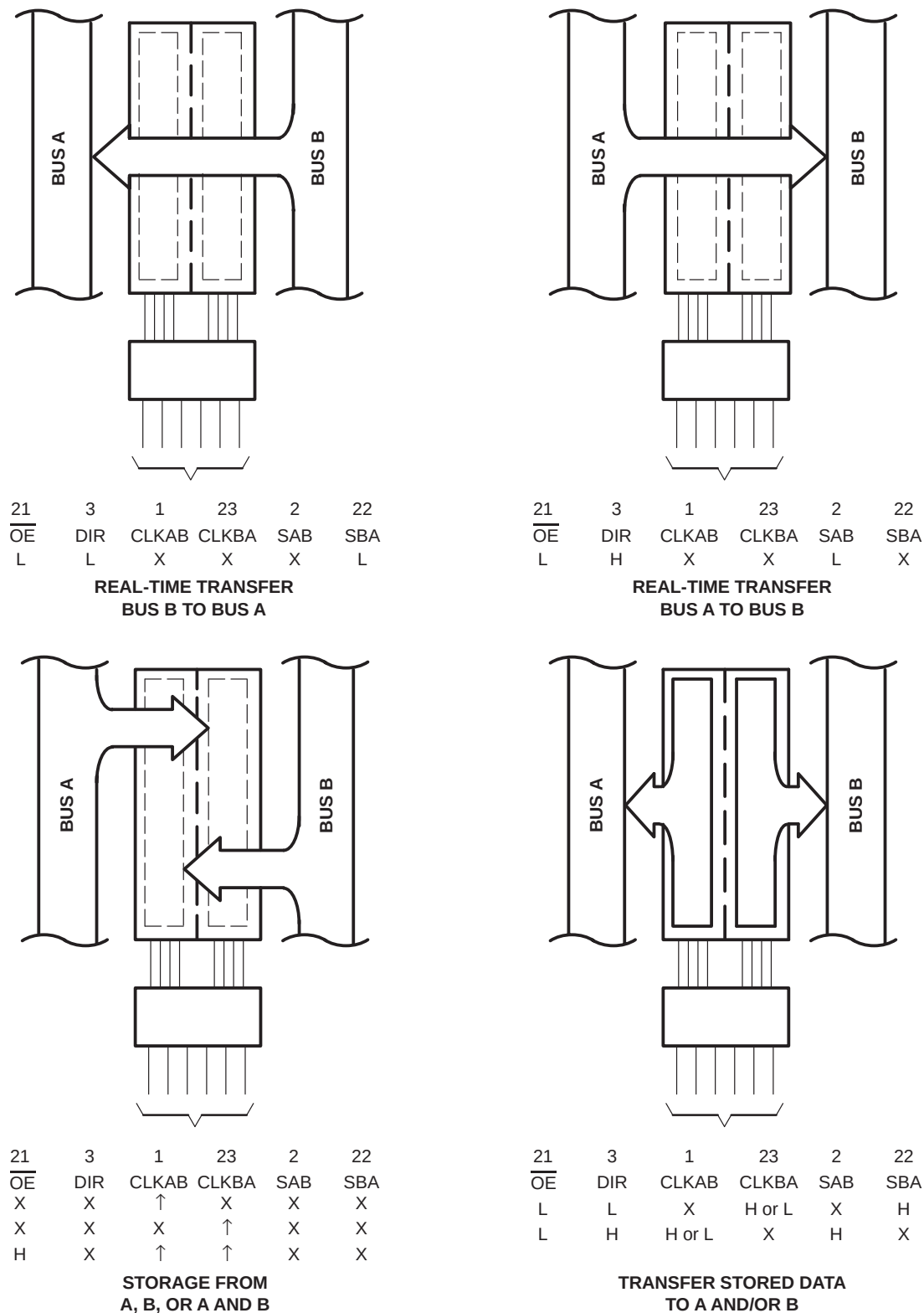


Figure 1. Bus-Management Functions

INPUTS						DATA I/O		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

logic symbol[‡]



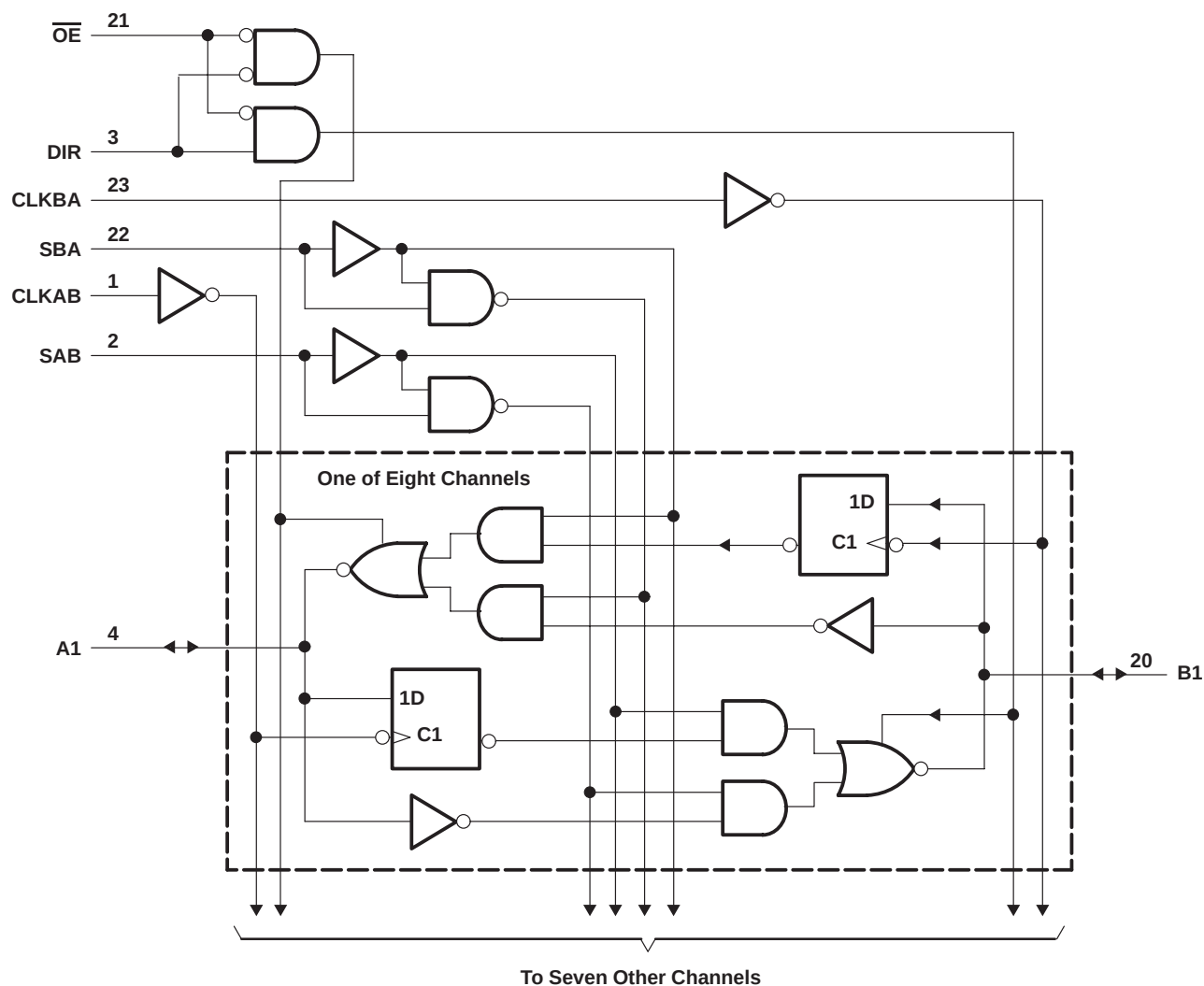
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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

DC supply voltage range, V_{CC}	–0.5 V to 6 V
DC input clamp current, I_{IK} ($V_I < -0.5$ V)	–20 mA
DC output clamp current, I_{OK} ($V_O < -0.5$ V)	–50 mA
DC output sink current per output pin, I_{OL}	70 mA
DC output source current per output pin, I_{OH}	–30 mA
Continuous current through V_{CC} , I_{CC}	140 mA
Continuous current through GND	528 mA
Package thermal impedance, θ_{JA} (see Note 1): EN package	67°C/W
M package	46°C/W
SM package	61°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.75	5.25	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	V
I_{OH} High-level output current		–15	mA
I_{OL} Low-level output current		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	ns/V
T_A Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
V_{IK}	$I_I = -18$ mA	4.75 V	–1.2		–1.2		V
V_{OH}	$I_{OH} = -15$ mA	4.75 V	2.4		2.4		V
V_{OL}	$I_{OL} = 64$ mA	4.75 V		0.55		0.55	V
I_I	$V_I = V_{CC}$ or GND	5.25 V		± 0.1		± 1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.25 V		± 0.5		± 10	μA
$I_{OS}^\ddagger$	$V_I = V_{CC}$ or GND, $V_O = 0$	5.25 V	–60		–60		mA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.25 V		8		80	μA
$\Delta I_{CC}^\S$	One input at 3.4 V, Other inputs at V_{CC} or GND	5.25 V		1.6		1.6	mA
C_i	$V_I = V_{CC}$ or GND			10		10	pF
C_O	$V_O = V_{CC}$ or GND			15		15	pF

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

[§] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC} .



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timing requirements over recommended operating temperature conditions (unless otherwise noted) (see Figure 2)

		MIN	MAX	UNIT
f_{clock}	Clock frequency		85	MHz
t_w	Pulse duration	CLKBA or CLKAB high or low	6	ns
t_{su}	Setup time	A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$	4	ns
t_h	Hold time	A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$	2	ns

switching characteristics over recommended operating temperature conditions (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$	MIN	MAX	UNIT
			TYP			
f_{max}				85		MHz
t_{pd}	CLKBA or CLKAB	A or B	6.8	2	9	ns
	A or B	B or A	6.8	2	9	
	SBA or SAB $\uparrow$	A or B	8.3	2	11	
t_{en}	$\overline{\text{OE}}$	A or B	10.5	2	14	ns
t_{dis}	$\overline{\text{OE}}$	A or B	6.8	2	9	ns

$\uparrow$ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

noise characteristics, $V_{\text{CC}} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

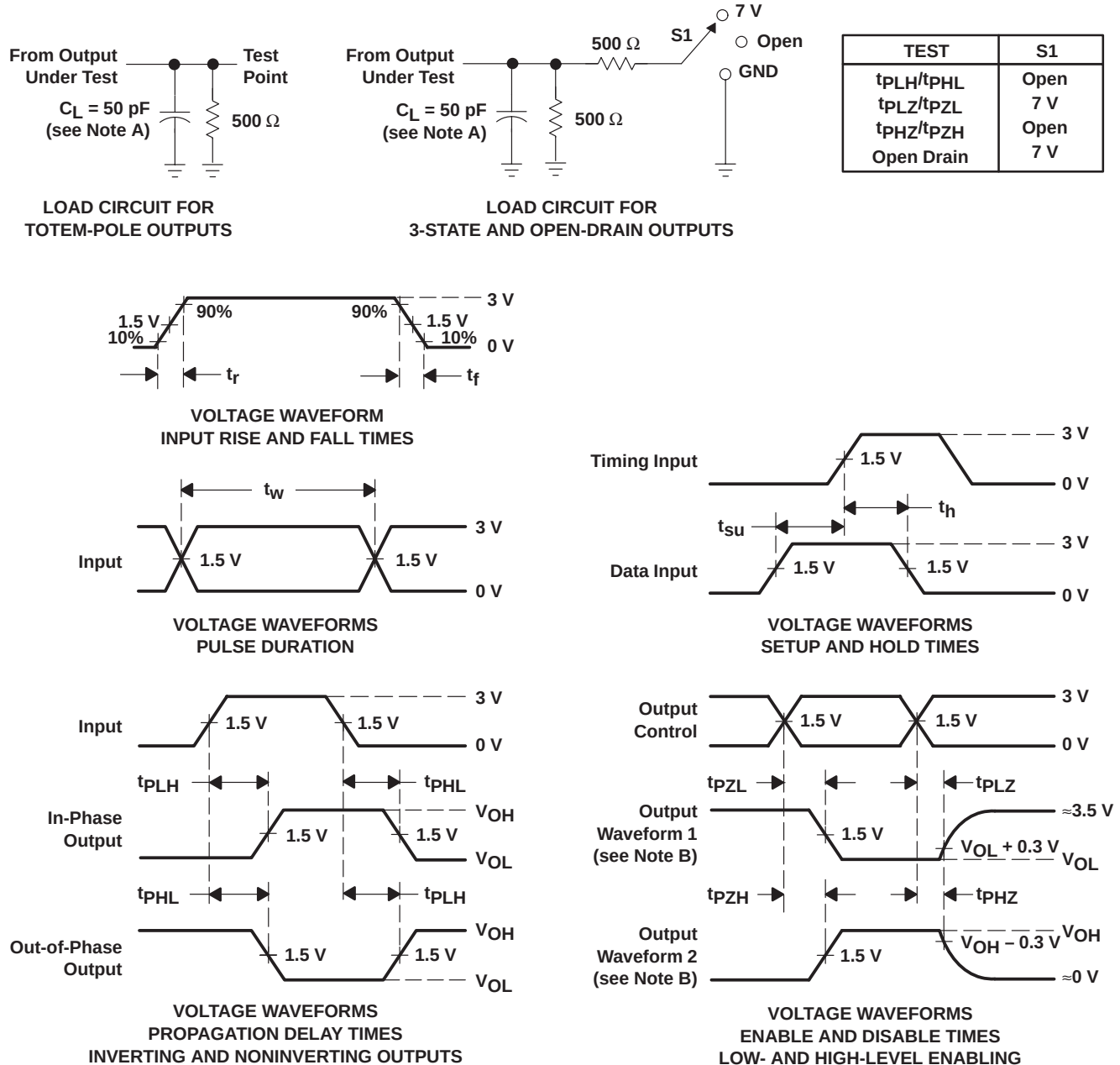
PARAMETER	MIN	TYP	MAX	UNIT
$V_{\text{OL(P)}}$ Quiet output, maximum dynamic V_{OL}		1		V
$V_{\text{OH(V)}}$ Quiet output, minimum dynamic V_{OH}		0.5		V
$V_{\text{IH(D)}}$ High-level dynamic input voltage	2			V
$V_{\text{IL(D)}}$ Low-level dynamic input voltage			0.8	V

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, t_r and $t_f = 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74FCT646EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
CD74FCT646M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
CD74FCT646M96	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
CD74FCT646SM	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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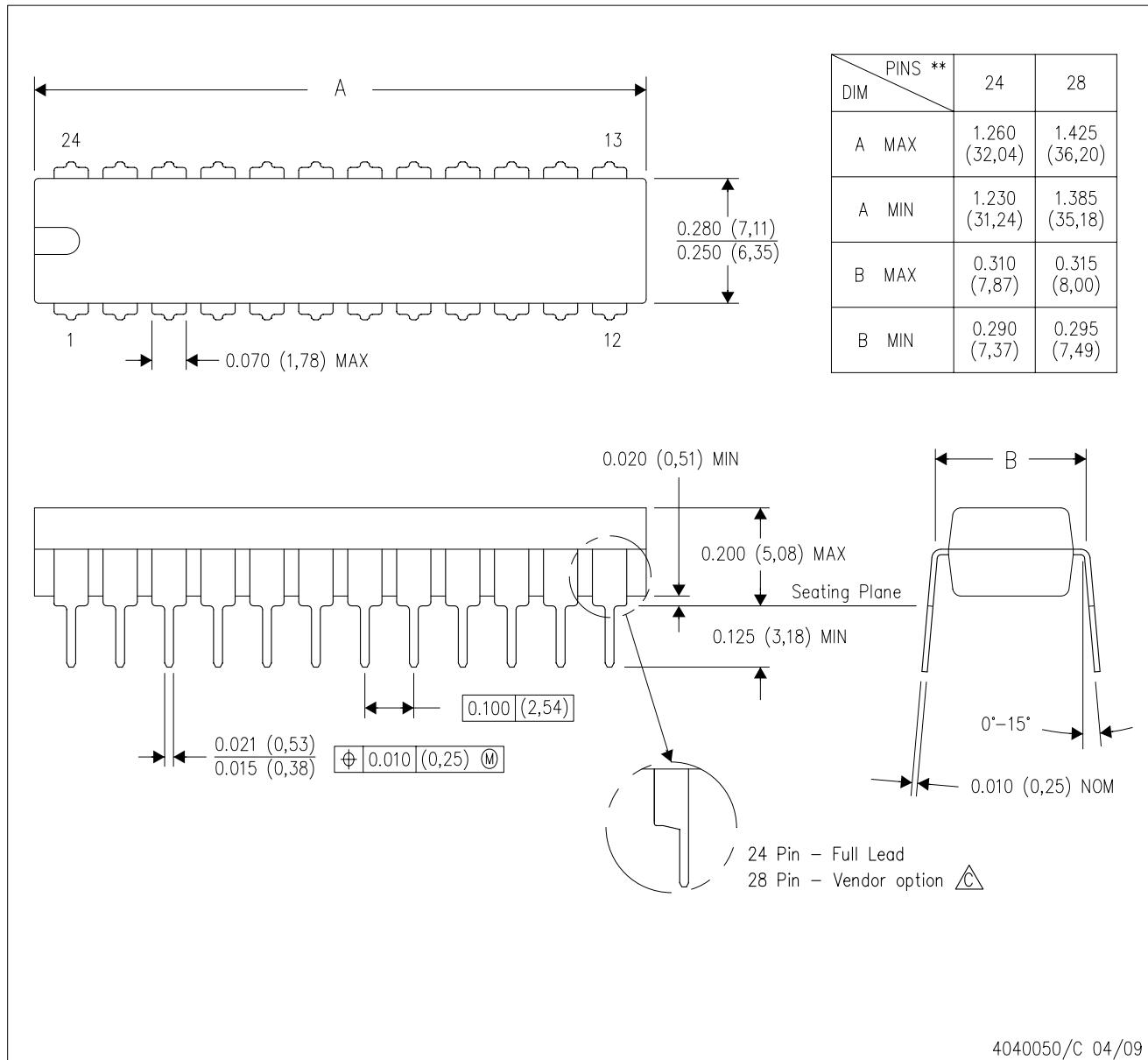
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MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

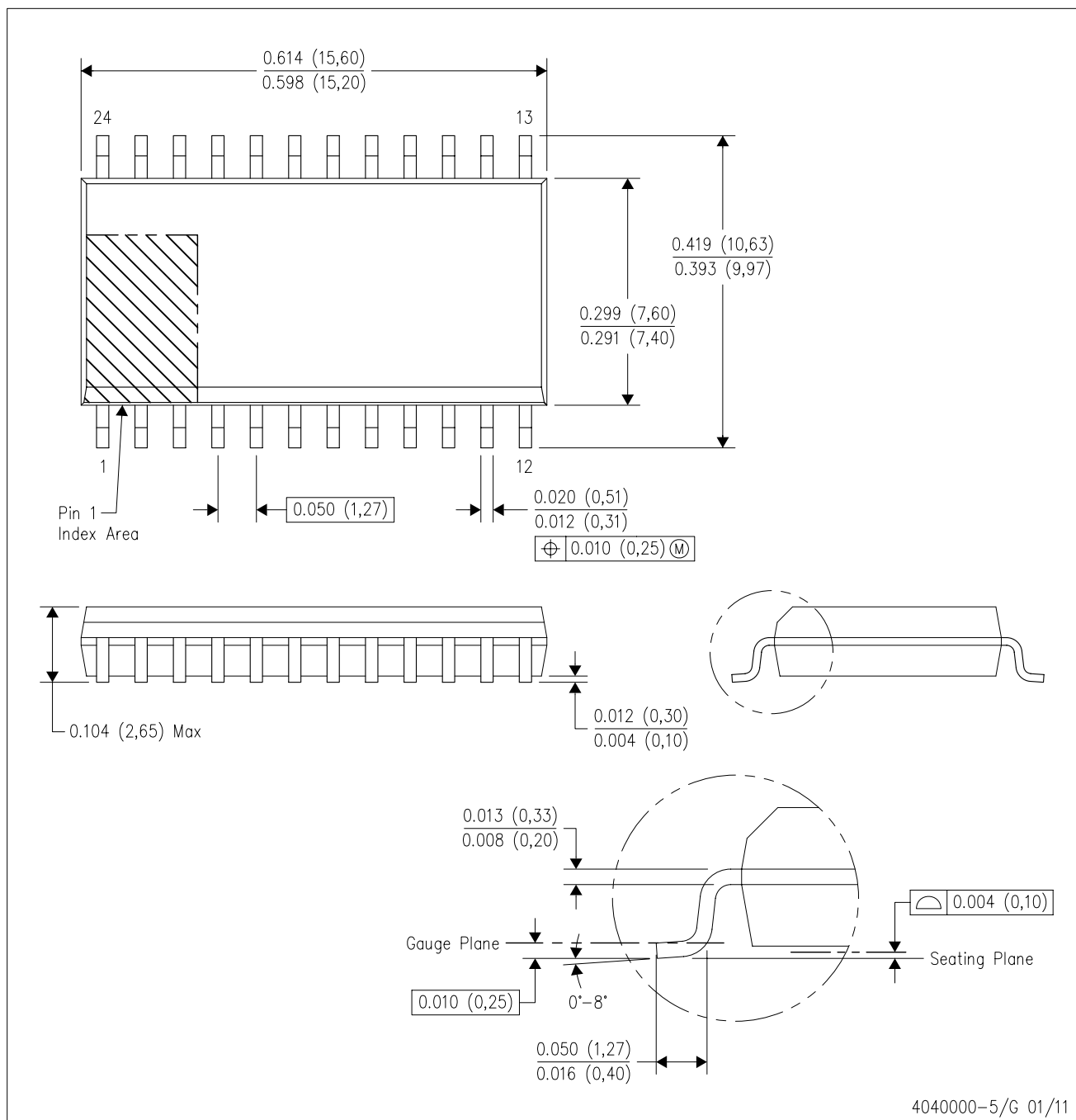
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

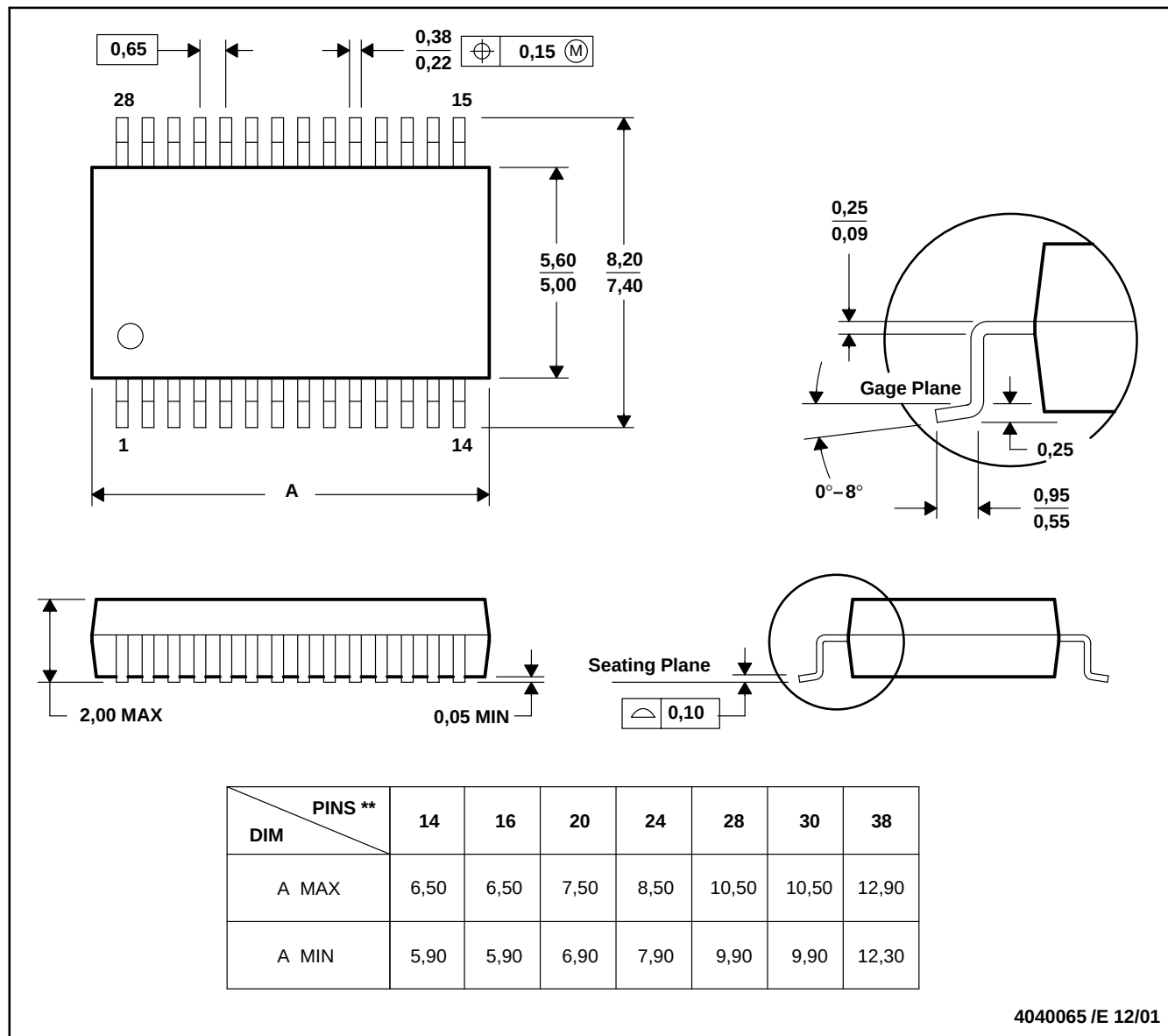


- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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