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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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H7N0310LD, H7N0310LS, H7N0310LM

Silicon N Channel MOS FET
High Speed Power Switching

ADE-208-1422C(Z)

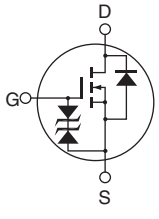
4th. Edition
Aug. 2002

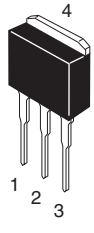
Features

- Low on-resistance
- $R_{DS(on)}$ = 8 mΩ typ.
- Low drive current

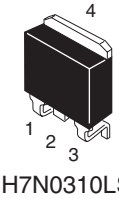
Outline

LDPAK

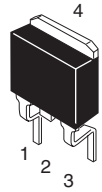




H7N0310LD



H7N0310LS



H7N0310LM

1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	30	A
Drain peak current	$I_{D(pulse)}$ Note 1	120	A
Body-drain diode reverse drain current	I_{DR}	30	A
Channel dissipation	Pch Note 2	50	W
Channel to Case Thermal Impedance	θch-c	2.5	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C

Electrical Characteristics

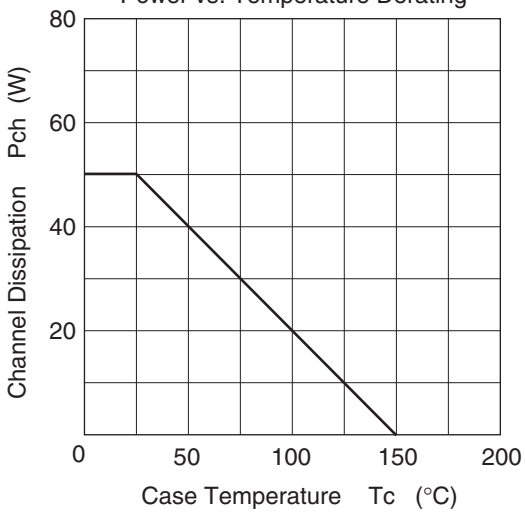
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—		I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V[Note1]
Static drain to source on state resistance	$R_{DS(on)}$	—	8.0	10	mΩ	I_D = 15 A, V_{GS} = 10 V[Note1]
		—	13	19	mΩ	I_D = 15 A, V_{GS} = 5 V[Note1]
Forward transfer admittance	$\|y_{fs}\|$	21	35	—	S	I_D = 15 A, V_{DS} = 10 V[Note1]
Input capacitance	Ciss	—	1400	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	380	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	210	—	pF	f = 1 MHz
Total gate charge	Qg	—	24	—	nc	V_{DD} = 10 V
Gate to source charge	Qgs	—	4.8	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	4.6	—	nc	I_D = 30 A
Turn-on delay time	$t_{d(on)}$	—	21	—	ns	V_{GS} = 10 V, I_D = 15 A
Rise time	t_r	—	250	—	ns	R_L = 0.67 Ω
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	R_g = 4.7 Ω
Fall time	t_f	—	16	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.90	—	V	I_F = 30 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	35	—	ns	I_F = 30 A, V_{GS} = 0 diF/ dt = 50 A/µs

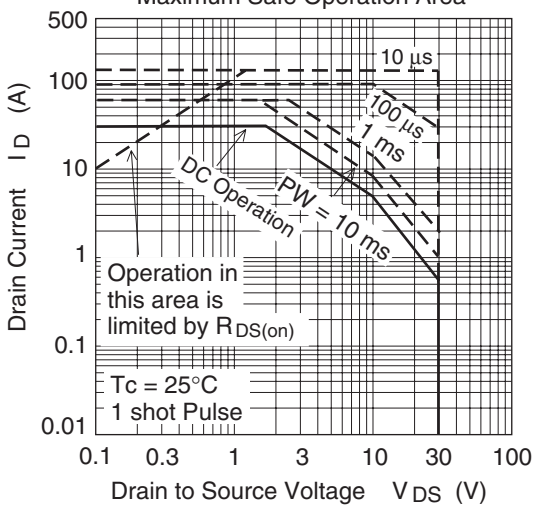
Notes: 1. Pulse test

Main Characteristics

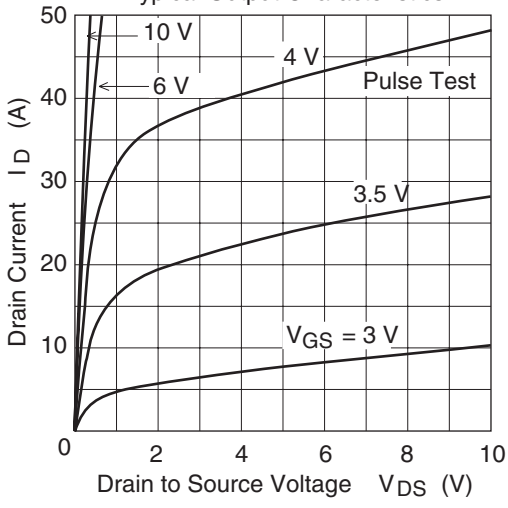
Power vs. Temperature Derating



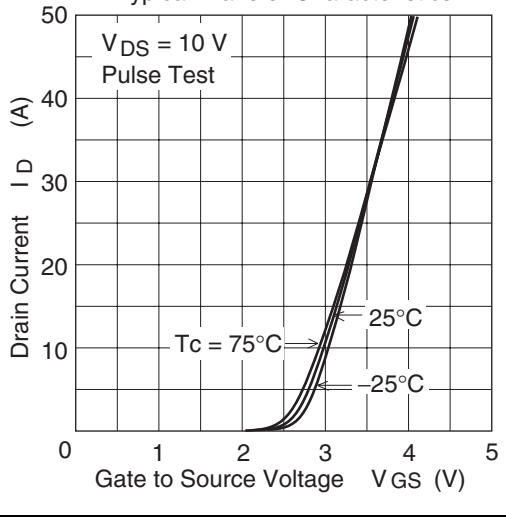
Maximum Safe Operation Area



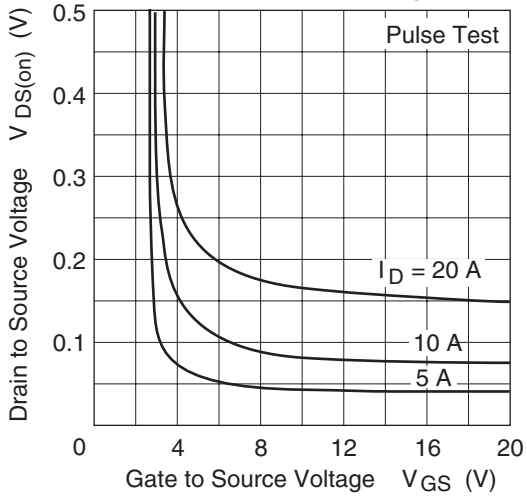
Typical Output Characteristics



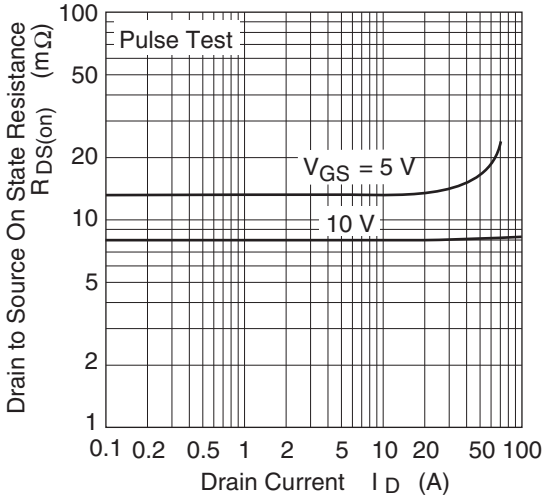
Typical Transfer Characteristics



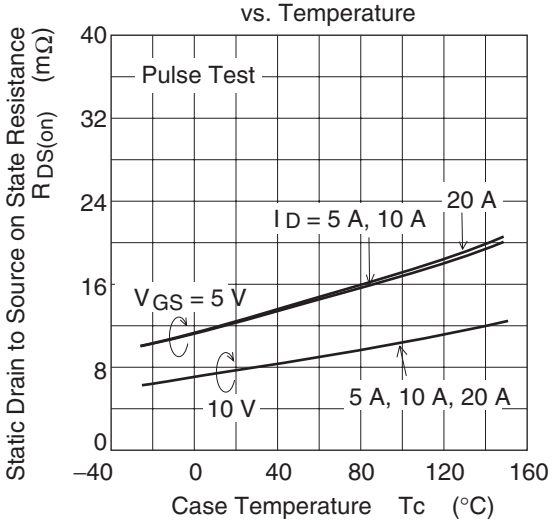
Drain to Source Saturation Voltage vs. Gate to Source Voltage



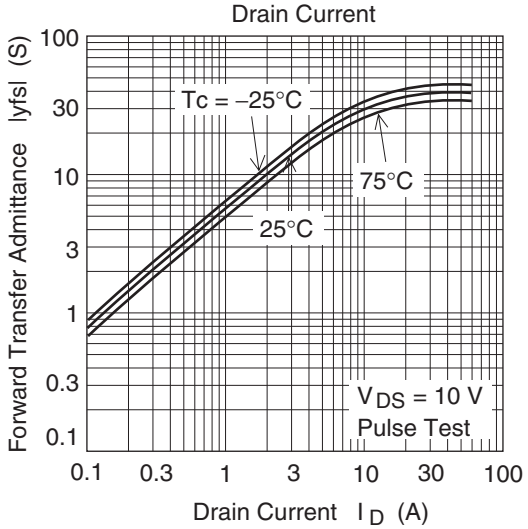
Static Drain to Source on State Resistance vs. Drain Current



Static Drain to Source on State Resistance vs. Temperature

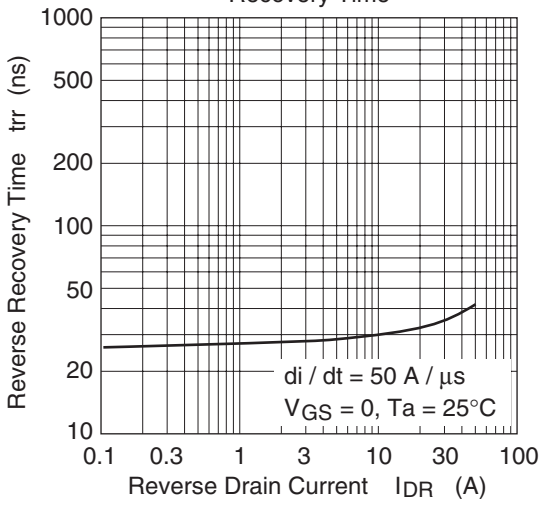


Forward Transfer Admittance vs. Drain Current

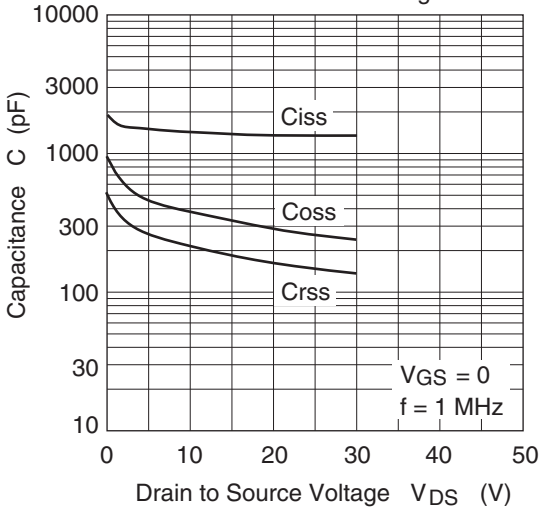


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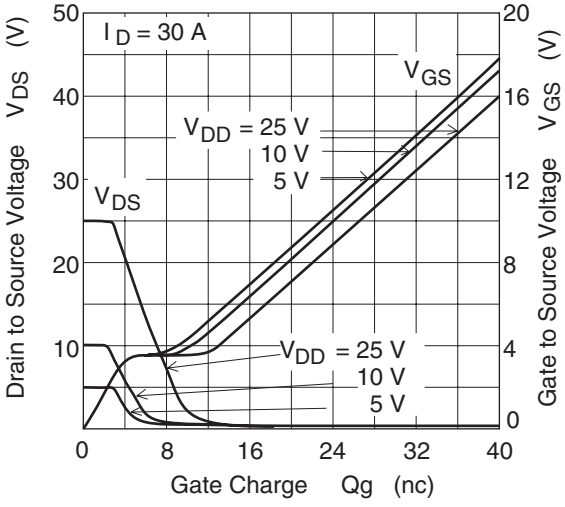
Body-Drain Diode Reverse Recovery Time



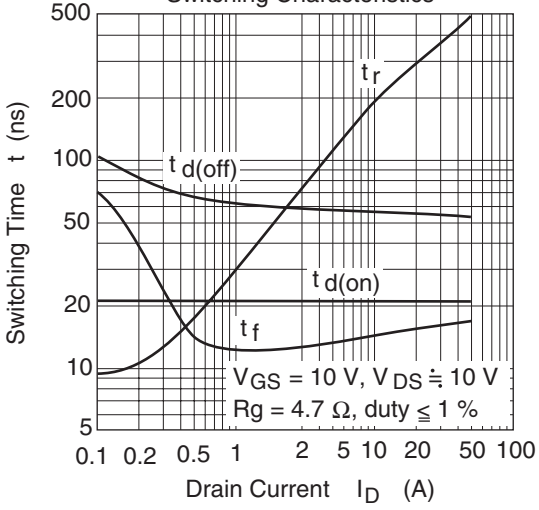
Typical Capacitance vs. Drain to Source Voltage



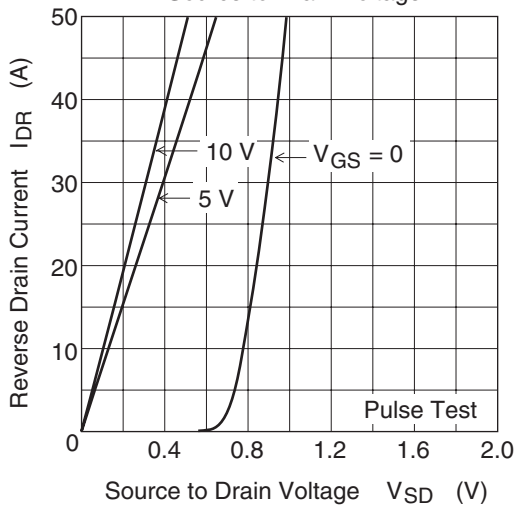
Dynamic Input Characteristics



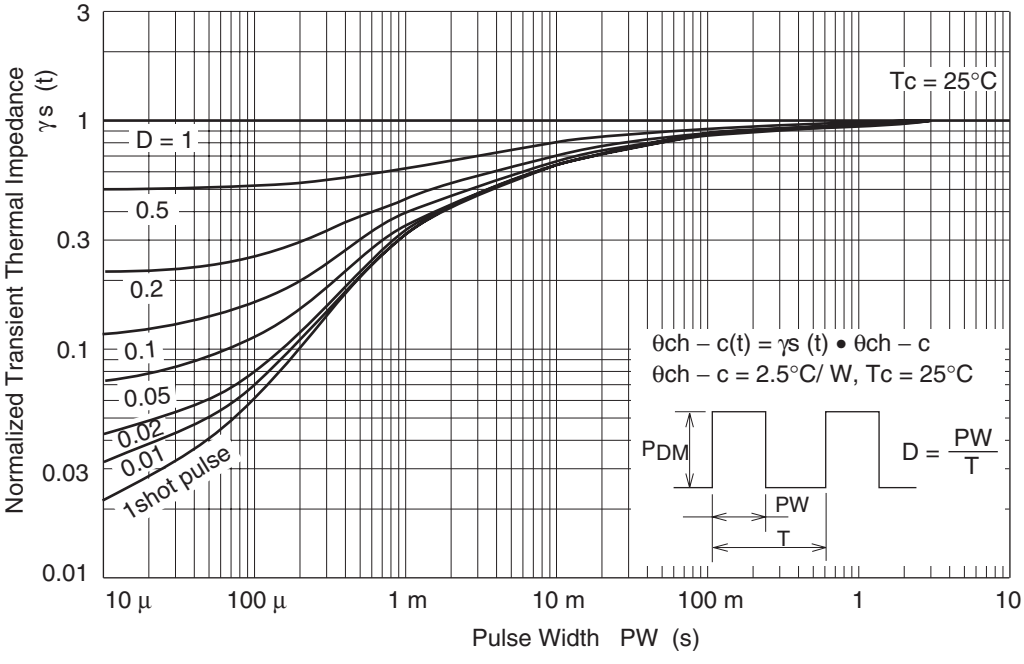
Switching Characteristics



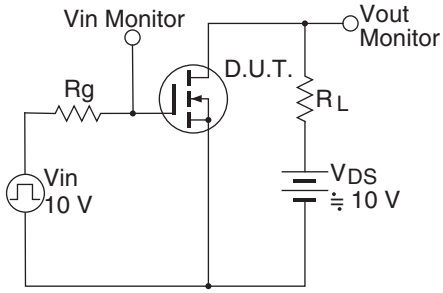
Reverse Drain Current vs.
Source to Drain Voltage



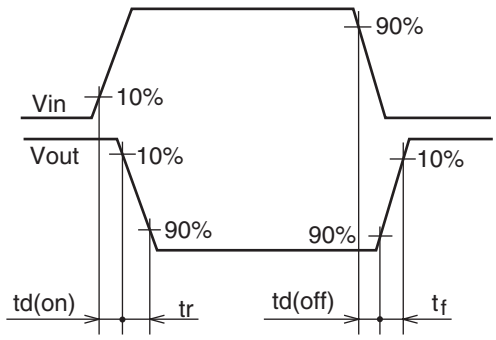
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



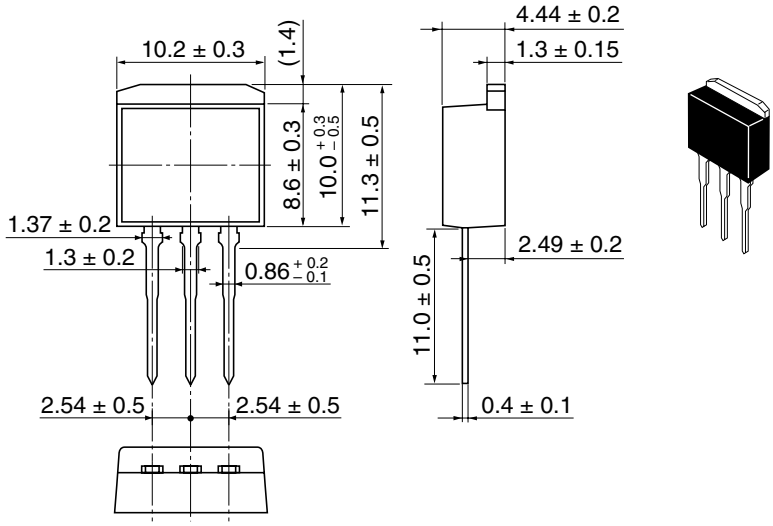
Switching Time Waveform



Package Dimensions

• H7N0310LD

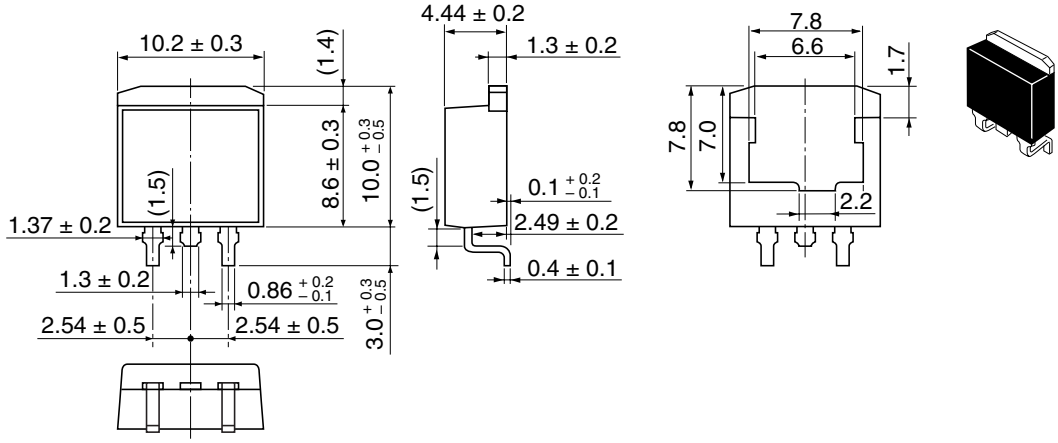
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

• H7N0310LS

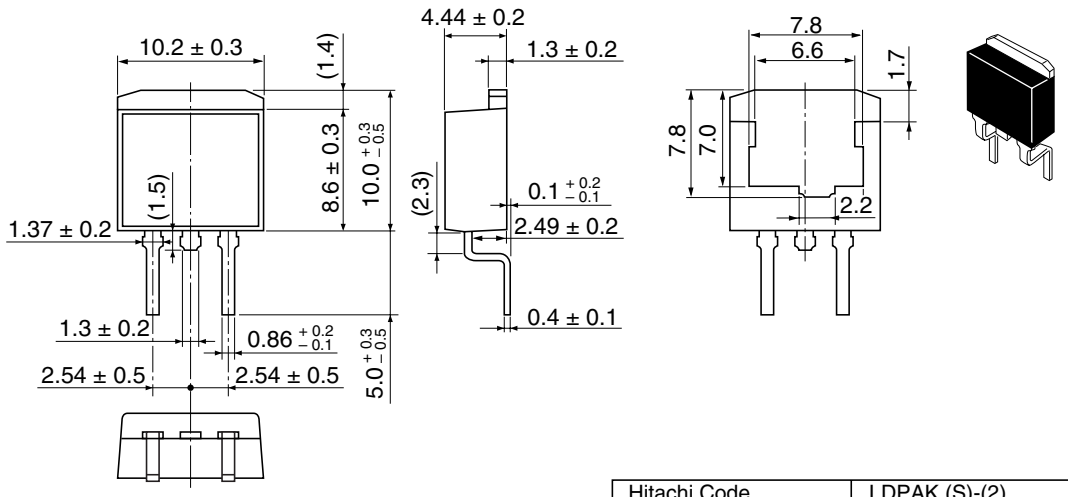
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

• H7N0310LM

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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