

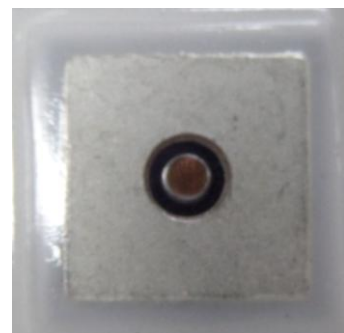
JMC110-12/16/18/20

Description:

- 1) Chip: double mesa SCRs of reverse blocking high-voltage
- 2) Chip area: 12.4mm×12.4mm (central gate thyristor)
- 3) Technology: mesa glass passivation technology, multilayer metallization technology and non-void welding by vacuum welding technology

Typical Application:

Reactive power compensation, solid state relay, power module, etc.



Absolute Maximum Ratings (Packaged into modules, unless otherwise specified, $T_C=25^{\circ}\text{C}$)

Parameter	Test Conditions	Symbol	Values	Unit
Operating junction temperature range		T_j	-40-125	$^{\circ}\text{C}$
Repetitive peak off-state voltage	$T_j=25^{\circ}\text{C}$	V_{DRM}	1200/1600/1800/2000	V
Repetitive peak reverse voltage	$T_j=25^{\circ}\text{C}$	V_{RRM}	1200/1600/1800/2000	V
Average on-state current	$T_C=80^{\circ}\text{C}$	$I_{\text{T(AV)}}$	110	A
Peak on-state surge current	$t_p=10\text{ms}$	I_{TSM}	2500	A
I^2t value for fusing	$t_p=10\text{ms}$	I^2t	31250	A^2s
Critical rate of rise of on-state current	$V_D=2/3V_{\text{DRM}}$ $t_p=200\mu\text{s}$ $I_G=0.3\text{A } T_j=125^{\circ}\text{C}$ $dI_G/dt=0.3\text{A}/\mu\text{s}$	dI/dt	150	$\text{A}/\mu\text{s}$

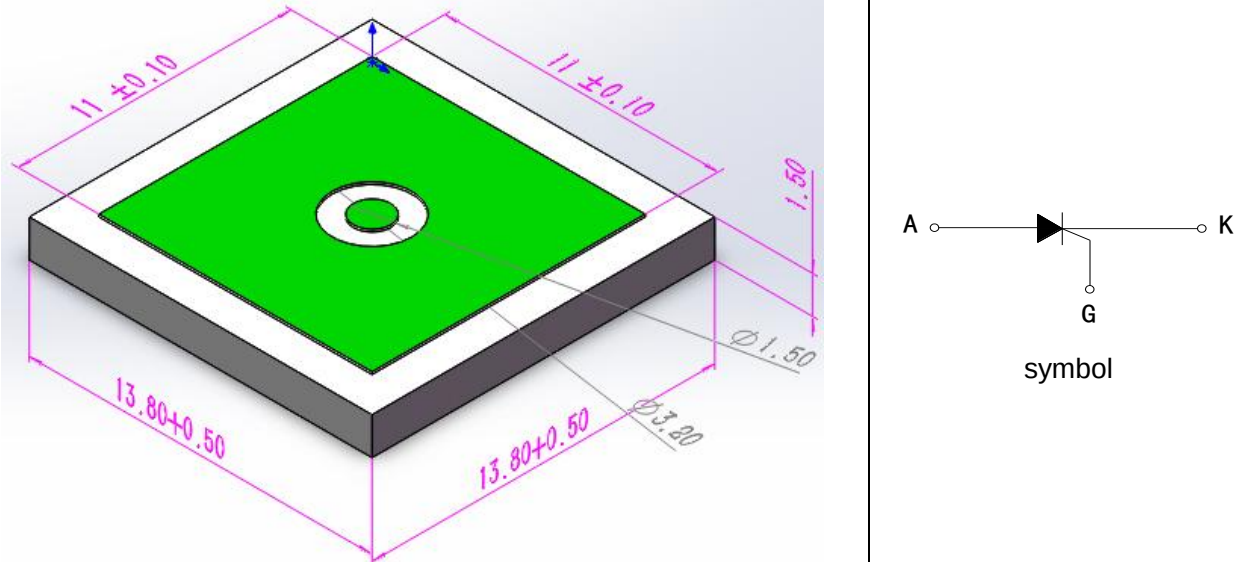
Electrical Characteristics (Packaged into modules, unless otherwise specified, $T_C=25^{\circ}\text{C}$)

Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	$I_T=350\text{A } t_p=380\mu\text{s}$	V_{TM}	≤ 1.8	V
Repetitive peak off-state current	$V_D=V_{\text{DRM}}$ $T_C=25^{\circ}\text{C}$	I_{DRM1}	≤ 100	μA
	$T_C=125^{\circ}\text{C}$	I_{DRM2}	≤ 20	mA
Repetitive peak reverse current	$V_R=V_{\text{RRM}}$ $T_C=25^{\circ}\text{C}$	I_{RRM1}	≤ 100	μA
	$T_C=125^{\circ}\text{C}$	I_{RRM2}	≤ 20	mA
Triggering gate current	$V_D=12\text{V } R_L=30\Omega$	I_{GT}	20-120	mA
Latching current	$I_G=1.2 I_{\text{GT}}$	I_L	≤ 300	mA
Holding current	$I_T=1\text{A}$	I_H	≤ 250	mA



Triggering gate voltage	$V_D=12V$ $R_L=30\Omega$	V_{GT}	≤ 2	V
Non triggering gate voltage	$V_D=V_{DRM}$ $T_j=125^\circ C$	V_{GD}	≥ 0.25	V
Critical rate of rise of voltage	$V_D=2/3V_{DRM}$ $T_j=125^\circ C$ Gate Open	dV/dt	≥ 1000	V/ μs

Mechanical Characteristics

Module size	13.8 mm×13.8 mm
Module thickness	1.6 mm
Welding area of cathode electrode	11 mm×11 mm
Welding area of control electrode	φ 1.5 mm
	

Working Conditions

- 1) No severe mechanical shock as impact and drop off in the process of transportation, storage and working of product.
- 2) Storage conditions
Temperature: 5~40℃
Relative humidity: ≤45%
Storage time: 3 days for the open package; 3 months for the closed package
- 3) Welding conditions
Recommended solder component: Sn63Sb37 (or lead-free solder of liquid quadrant less than 240℃)
Recommended soldering conditions: shown in Table 1
- 4) Welding in the gate spot is recommended to be completed one-time by using fixture. If it is necessary to use a soldering iron, the temperature of soldering iron is controlled within 280℃ and time is controlled within 20s.

Table 1

Sn63Sb37 Soldering conditions			
Average heating rate		3°C/s (Max)	
Preheating activation	Low limit of temperature	T _s (Min)	100°C
	Upper limit of temperature	T _s (Max)	150°C
	Time (min ~ max)	t _s	60 ~ 90s
Reflow zone	Melting point temperature	T _L	183°C (Sn63Sb37)
	Peak temperature	T _P	240°C (+0/-5°C)
	Reflow time (Peak temperature ±5°C)	t _p	10~30s
	Melting time	T _L	40~60s
Maximum cooling rate		3.5°C/s	
Recommended process time		300 ~ 360s	

Ordering Information

J	M	C	110	-16
JieJie Microelectronics Co.,Ltd				12:V _{DRM} /V _{RRM} ≥1200V 16:V _{DRM} /V _{RRM} ≥1600V 18:V _{DRM} /V _{RRM} ≥1800V 20:V _{DRM} /V _{RRM} ≥2000V
Module of series		C:Central gate	I _{T(AV)} =110A	